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Object name: IBM Systems Reference Library - IBM System/360 Model 44 - Functional Characteristics
Vintage: c.196x
Synopsis: IBM.

Description:
The System/360 Model 44 was a mainframe computer system manufactured by IBM, one of which was installed in 1969 in the Department of Computer Science in TCD, see the Hardware category of this catalog. The functional characteristics are thoroughly described in this document.

For the front and rear covers, title pages, table of contents, selected content, etc, see Figure 1 onwards below.

The homepage for this catalog is at: https://www.scss.tcd.ie/SCSSTreasuresCatalog/
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Accession Index	Object with Identification
TCD-SCSS-V.20160425.002	IBM Systems Reference Library - IBM System/360 Model 44 - Functional Characteristics, IBM, c.196x.
TCD-SCSS-V.20121208.258	IBM Systems Reference Library - IBM System/360 Model 44 - Functional Characteristics, IBM, c.196x.
TCD-SCSS-T.20121208.018	IBM 360/44 console and subsystems, Control panel, CPU logic, core memory from IBM 360/44 installed in Trinity College Dublin to provide a service to all sectors of College, including the Dept.Computer Science, from 1969, c.1969.

References:

1. Wikipedia, IBM System/360 Model 44, see: https://en.wikipedia.org/wiki/IBM_System/360_Model_44 Last browsed to on 18-Jun-2016.

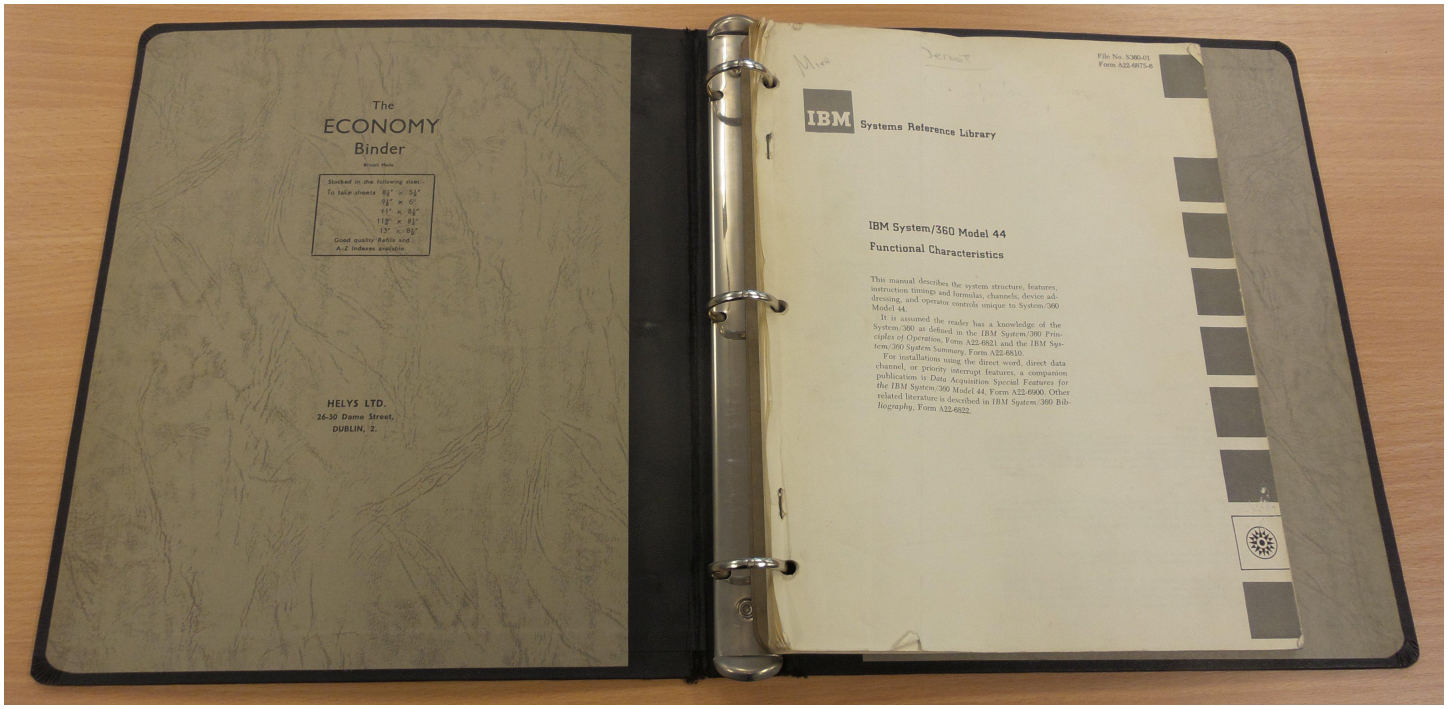


Figure 1: IBM 360/44 Functional Characteristics, folder opened on front page

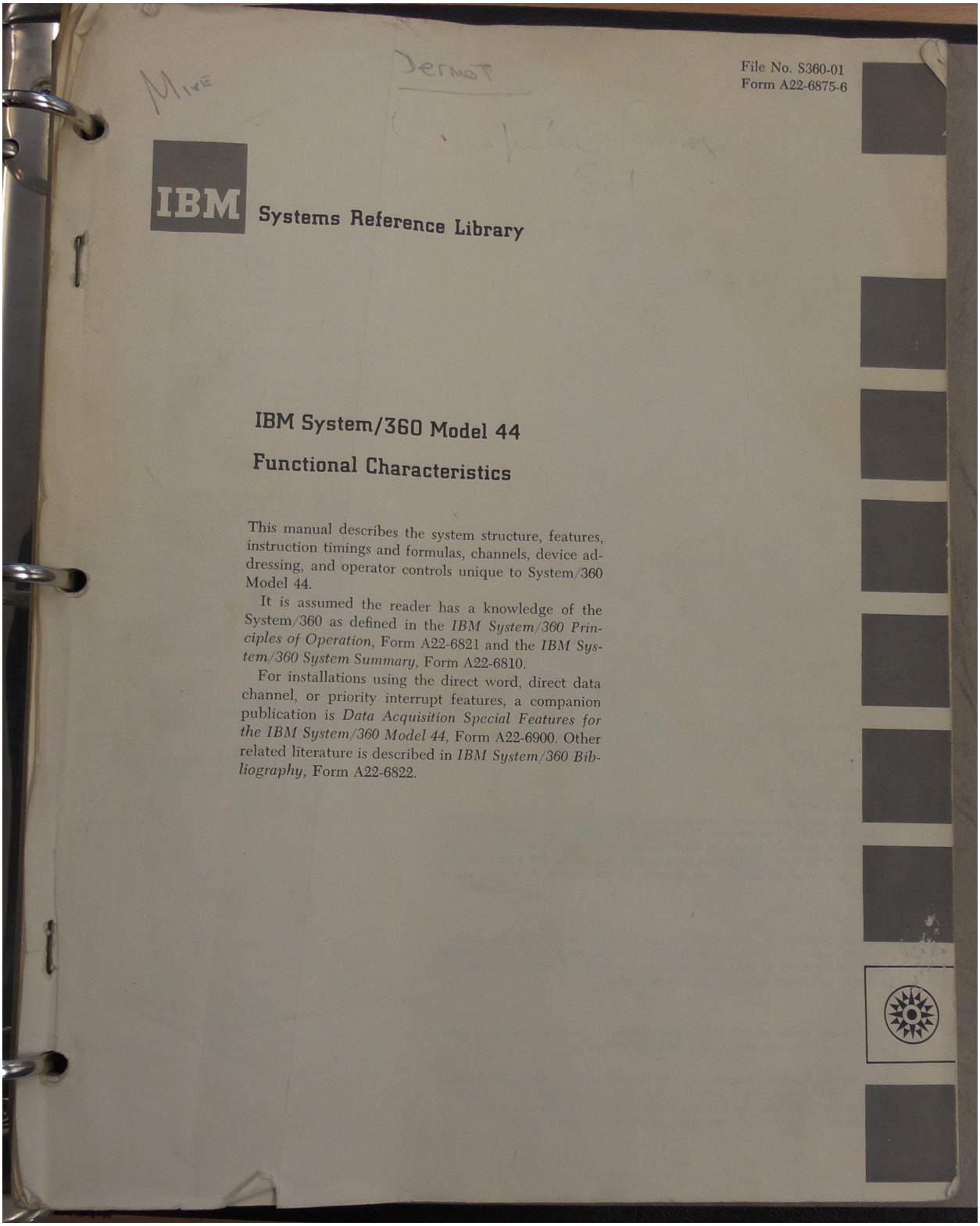
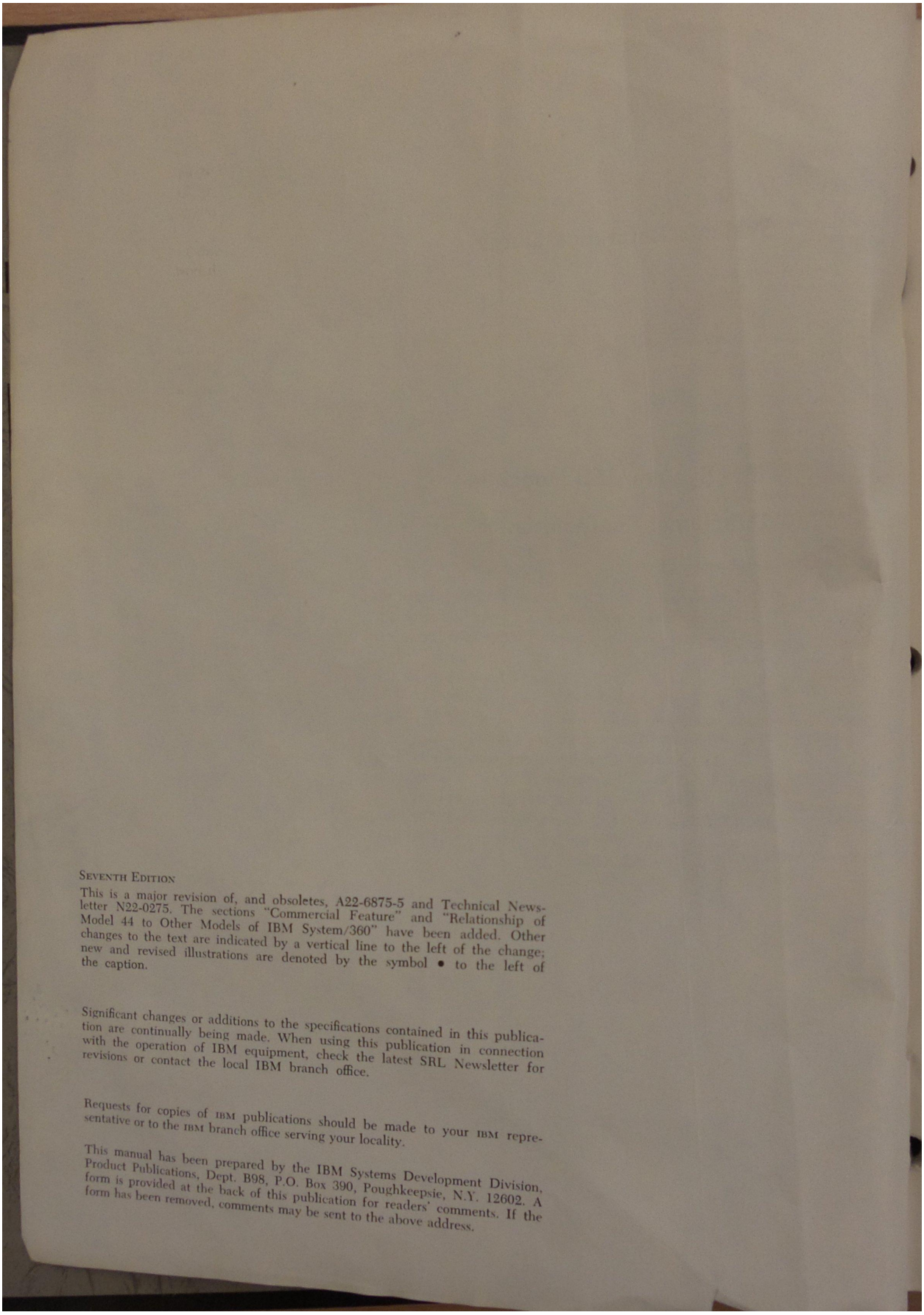


Figure 2: IBM 360/44 Functional Characteristics, Page 1 (front cover)



SEVENTH EDITION

This is a major revision of, and obsoletes, A22-6875-5 and Technical Newsletter N22-0275. The sections "Commercial Feature" and "Relationship of Model 44 to Other Models of IBM System/360" have been added. Other changes to the text are indicated by a vertical line to the left of the change; new and revised illustrations are denoted by the symbol • to the left of the caption.

Significant changes or additions to the specifications contained in this publication are continually being made. When using this publication in connection with the operation of IBM equipment, check the latest SRL Newsletter for revisions or contact the local IBM branch office.

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This manual has been prepared by the IBM Systems Development Division, Product Publications, Dept. B98, P.O. Box 390, Poughkeepsie, N.Y. 12602. A form is provided at the back of this publication for readers' comments. If the form has been removed, comments may be sent to the above address.

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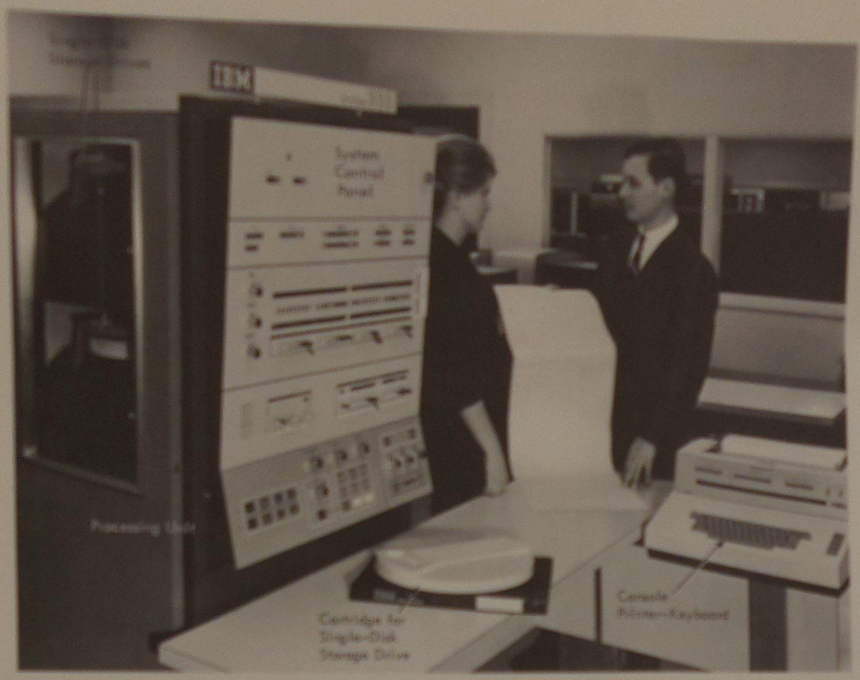


IBM System/360 Model 44

Figure 5: IBM 360/44 Functional Characteristics, Page 4

Model 44, a new member of the IBM System/360, is tailored to handle all relatively small to medium-sized scientific applications and advanced data acquisition and process control applications. Although the Model 44 is thus specialized, its inclusion within the context of System/360 philosophy provides for a very large addressing capability, a wide range of high-speed storage capacities, and I/O multiplexing on channels of low and high data-transfer rates.

The basic Model 44 is unilaterally compatible with System/360 Models 30 through 91. That is, a program written for the Model 44 can be executed on any of these other models if the compatibility constraints of System/360 are observed. However, programs that depend on special features available for only the Model 44 cannot be run on any other System/360 model. These features are: the selection of less than eight bytes for long-precision floating-point arithmetic (to be discussed) and three features (direct word, direct data channel, and priority interrupt) described in *Data Acquisition Special Features for the IBM System/360 Model 44*, Form A22-6900.

Model 44 was derived from standard System/360 architecture by including only those capabilities and instructions that are required for a binary and scientific model. The Model 44 therefore excludes 19 instructions that are normally included in the standard instruction set; those excluded are decimal arithmetic and other variable-field-length instructions.

One or more multiplexer channels, providing a choice of two data transfer rates, can be included in the Model 44 system. (Model 44 cannot be equipped with selector channels; however, a multiplexer channel in which one of its subchannels is operating in burst mode performs very similarly to a selector channel.)

Model 44 uses conventional high-speed sequential logic control instead of read-only storage.

Although the Model 44 processing unit is about the same in physical size (Figure 1) as that of its nearest neighbor, the Model 50, its performance on problems for which it is optimized is 30 to 60 per cent faster than that of a Model 50. Performance figures depend much on the specific applications and optional equipment selected, namely: storage size, number and speed of channels, and quantity and speed of I/O devices supporting the CPU.

The Model 44 processing unit contains, as standard equipment, a single-disk storage drive (capacity 1,171,200 bytes) used for programming systems residence; the necessary disk storage adapter; and an adapter for the console printer-keyboard that is located on the processor table. A second single-disk storage drive, of equal capacity to the first, may be added within the processing unit as a special feature. (See Figure 2.)

All the I/O devices that can be attached to the Model 44 are listed, with channel and control-unit data, in Figure 9.

Processing Unit

As in all other models of the System/360, the smallest addressable data unit is the byte, consisting of eight bits. A ninth bit, called the parity bit (not available to the program), is associated, for checking purposes, with each byte. Because of the optimization of Model 44 toward scientific work, however, the common units of data are the 32-bit binary word and the 16-bit binary halfword, composed of four and two bytes, respectively. Parity is checked upon each data fetch from processor storage and each transfer of data to or from channels.

Floating-point arithmetic uses the 32-bit word for short operands and a 64-bit double word for long operands. Model 44 introduces a new feature, variable long-precision floating-point arithmetic, in which different selections can be made for the length of the fraction when long operands are used. (See "Variable Long-Precision Floating Point.")

Processor storage speed for the Model 44 is 1 microsecond. Four bytes (one word or two halfwords) are stored or fetched in each access. Processor storage, always housed within the CPU, is available in the four capacities shown at the top of Figure 3.

Data paths throughout the CPU are one word wide. Because variable-length fields are not used in Model 44, bytes are handled in groups of two or four; however, they can be manipulated singly by the INSERT CHARACTER, STORE CHARACTER, TEST UNDER MASK, or the five immediate instructions:

AND (NI)
COMPARE LOGICAL (CLI)
EXCLUSIVE OR (XI)
MOVE (MVI)
OR (OI)

Figure 6: IBM 360/44 Functional Characteristics, Page 5

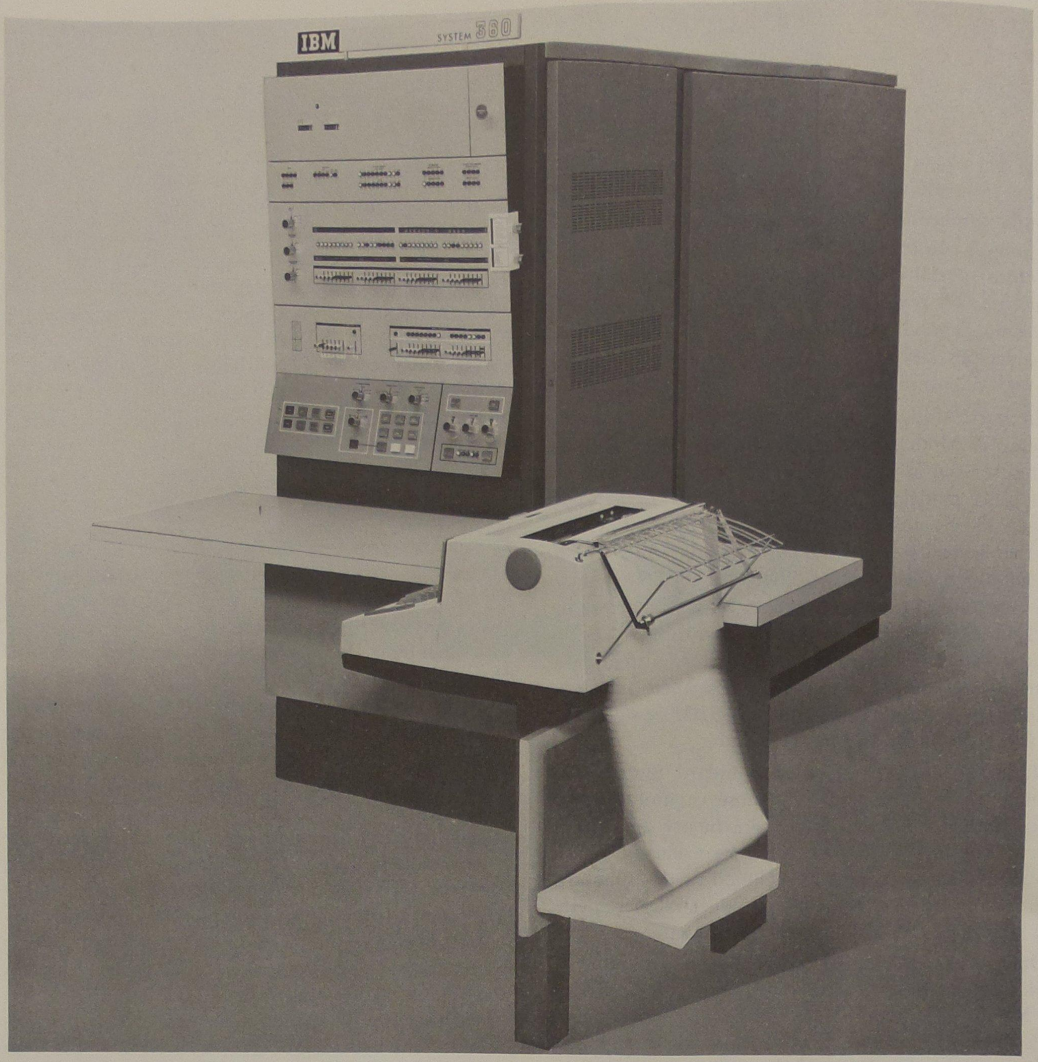


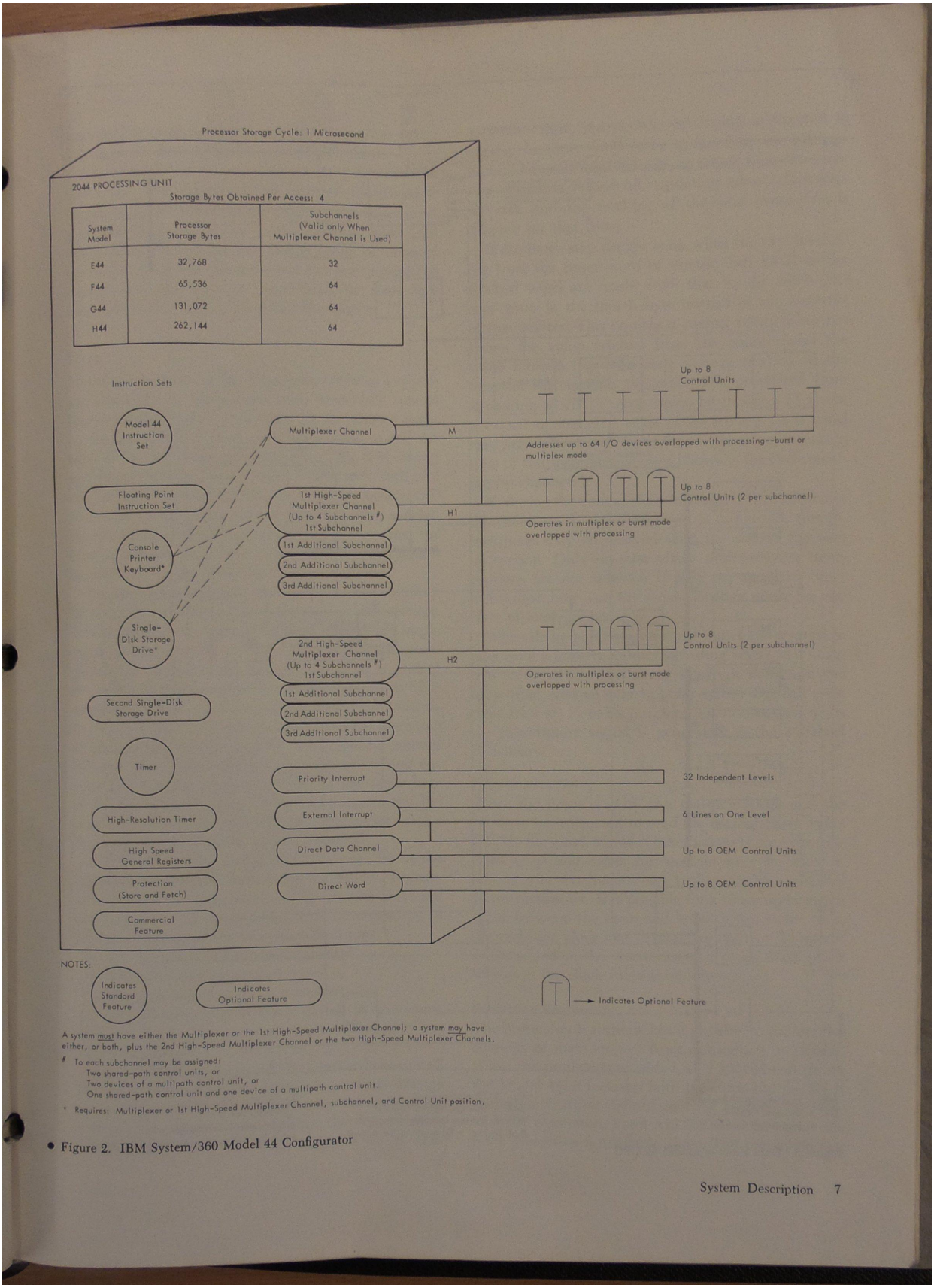
Figure 1. Processing Unit and Console Printer-Keyboard

The 16 general registers of the basic Model 44 are in a normally-unaddressable extension of the 1-microsecond processor storage. (This extension is often called "bump" storage or "core extension.") If the optional high-speed general registers feature (sometimes called "accelerator" feature) is installed, the 16 general registers are provided instead in solid logic technology (SLT) circuitry having 0.25 microsecond read/write time. This quartering of the access periods substantially reduces address generation time as well as the basic execution time of all fixed-point instructions in particular. (See Figures 3 and 7.)

Arithmetic and logical operations are performed between the A and B registers; the results are usually formed in the B register. The Bx register, coupled to the B register with left and right shifting ability, is used in multiply and divide operations and as an auxiliary address register.

If the floating-point feature is installed, the Ax register extends the A register to the 64-bit width needed for long-operand floating-point arithmetic. For long operands, the high-order halves of the floating-point registers are contained in SLT circuitry and the low-order halves are contained in the extension of processor

Figure 7: IBM 360/44 Functional Characteristics, Page 6



• Figure 2. IBM System/360 Model 44 Configurator

Figure 8: IBM 360/44 Functional Characteristics, Page 7

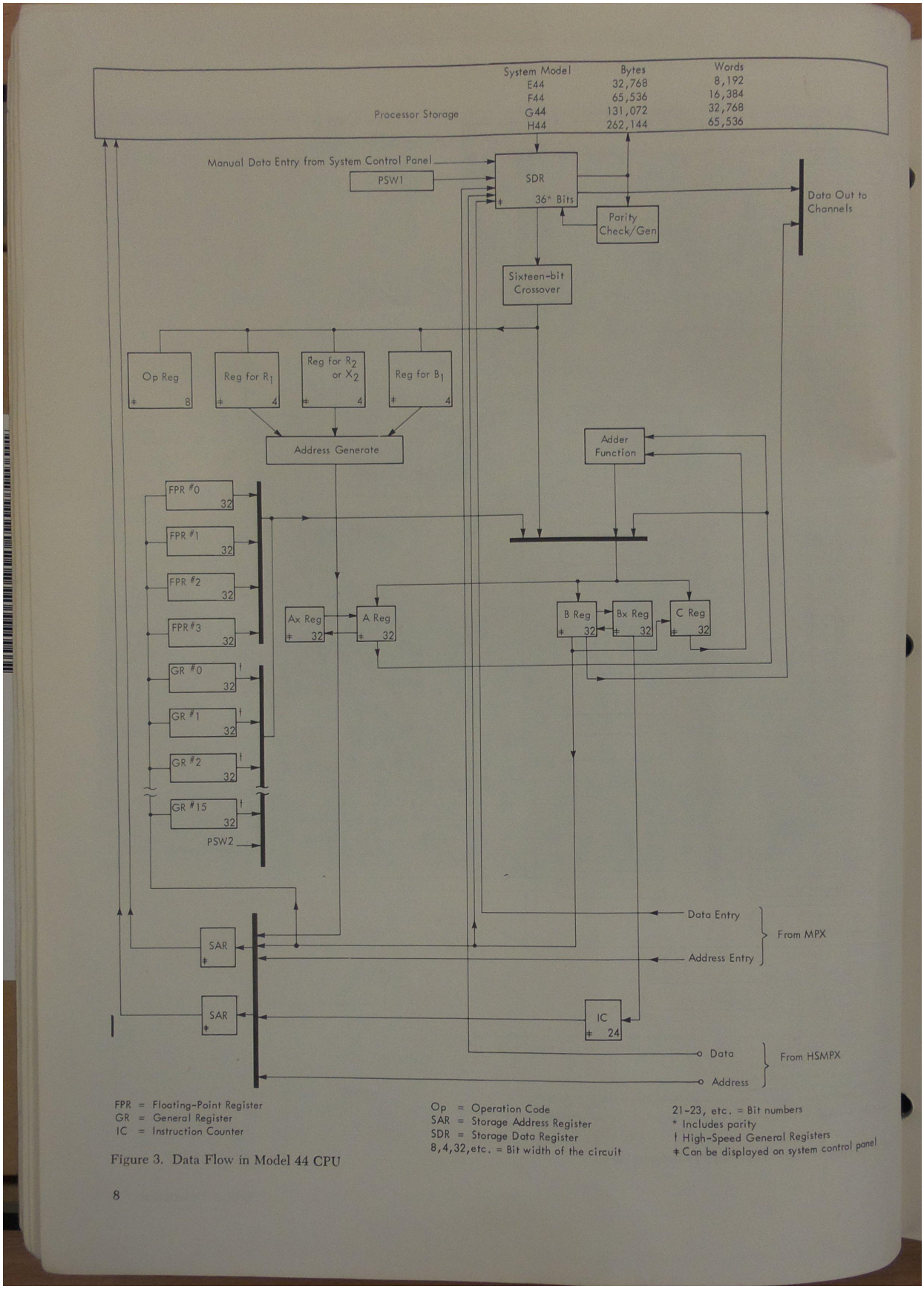


Figure 3. Data Flow in Model 44 CPU

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Figure 9: IBM 360/44 Functional Characteristics, Page 8

storage. For short operands, only the high-order (SLT) halves of the floating-point registers are used.

An optional feature provides six lines for external interrupts. The source of the external interrupts is identified by bits 26-31 of the interruption code in bit positions 16-31 of the old program status word (old PSW). These interrupts are independent of channel operations or of the direct-control feature required to provide external-interrupt capabilities for most System/360 models. Figure 14 shows the PSW.

Timer

Model 44 has either a line-frequency timer as a standard capability or a high-resolution timer as a special feature. Either type can be used as an interval timer to measure elapsed time, or programmed to tell the time of day for program completions, etc. The standard timer is counted down every 1/60th or 1/50th of a second, and is fully described in *IBM System/360 Principles of Operation*, Form A22-6821. The special-feature timer is mentioned therein also; for this, the least significant bit of the 32-bit timer word is decremented and the resolution is 13 microseconds.

The low-order eight bits of the high-resolution timer lie in an SLT-circuit counter rather than in core storage. The contents of the storage address register are monitored for any reference to byte 83, whether addressed directly, or as part of the halfword at 82, or as part of the fullword at 80. When any such reference to 83 is detected, a substitution occurs that causes the contents of the eight-bit counter to participate in the operation in place of the storage byte 83. This eight-bit counter includes the decrementing and parity-generating circuits and acts for all purposes as the low-order byte of the timer word. Byte 83 in the storage array becomes unaddressable either by CPU instructions or by channels, and its bits cannot be displayed.

A 76.8-KC oscillator causes the low-order bit of the counter to be decremented at approximately 13-microsecond intervals. Decrementing the counter does not interfere with CPU processing. The decrementing is prevented by any of the following conditions:

1. The initial program is being loaded
2. The CPU is in the stopped state
3. The rate switch is set to INSN STEP
4. The disable interval timer switch is turned on. This switch is for the use of customer engineering (CE) personnel.

Every 1/300th of a second the counter becomes all 1's, and bit 23 is updated whenever access to storage permits. Specifically, when the counter becomes all 1's, a timer step trigger turns on (while the decrementing continues); if the timer step trigger is on at end-operation time, instruction sequencing is stopped to permit the timer word to be updated by the subtraction of 1 from bit position 23, at which time the timer step trigger is turned off. Updating takes 1.75 microseconds, and the fetching of the next instruction is delayed for that time.

If the timer step trigger is on when the CPU is fetching from the timer word in storage, bits 24-31 of the fetched word are made zero; that is, the fetch gets only zeros in the fourth byte instead of the contents of the counter. This ensures a correct relationship between the value fetched from the counter and the value fetched from the main storage portion of the timer at this instant; the counter is prevented from appearing as all 1's when timer bit position 23 is not yet decremented. The value of the fetched timer word may appear to be off by no more than the execution time of the instruction (after allowing for cycle-stealing by channels).

If, during the course of an instruction that addresses the timer word, an interruption is requested, this interruption may be delayed until the end of the next instruction. Only machine-check and program interruptions are not delayed. If only the standard timer is installed, however, the delay does not occur for any class of interruption.

When decrementing causes the entire timer word to pass from a positive value (including zero) to a negative value, a standard timer interrupt occurs in the form of an external interruption request. The full cycle time, from all 1's in bit positions 0-23 to the time when the interruption signal is generated, is the standard 15.5 hours.

Programming Note

When the timer is used as a real-time clock and the CPU is to be instructed to read the current timer value and set the clock to some other value, successive fullword LOAD and STORE instructions must be used to simulate the MVC move which is absent from the Model 44 instruction set. It is possible for a timer updating to occur between the LOAD and STORE instructions; thus, the real-time clock may "creep" forward by 13 microseconds, and in the worst case this creep takes place whenever the clock value is changed.

Protection Feature

The protection feature makes it possible to protect the contents of main storage from destruction or misuse. When the protection is added, as a special feature, to the Model 44, it includes both the store and the fetch protection features defined in *IBM System/360 Principles of Operation*, Form A22-6821. Neither store nor fetch protection is available alone. The protection key

Figure 10: IBM 360/44 Functional Characteristics, Page 9

in storage can be changed by the SET STORAGE KEY instruction and inspected by the INSERT STORAGE KEY instruction. Note that these two instructions are added to the Model 44 instruction set only when the protection feature is installed. The instruction timings are included in Figure 7.

In the INSERT STORAGE KEY instruction, bit 28 of the register designated by the first operand is the fetch protection bit and is set to one for both store and fetch protection or to zero for store protection only.

It is possible for the Model 44 to access in one cycle a storage word that straddles a 2,048-byte protection boundary. This can happen only in instruction fetching, at which time a fetch protection violation may cause the instruction to be suppressed. However, Model 44 has time to fetch and compare both storage keys during the one main storage access with no increase in the instruction time.

• Commercial Feature

The System/360 Model 44 is custom-designed for small to medium-size scientific applications and advanced data acquisition and process control applications. The basic instruction set of the Model 44 consequently does not include all the System/360 instructions. To provide Model 44 compatibility with the System/360, the commercial feature adds five of the System/360 standard instructions to the Model 44

Figure 4. Console Printer-Keyboard

Figure 11: IBM 360/44 Functional Characteristics Page 10

capability and enables the Model 44 to execute by emulation 22 System/360 instructions that are not normally a part of the Model 44 basic instruction set.

The commercial feature provides the circuitry and emulator program required to execute 19 instructions of the System/360's standard set and eight instructions of System/360's decimal set. This feature also provides the capability to operate the high-speed multiplexer channels in selector mode, assuming the direct data channel feature is not installed.

The operating controls are described under "Commercial Feature Operating Controls and Procedures." Representative commercial feature instruction timings are shown in Figure 10.

Restrictions

Restrictions on the commercial feature are:

1. The feature is available only for Models F44, G, and H.
2. Model F44 is limited to 32 subchannels.
3. Programs that are run under emulation cannot be time-dependent.
4. The Model 44 configuration must meet the requirements of the operating system in use.
5. If emulation of selector channel operation is required, the Model 44 configuration must include a high-speed multiplexer channel and cannot include the direct data channel feature.
6. Only valid System/360 op codes are emulated. RPQ or special op codes are not included.
7. Throughput is at a degraded rate and varies with the instruction mix.
8. The emulator disable switch does not disable the five standard System/360 instructions (EX, LM, STM, BXH, and BXLE) that are implemented by circuitry.
9. The single-disk storage drive operates with a multiplexer channel. If the drive is used in emulation, it must be connected to a low-speed multiplexer channel; if it is connected to a high-speed multiplexer channel, the selector mode switch must not be on.

Theory of Operation

To emulate an instruction, Model 44 instructions are executed to produce the result that would have been produced by executing the original System/360 instruction. A machine language subroutine for each of the 22 instructions to be emulated exists in an extension of main storage. Whenever one of the 22 specified operation codes (shown in the following list) is decoded during an instruction fetch cycle, the appropriate subroutine is substituted to produce the desired result. In effect, all System/360 instructions of the commercial instruction set become valid when the commercial feature is installed.

FORMAT	CODE	MNEMONIC	NAME
RX	44	*EX	Execute
	4E	CVD	Convert to decimal
	4F	CVB	Convert to binary
RS	86	*BXH	Branch on index high
	87	*BXLE	Branch on index low or equal
	90	*STM	Store multiple
	98	*LM	Load multiple
SS	D1	MVN	Move numerics
	D2	MVC	Move characters
	D3	MVZ	Move zones
	D4	NC	AND characters
	D5	CLC	Compare logical characters
	D6	OC	OR characters
	D7	XC	Exclusive OR characters
	DC	TR	Translate
	DD	TRT	Translate and test
	DE	ED	Edit
	DF	EDMK	Edit and Mark
	F1	MVO	Move with offset
	F2	PACK	Pack
	F3	UNPK	Unpack
	F8	ZAP	Zero and add
	F9	CP	Compare decimal
	FA	AP	Add decimal
	FB	SP	Subtract decimal
	FC	MP	Multiply decimal
	FD	DP	Divide decimal

NOTE: Op codes not listed cause a 01 program interruption in main storage.
*Instructions implemented in circuitry.

Implementation

The implementation of instruction emulation requires additional core storage as residence for the emulator program. The additional storage, called storage extension, although it is an extension of main storage, is not addressable by the user programs.

Three operator switches (see "Operator Control Section") located on the console, provide control over initial program loading of the emulator program, conversion of the high-speed multiplexer channels to selector channels, and enabling of the emulate mode.

Circuitry, in conjunction with the operator controls, does the following:

1. Forces burst mode on all high-speed multiplexer channels, causing them to emulate selector channels, when the selector mode switch is on.
2. Causes all I/O channels to reference only storage extension addresses during an emulator initial program load (IPL).
3. Allows a system reset to set the Model 44 in the emulate mode when the emulator disable switch is set to normal.
4. Recognizes invalid operation codes during instruction fetch cycles in emulate mode.
5. Causes a program interruption that takes its new program status word (PSW) from the corresponding storage extension location, when an invalid op code is detected.
6. Causes the stop key to be inactive during in-

Figure 12: IBM 360/44 Functional Characteristics, Page 11

struction emulation, that is, the CPU stops only after emulation is complete.

7. Causes instruction fetching from storage extension instead of main storage during emulation.

8. Examines bit 8 of load PSW and supervisor call (SVC) instructions. The special use of bit 8 in these instructions in emulate mode is explained later in this section.

With the emulator disable switch set to normal, and the emulator program loaded into storage extension, the CPU is ready to execute all of the commercial instructions used by the System/360. During normal program execution, each instruction fetched is decoded. When the decoded op code is invalid for the Model 44 (is not implemented in circuitry), a 01 program interrupt is signaled, emulate mode is set on, and a program interrupt is taken in storage extension. The program old PSW is stored in storage extension address 28(hex) and the program new PSW is taken from 68(hex). The new PSW places the CPU in the supervisor state disabled to all interrupts. The 16 general registers (GR) are stored, freeing them for use by the emulator program. The instruction address in the old PSW is used to examine the instruction causing entrance to the emulator. If it is System/360 invalid, or an execute exception, the old PSW in extension storage is moved to the program old PSW area in main storage location 28(hex). The program new PSW from main storage location 68(hex) is then loaded and emulation mode is turned off. This procedure simulates a code 01 program interruption to the problem program.

If the instruction causing entrance to the emulator is System/360 valid, the appropriate subroutine of the emulator is executed to simulate the decoded instruction.

Satisfactory completion of the emulation subroutine is followed by a load PSW instruction with bit 8 of the instruction set to 1. This instruction resets the emulate mode and loads the modified old PSW from the storage extension location 20(hex) to become the current PSW in resumption of the main program. Note that the load PSW instruction, with bit 8 set to 1, serves the additional function of resetting the emulate mode. Similarly, bit 8 of the supervisor call (SVC) instruction serves a special function. Because the emulator always operates in the supervisor state, the SVC instruction is redundant; therefore, SVC interrupts are inhibited in the emulate mode. The SVC instruction is utilized instead to allow or disallow main storage accesses in the emulate mode. Bit 8 set to 1 in a decoded SVC enables *main storage* accesses for operands (not for instructions); bit 8 set to 0 resets the function to allow only *storage extension* accesses.

In emulate mode, SVC interrupts are inhibited; machine check, external, and I/O interrupts are held pending until emulation is complete; and program interrupts are handled according to the type.

To prevent overwriting the old PSW in storage extension that records the exit point of the problem program, any program interruptions taken while in emulate mode result in the new PSW being taken from location 78(hex) and the old PSW being stored in location 38(hex).

As noted in *IBM System/360 Principles of Operation*, Form A22-6821, when the timer is to be used as a real-time clock, the move instruction (MVC) may be used to read the current timer value and to set a new timer value without danger of timer updating occurring between the two operations. Because the Model 44 has no MVC instruction, successive load and store instructions must be used, and nothing can prevent a "creep" in the real-time clock. The "creep" could amount to 13 microseconds each time the timer value is changed.

Although the MVC instruction is emulated with the commercial feature, load and store instructions should still be used, because updating of the timer can occur between the machine instructions that move individual bytes.

Instructions related to System/360 RPQ's or special features, such as the direct control feature, are not emulated. No attempt is made to inhibit Model 44 special feature instructions, such as write direct word or read direct word; these instructions are executed when the feature is present, although they are categorized as System/360 invalid.

Storage Extension Allocations

Figure 5 shows the storage extension locations used during normal operation of the CPU, depending on the model number and the corresponding size of main storage.

Storage Address Assignments in Storage Extension

ADDRESS (DEC)	ADDRESS (HEX)	ASSIGNMENT
0	0	IPL PSW
8	8	IPL CCW 1
16	10	IPL CCW 2
24	18	External OPSW
32	20	SVC OPSW
40	28	Program OPSW
48	30	Machine OPSW
56	38	I/O OPSW
64	40	CSW
72	48	CAW
76	4C	Unassigned
80	50	Timer
84	54	Unassigned
88	58	External NPSW
96	60	SVC NPSW

Figure 13: IBM 360/44 Functional Characteristics, Page 12

Storage Extension Location		Model F	Model G	Model H
Hexadecimal	Decimal			
0 - 11F	0 - 287	Reserved	Reserved	Reserved
120 - 7FF	288 - 2047	1,760 Bytes	1,760 Bytes	1,760 Bytes
8,000 - 83FF	32,768 - 33,791	1,024 Bytes		
8,400 - 87FF	33,792 - 34,815	64 Multiplex UCWs	2,048 Bytes	2,048 Bytes
10,000 - 107FF	65,536 - 67,583		2,048 Bytes	2,048 Bytes
18,000 - 183FF	98,304 - 99,427		1,024 Bytes	
18,400 - 187FF	99,428 - 101,351		64 Multiplex UCWs	2,048 Bytes
20,000 - 207FF	131,072 - 133,119	Not Available		2,048 Bytes
28,000 - 287FF	163,840 - 165,887			2,048 Bytes
30,000 - 307FF	196,608 - 198,655		Not Available	2,048 Bytes
38,000 - 383FF	229,376 - 230,399			1,024 Bytes
38,400 - 387FF	230,400 - 231,423			64 Multiplex MCWs

● Figure 5. Storage Extension Allocations

ADDRESS (DEC)	ADDRESS (HEX)	ASSIGNMENT
104	68	Program NPSW
112	70	Machine NPSW
120	78	I/O NPSW
128	80	GR0
132	84	GR1
136	88	GR2
140	8C	GR3
144	90	GR4
148	94	GR5
152	98	GR6
156	9C	GR7
160	A0	GR8
164	A4	GR9
168	A8	GR10
172	AC	GR11
176	B0	GR12
180	B4	GR13
184	B8	GR14
188	BC	GR15
192-255	C0-FF	64 Bytes
256	100	FR0
260	104	
264	108	FR2
268	10C	
272	110	FR4
276	114	
280	118	FR6
284	11C	
288 to 2047	120 to 7FF	1,760 Bytes
2048 to 32,767	800 to 7FFF	
32,768 to 33,791	8000 to 83FF	1,024 Bytes
33,792	8400	MPX UCW
33,804	840C	
33,808	8410	MPX UCW
33,812	841C	
33,824 to 34,800	8420 to 87F0	MPX UCW
34,812	87FC	
34,816 to 65,535	8800 to FFFF	
65,536	10000	Invalid on Model F
131,072	20000	Invalid on Model G

Standard Supporting Equipment

Console Printer-Keyboard

The console printer-keyboard (Figure 4) permits communication between the operator and the system. Facilities are provided for interrupting the processing unit and for signalling the end of a data transmission.

The printer-keyboard has a stationary carriage and a replaceable, interchangeable printing sphere. Its typewriter-style keyboard and the printing function can be used independently: the keyboard for system input and the printer for computer output. The font of each printing sphere is specified by the customer.

The functions and operations of the console printer-keyboard are the same as those described for the IBM 1052 Printer-Keyboard Model 7 in *IBM System/360 System Summary*, Form A22-6810. Operating procedures and details are the same as those in *IBM 1052 Printer-Keyboard Model 7 with IBM 2150 Console*, Form A22-6877.

The console printer-keyboard is attached to one of the system channels via an adapter which is physically located within the CPU as a standard feature. The installation of the console printer-keyboard is also standard and takes up either one control-unit position and one subchannel of a multiplexer channel or one control-unit position and half a subchannel on a high-speed multiplexer channel.

Single-Disk Storage Drive

The single-disk storage drive provides direct access auxiliary storage for a minimum of 1,171,200 bytes on

Figure 14: IBM 360/44 Functional Characteristics, Page 13

a single disk permanently enclosed in an IBM 2315 Disk Cartridge and housed within the CPU, with side access for replacement of cartridges (Figure 6.) Each cartridge must be purchased separately, but the drive is a standard feature of Model 44.

The data rate of the disk storage is 90,000 bytes per second, necessitating operation in burst mode. Average time to seek a track is 70 milliseconds; the subsequent rotational delay to a particular record ranges from 0 to 40 milliseconds and averages 20 milliseconds.

Information is written on or read from the disk by a pair of magnetic read/write heads, one head for each surface. The disk is organized in 200 cylinders and three spare cylinders; a cylinder consists of a pair of tracks, one track per disk surface. Each cylinder contains 16 sectors (eight per track and surface). Each sector has a fixed length of 366 bytes. The three spare cylinders ensure that the stated capacities are maintained for the life of the cartridge. The read/write heads move, under a single seek command, directly to the track addressed. Error detection is accomplished on reading data from the disk.

No programming compatibility exists between the single-disk storage drive and disk storage drives controlled through the IBM 2841 Storage Control.

Figure 6. Removing an IBM 2315 Disk Cartridge from a Single-Disk Storage Drive

Figure 15: IBM 360/44 Functional Characteristics, Page 14

The drive is attached to one of the system channels only via an adapter, which is also installed in the CPU as a standard feature. A second drive may be installed in the CPU, as a special feature, to double the storage capacity. The two drives use the same shared-path adapter and operate on one shared subchannel, requiring one control-unit position on either a multiplexer or a high-speed multiplexer channel. Seek overlap is permissible when both drives are installed.

Commands

Control Seek — 00001011: One byte is transferred to the adapter. The byte contains the required cylinder address (0 through 202). The channel is free after the transfer of this byte, and the drive is free at the end of the seek.

Read Data — HSSS1010: Reading begins with the head for track H, sector SSS, and continues to the end of the track. If SSS=0, the entire track of 2,928 bytes is read. If the CCW count goes to zero at the end of sector 7 (end of track) or before the end of any other sector, the drive is free at the end of the sector being read. If the CCW count goes to zero at the last byte of a sector 0-6, however, the device end is delayed until the end of the following sector.

Write Data — HSSS1001: Writing begins at track H, sector SSS, and continues to the end of the track. If the CCW count goes to zero before the end of the track, the remainder of the sector being written is filled with zeros by the adapter and the drive is then free.

Other Commands: The adapter also recognizes read IPL (00000010), control no-op (00000011), and sense commands (00000100).

Programming Notes

The formal record length of the single-disk storage drive is 2,928 bytes (one full track); for all correct but shorter records, "incorrect length" is a normal indication. The CCW for a read or write command must therefore contain the SLI flag (suppress-length-indication, bit 34) unless the operation is to end with the 366th byte of the eighth sector.

Command chaining to the next sector may take place at a sector boundary without rotational delay unless a read operation ends with the 366th byte of sectors 0-6.

Keys and Lights

All keys and lights for the proper operation of each drive are on the lower left portion of the system control panel and are described under "Operator Control Section."

Instructions

The Model 44 executes the following instructions:

	MNEMONICS			
INSTRUCTION	RR FORMAT	RX FORMAT	RS FORMAT	SI FORMAT
Add	AR	A	———	———
Add Halfword	———	AH	———	———
Add Logical	ALR	AL	———	———
AND	NR	N	———	NI
Branch and Link	BALR	BAL	———	———
Branch on Condition	BCR	BC	———	———
Branch on Count	BCTR	BCT	———	———
Compare	CR	C	———	———
Compare Halfword	———	CH	———	———
Compare Logical	CLR	CL	———	CLI
Divide	DR	D	———	———
Exclusive OR	XR	X	———	XI
Halt I/O	———	———	———	HIO
Insert Character	———	IC	———	———
Load	LR	L	———	———
Load Address	———	LA	———	———
Load and Test	LTR	———	———	———
Load Complement	LCR	———	———	———
Load Halfword	———	LH	———	———
Load Negative	LNR	———	———	———
Load Positive	LPR	———	———	———
Load PSW	———	———	———	LPSW
Move	———	———	———	MVI
Multiply	MR	M	———	———
Multiply Halfword	———	MH	———	———
OR	OR	O	———	OI
Set Program Mask	SPM	———	———	———
Set System Mask	———	———	———	SSM
Shift Left Double	———	———	SLDA	———
Shift Left Double Logical	———	———	SLDL	———
Shift Left Single	———	———	SLA	———
Shift Left Single Logical	———	———	SLL	———
Shift Right Double	———	———	SRDA	———
Shift Right Double Logical	———	———	SRDL	———
Shift Right Single	———	———	SRA	———
Shift Right Single Logical	———	———	SRL	———
Start I/O	———	———	———	SIO
Store	———	ST	———	———
Store Character	———	STC	———	———
Store Halfword	———	STH	———	———
Subtract	SR	S	———	———
Subtract Halfword	———	SH	———	———
Subtract Logical	SLR	SL	———	———
Supervisor Call	SVC	———	———	———
Test and Set	———	———	———	TS
Test Channel	———	———	———	TCH
Test I/O	———	———	———	TIO
Test Under Mask	———	———	———	TM

An optional feature provides the full complement of floating-point instructions for both long and short operands and the RR and RX formats:

	MNEMONICS			
	RR FORMAT		RX FORMAT	
INSTRUCTION	LONG	SHORT	LONG	SHORT
Add Normalized	ADR	AER	AD	AE
Add Unnormalized	AWR	AUR	AW	AU
Compare	CDR	CER	CD	CE
Divide	DDR	DER	DD	DE
Halve	HDR	HER	———	———
Load	LDR	LER	LD	LE
Load and Test	LTDR	LTER	———	———
Load Complement	LCDR	LCER	———	———
Load Negative	LNDR	LNER	———	———

Figure 16: IBM 360/44 Functional Characteristics, Page 15

INSTRUCTION	MNEMONICS RR FORMAT	RX FORMAT	RS FORMAT	SI FORMAT
Load Positive	LPDR	LPER	——	——
Multiply	MDR	MER	MD	ME
Store	——	——	STD	STE
Subtract Normalized	SDR	SER	SD	SE
Subtract Unnormalized	SWR	SUR	SW	SU

As already described under "Protection Feature," two more instructions are added when that special feature is installed:

INSTRUCTION	FORMAT	MNEMONICS
Set Storage Key	RR	SSK
Insert Storage Key	RR	ISK

A full description of each instruction (except for execution time) is in the *IBM System/360 Principles of Operation*, Form A22-6821. Full timing formulas, and bases for determining the average times given in Figures 8 and 9, are described in this manual under "Instruction Timing Formulas."

Variable Long-Precision Floating Point

Some floating-point problems need more than short precision but do not require the 56 bits of long precision. With the variable long-precision floating-point feature, the user can adjust long-precision instructions for execution with 32, 40, 48, or the full 56 bits of precision. The adjustment for variable long-precision floating point is made at program execution time by setting a rotary switch on the system control panel to one of four positions (Figure 7). Only the floating-point long-precision multiply and divide operations are affected by the setting of the switch.

SWITCH SETTING (NO. OF HEXADECIMAL DIGITS IN FRACTION)	LONG PRECISION (FRACTION LENGTH IN BITS)
14	56
12	48
10	40
8	32

For maximum speed, the switch is set to 8; for maximum precision, it is set to 14. Setting the switch to 14 maintains complete compatibility with other System/360 models using long-precision floating point. At settings 8, 10, or 12, the operands of the long multiply instructions are pre-normalized and then truncated, as shown in Figure 7. A full 56-bit product is developed from these operands. The product is identical to that which would be obtained at 14-digit precision, using the operands after truncation. At settings 8, 10, or 12, the normalized quotient fraction of the long divide instruction is truncated (see Figure 7). At settings 10 or 12, the full operand fractions participate in the divide, and consequently, those digits of the quotient which are not truncated are identical to the corresponding digits of the quotient (which would be obtained by using 14-digit precision). At 8-digit precision however, the divisor is truncated to 8 digits (after pre-normalization) as well as the quotient.

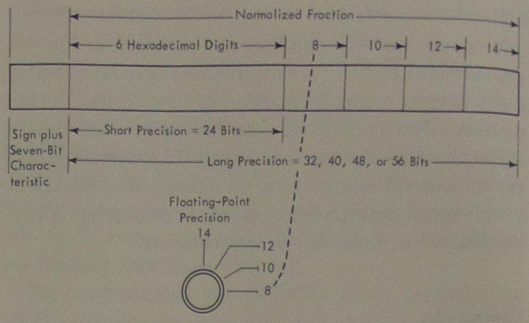

Figure 7. Variation of Fraction Length in Long Precision

Indexing Time

All Model 44 instruction timings (Figures 8 and 9) include the 1-microsecond I time and, for instructions that reference storage, the time to perform single indexing by one general register as referenced in the instruction (i.e., B ≠ 0).

For instructions in which double indexing is possible (i.e., all RX format instructions) the time required for the second indexing is 1 microsecond on the basic Model 44, or 0.75 microsecond when the high-speed general registers feature is installed. The times shown for the eight shift instructions assume no indexing (i.e., B = 0). For special timing calculations, the following adjustments may be made:

	BASIC MODEL 44	WITH HIGH-SPEED GENERAL REGISTERS
INSTRUCTION FETCH (included in all timings):	1.00	1.00
FIRST INDEXING (excluded for shift instructions):	1.00	0.25
SECOND INDEXING (excluded from all timings):	1.00	0.75

Figure 17: IBM 360/44 Functional Characteristics, Page 16

Instruction	Format	Mnemonic	Average Time in Microseconds**			
			Basic Model 44		Model 44 with High-Speed General Registers Feature	
Add	RR	AR	3.75		1.75	
Add	RX	A	4.75		2.25	
Add Halfword	RX	AH	4.75		2.25	
Add Logical	RR	ALR	3.75		1.75	
Add Logical	RX	AL	4.75		2.25	
AND	RR	NR	3.75		1.75	
AND	RX	N	4.75		2.25	
AND	SI	NI	3.75		3.00	
Branch and Link	RR	BALR	3.25		2.25	
Branch and Link	RX	BAL	3.25		2.50	
Branch on Condition	RR	BCR	BR 2.50 No BR 1.00		1.75 1.00	
Branch on Condition	RX	BC	BR 2.75 No BR 2.00		2.00 1.25	
Branch on Count	RR	BCTR	3.75		2.50	
Branch on Count	RX	BCT	3.75		2.75	
Compare	RR	CR	3.00		1.75	
Compare	RX	C	4.00		2.25	
Compare Halfword	RX	CH	4.00		2.25	
Compare Logical	RR	CLR	3.00		1.75	
Compare Logical	RX	CL	4.00		2.25	
Compare Logical	SI	CLI	3.25		2.50	
Divide	RR	DR	31.75		28.75	
Divide	RX	D	32.75		29.00	
Exclusive OR	RR	XR	3.75		1.75	
Exclusive OR	RX	X	4.75		2.25	
Exclusive OR	SI	XI	3.75		3.00	
Halt I/O	SI	HIO	3.00 - 35.00		2.25 - 35.00	
Insert Character	RX	IC	4.00		2.50 EA, 2.25 OA	
*Insert Storage Key	RR	ISK	3.50		2.00	
Load	RR	LR	3.00		1.00	
Load	RX	L	4.00		2.25	
Load Address	RX	LA	3.00		1.25	
Load and Test	RR	LTR	3.00		1.00	
Load Complement	RR	LCR	3.00		1.75	
Load Halfword	RX	LH	4.00		2.25	
Load Negative	RR	LNR	3.00		1.75	
Load Positive	RR	LPR	3.00		1.75	
Load PSW	SI	LPSW	4.50		3.75	
Move	SI	MVI	3.75		3.00	
Multiply	RR	MR	18.39		16.14	
Multiply	RX	M	19.39		16.89	
Multiply Halfword	RX	MH	12.72		10.72	
OR	RR	OR	3.75		1.75	
OR	RX	O	4.75		2.25	
OR	SI	OI	3.75		3.00	
Set Program Mask	RR	SPM	2.00		1.50	
*Set Storage Key	RR	SSK	3.00		2.00	
Set System Mask	SI	SSM	3.50 EA,4.00 OA		2.75 EA,3.00 OA	
			$S \leq 3$	$S > 3$	$S \leq 1$	$S > 1$
Shift Left Double	RS	SLDA	5.50	5.50 + 0.25 (S-3)	3.00	3.00 + 0.25 (S-1)
Shift Left Double Logical	RS	SLDL	5.50	5.50 + 0.25 (S-3)	3.00	3.00 + 0.25 (S-1)
Shift Left Single	RS	SLA	3.50	3.50 + 0.25 (S-3)	2.25	2.25 + 0.25 (S-1)
Shift Left Single Logical	RS	SLL	3.50	3.50 + 0.25 (S-3)	2.25	2.25 + 0.25 (S-1)
Shift Right Double	RS	SRDA	5.50	5.50 + 0.25 (S-3)	3.00	3.00 + 0.25 (S-1)
Shift Right Double Logical	RS	SRDL	5.50	5.50 + 0.25 (S-3)	3.00	3.00 + 0.25 (S-1)
Shift Right Single	RS	SRA	3.50	3.50 + 0.25 (S-3)	2.25	2.25 + 0.25 (S-1)
Shift Right Single Logical	RS	SRL	3.50	3.50 + 0.25 (S-3)	2.25	2.25 + 0.25 (S-1)
			For single indexing of shift instructions, Add 1.00		For single indexing of shift instructions, Add 0.25	
Start I/O	SI	SIO	3.00 - 40.00		2.25 - 40.00	
Store	RX	ST	4.25		2.50	
Store Character	RX	STC	4.75 EA,4.25 OA		3.00 EA,2.50 OA	
Store Halfword	RX	STH	4.25		2.50	
Subtract	RR	SR	3.75		1.75	
Subtract	RX	S	4.75		2.25	
Subtract Halfword	RX	SH	4.75		2.25	
Subtract Logical	RR	SLR	3.75		1.75	
Subtract Logical	RX	SL	4.75		2.25	
Supervisor Call	RR	SVC	1.00		1.00	
Test and Set	SI	TS	3.50		2.75	
Test Channel	SI	TCH	4.00 - 20.00		3.25 - 20.00	
Test I/O	SI	TIO	3.00 - 38.00		2.25 - 38.00	
Test Under Mask	SI	TM	3.00 EA,3.25 OA		2.25 EA,2.50 OA	
			For double indexing of RX format instructions, add	1.00		0.75

NOTES: EA = Even Address
OA = Odd Address
S = Number of bits shifted
*Instruction added with protection feature
**All times except those for the eight shift instructions include single indexing; see "Indexing Time."

Figure 8. Execution Time for Standard Instructions and Protection-Feature Instructions

Figure 18: IBM 360/44 Functional Characteristics, Page 17

Instruction	Format	Mnemonic	Average Time in Microseconds *	
			Basic Model 44	Model 44 with High-Speed General Registers Feature
Add Normalized (Long)	RR	ADR	6.28	6.28
Add Normalized (Long)	RX	AD	8.28	7.53
Add Normalized (Short)	RR	AER	3.81	3.81
Add Normalized (Short)	RX	AE	5.31	4.56
Add Unnormalized (Long)	RR	AWR	6.25	6.25
Add Unnormalized (Long)	RX	AW	8.25	7.50
Add Unnormalized (Short)	RR	AUR	3.79	3.79
Add Unnormalized (Short)	RX	AU	5.29	4.54
Compare (Long)	RR	CDR	5.84	5.84
Compare (Long)	RX	CD	7.84	7.09
Compare (Short)	RR	CER	3.50	3.50
Compare (Short)	RX	CE	5.00	4.25
Divide (Long)				
Precision 14	RR	DDR	124.00	124.00
Precision 12	RR	DDR	108.50	108.50
Precision 10	RR	DDR	93.00	93.00
Precision 8	RR	DDR	32.75	32.75
Divide (Long)				
Precision 14	RX	DD	126.00	125.25
Precision 12	RX	DD	110.50	109.75
Precision 10	RX	DD	95.00	94.25
Precision 8	RX	DD	34.75	34.00
Divide (Short)	RR	DER	23.25	23.25
Divide (Short)	RX	DE	24.75	24.00
Halve (Long)	RR	HDR	3.75	3.75
Halve (Short)	RR	HER	2.00	2.00
Load (Long)	RR	LDR	3.00	3.00
Load (Long)	RX	LD	5.00	4.25
Load (Short)	RR	LER	1.00	1.00
Load (Short)	RX	LE	3.00	2.25
Load and Test (Long)	RR	LTDR	3.00	3.00
Load and Test (Short)	RR	LTER	1.00	1.00
Load Complement (Long)	RR	LCDR	3.00	3.00
Load Complement (Short)	RR	LCER	1.00	1.00
Load Negative (Long)	RR	LNDR	3.00	3.00
Load Negative (Short)	RR	LNER	1.00	1.00
Load Positive (Long)	RR	LPDR	3.00	3.00
Load Positive (Short)	RR	LPER	1.00	1.00
Multiply (Long)				
Precision 14	RR	MDR	61.39	61.39
Precision 12	RR	MDR	52.72	52.72
Precision 10	RR	MDR	44.06	44.06
Precision 8	RR	MDR	21.14	21.14
Multiply (Long)				
Precision 14	RX	MD	63.39	62.64
Precision 12	RX	MD	54.72	53.97
Precision 10	RX	MD	46.06	45.31
Precision 8	RX	MD	23.14	22.39
Multiply (Short)	RR	MER	14.06	14.06
Multiply (Short)	RX	ME	15.56	14.81
Store (Long)	RX	STD	5.25	4.50
Store (Short)	RX	STE	3.25	2.50
Subtract Normalized (Long)	RR	SDR	6.28	6.28
Subtract Normalized (Long)	RX	SD	8.28	7.53
Subtract Normalized (Short)	RR	SER	3.81	3.81
Subtract Normalized (Short)	RX	SE	5.31	4.56
Subtract Unnormalized (Long)	RR	SWR	6.25	6.25
Subtract Unnormalized (Long)	RX	SW	8.25	7.50
Subtract Unnormalized (Short)	RR	SUR	3.79	3.79
Subtract Unnormalized (Short)	RX	SU	5.29	4.54
For double indexing of RX format instructions, add			1.00	0.75

*All times include single indexing; see "Indexing Time."

Figure 9. Execution Time for Floating-Point Instructions

Figure 19: IBM 360/44 Functional Characteristics Page 18

• Relationship of Model 44 to Other Models of IBM System/360

Model-Dependent Functions

The compatibility rule of System/360 does not apply to a number of detail functions for which neither the frequency of occurrence nor usefulness of results warrants identical action on all models. These functions are concerned with the handling of invalid programs and machine malfunctions and are explicitly identified in *System/360 Principles of Operation*, Form A22-6821, in the section "Functions that May Differ Among Models." Whenever model dependency exists, the definition of System/360 allows choice in implementation or specifies that the operation is unpredictable. The intent is that the user should ignore results that are defined to be unpredictable and should not base his program on any function where choice in implementation is permitted.

Considering any particular installation and operation, the operation normally is not truly unpredictable; the action may depend on the particular system components or on the input data. The purpose of this section is to describe how some of the model-dependent functions are performed on the Model 44.

It should be noted, however, that writing a program on the basis of information contained in this section is in violation of the rules of compatibility of System/360. If a program depends on a function that is model-dependent, it may not run on another model of System/360. Even if the program takes into account the model-dependent operation of all other models of System/360, difficulties may be encountered if and when new models of System/360 are introduced. Furthermore, a mandatory engineering change may in some instances require a change in the execution of a model-dependent function in a machine installed in a customer's office, and therefore may require changes in a program making use of such model-dependent information.

Machine Check Interruption

1. No storage area is required for diagnostic log-out. Instead, an interruption code is generated in the old PSW. The following bits are used:

Bit 16 = 0	Internal machine check (CPU affected)
= 1	External machine check (CPU not affected)
Bit 21 = 1	Channel 0 affected
Bit 22 = 1	Channel 1 affected
Bit 23 = 1	Channel 2 affected
Bit 27 = 1	Control sequence error
Bit 28 = 1	Storage parity error

NOTE: For a channel interface control check, bits 27, 28 = 00

A channel-detected error during data transfer or chaining only affects that channel, but nevertheless causes a machine check interruption. An error detected during an I/O instruction or an I/O interruption affects both the channel and the CPU. Other errors normally affect only the CPU.

2. Machine check interruptions can occur only when the mask bit in the current PSW is 1. When the CPU is affected, the current instruction is terminated and the interruption takes place immediately. When the CPU is not affected, the interruption is delayed until the end of the current instruction. Any affected channels cease interface activity at once, and are subjected to a general reset when the interruption takes place, which may be some time after detection of the error, if the CPU is not affected.

3. If machine check interruptions are disabled (mask bit 0), they are held pending. Operation of CPU and channels continues, but may be with or without error or the CPU or channels may hang up.

Normal Channel Operation

Channel 1 (if used) is a high-speed multiplexer channel. Channel 2 (if used) is either a HSMPX or a direct data channel. If only 1 or 2 HSMPX channels are installed, and the commercial feature is fitted, they will all operate as selector channels, under switch control. (See "Channels" for a description of their operations.)

Instruction Execution

1. The following direct control feature instructions are not available on Model 44; if used, they cause an operation exception (instruction length code 1):

RDD, WRD

Do *not* confuse these instructions with RDDW, WRDW (direct word feature).

2. The following instructions are available only as part of the commercial feature (see "Commercial Feature"), and cause an operation exception (instruction length code 1), if that feature is not installed:

CVB, CVD
EX
LM, STM
BXH, BXLE
All SS-format instructions

3. Long-precision floating point results may differ from those obtained on other models, depending on the setting of a switch. See "Variable Long-Precision Floating Point."

4. The following instructions are valid and do not cause an instruction length code 1 operation exception when the corresponding feature is installed:

FEATURE	INSTRUCTION
Priority Interrupt	CHPM, LPSX
Direct Word	RDDW, WRDW

Figure 20: IBM 360/44 Functional Characteristics, Page 19

5. When the priority interrupt feature is installed:
   a. Bit 6 of the System Mask is used to enable and disable priority interruptions as a class.
   b. 512 bytes at location 2048 are used by PSW's.

Timer Functions

A line-frequency timer is provided as a standard feature. (A high-resolution timer is available as an optional feature.) See the Programming Note under "Timer." Because the move instruction is not available on Model 44, LOAD and STORE must be used to inspect and update the timer value. Load and store instructions should be used even when the commercial feature is installed.

As with a read direct (RDD) instruction on other models, a read direct word (RDDW) instruction can cause incomplete updating of the timer if the hold-in line is active for an excessive period. A similar update failure can occur when the direct data channel feature is installed if the data transmission time is of excessive duration when priority in is active.

Channel Equipment Errors

If a data parity error is detected, the operation continues, but command chaining is suppressed. A data check indication is given in the ending status. Parity is corrected on incoming data, but not on outgoing data. Channel 0 signals an interface control check if no data is received for 500 milliseconds after entering the burst mode state.

Other causes of interface control checks are:

1. Detection of a parity error on control information.
2. Multiple tag signals.
3. Addressed device responding with a different address.
4. Device appearing off-line during command chaining.
5. Device requesting service and presenting invalid address (channel 0).
6. Tag sequence longer than 50 microseconds (channels 1 and 2).

All channels signal channel control check for:

1. A sequence error when accessing storage.
2. A storage parity error on control information.

The effects of channel control and interface control checks are described under "Machine Check Interruption."

System Controls

The system controls are described in "System Control Functions." The Floating-Point Precision switch (see "Operator Intervention Controls") is unique to the Model 44.

Figure 21: IBM 360/44 Functional Characteristics, Page 20