AccessionIndex: TCD-SCSS-V.20160121.002 Accession Date: 21-Jan-2016 Accession By: Peter Canavan Object name: Programming the Z80 Vintage: c.1979 Synopsis: Rodnay Zaks, ISBN 0-89588-013-X, Sybex Inc, 2344 Sixth Street, Berkeley, California 94710.

Description:

Rodnay Zaks books (also see *Microprocessor Interfacing Techniques* elsewhere in this catalog) were popular guides for design engineers, students and enthusiasts in the late 1970s.

When introduced in Jul-1976 the Zilog Z80 was the most powerful 8-bit CPU on the market. Its internal circuitry was designed by the legendary Masatoshi Shima, while Federico Faggin designed the instruction set, a superset of that of the Intel i8080.

Programming the Z80 describes the Z80 CPU hardware, instruction set and address modes, and basic I/O techniques, then covers application examples, data structures and program development.

The instruction set is described in very great detail, so this book was an excellent reference for such details. It is also a good snapshot of the simplicity of a mid-to-late 1970s microprocessor, just before the evolution of increasingly complex 16/32/64-bit architectures.

Many thanks to Peter Canavan, Network Manager, Broadcast Operations, Australian Broadcasting Commission (ABC), who donated this item from his personal collection.

The homepage for this catalog is at: <u>https://www.scss.tcd.ie/SCSSTreasuresCatalog/</u> Click '*Accession Index*' (1st column listed) for related folder, or '*About*' for further guidance. Some of the items below may be more properly part of other categories of this catalog, but are listed here for convenience.

Accession Index	Object with Identification
TCD-SCSS-V.20160121.002	Rodnay Zaks, Programming the Z80, ISBN 0-89588-013-X, Sybex Inc, 2344 Sixth Street, Berkeley, California 94710, c.1979.



Figure 1: Programming the Z80 front cover

PROGRAMMING THE Z80

has been designed both as an educational text and as a self-contained reference book. As such, it can be used as a complete introductory book on programming, ranging from the basic concepts to advanced data structures manipulations.

It also contains a comprehensive description of all the Z80 instructions as well as its internal operation, and should provide a comprehensive reference for the reader who is already familiar with the principles of programming, but wishes to learn the Z80.

This book is the result of extensive experience by the author in the field of education and programming. As such, it has been designed to be clear and easy to read. All concepts are explained in simple yet precise terms, building progressively towards more complex techniques. The reader will gain not only an understanding of programming in the language of the Z80 but also a detailed understanding of the way a microprocessor such as the Z80 actually executes instructions. The reader will follow the flow of execution between the various registers and along the buses. This is indispensible for effective programming at machine level in the world of microprocessors. Because programming is not just the skill of coding an algorithm into a programming language but also the art of designing appropriate data structures, an extensive chapter on data structures is presented, which both introduces the concepts and actual application programs. The reader will find there lists, tables, binary trees, and the required algorithms.

After reading this book, the reader should have acquired all the basic skills required to program not just at the elementary level, but in most practical cases.

ABOUT THE AUTHOR

Dr. Rodnay Zaks has been involved with the industrial use of microprocessors since they first appeared. He is the author of a number of best-selling books on all aspects of microprocessors. He has taught microprocessor courses to more than 5,000 people internationally, ranging from the introductory level to bit-slice microprogramming techniques. He holds a Ph. D. in Computer Science from U.C. Berkeley, and is a member of ACM and IEEE.

NOTICE: "Z80" is a registered trademark of ZILOG Inc. SYBEX is not connected in any way to ZILOG Inc.

ISBN#0-89588-013-X

Figure 2: Programming the Z80 rear cover



Figure 3: Programming the Z80 title page

ACKNOWLEDGEMENTS

Designing a programming textbook is always difficult. Designing it so that it will teach elementary programming as well as advanced concepts while covering both hardware and software aspects makes it a challenge. The author would like to acknowledge here the many constructive suggestions for improvements or changes made by: O.M. Barlow, Dennis L.

Feick, Richard D. Reid, Stanley E. Erwin, Philip Hooper, Dennis B. Kitsz. A special acknowledgement is also due to Chris Williams for his contribution to the in-

struction-set and the data structures section. Any additional suggestions for improvements or changes should be sent to the author, and will be reflected in forthcoming editions.

Several tables in Chapter Four showing hexadecimal codes for the Z80 instructions have been reprinted by permission of Zilog Inc.

Cover Design by Daniel le Noury

Every effort has been made to supply complete and accurate information. However, Sybex assumes no responsibility for its use; nor any infringements of patents or other rights of third parties which would result. No license is granted by the equipment manufacturers under any patent or patent rights. Manufacturers reserve the right to change circuitry at any time without notice.

In particular, technical characteristics and prices are subject to rapid change. Comparisons and evaluations are presented for their educational value and for guidance principles. The reader is referred to the manufacturer's data for exact specification.

Copyright \odot 1979, SYBEX Inc. World Rights reserved. No part of this publication may be stored in retrieval system, transmitted, or reproduced in any way, including but not limited to, photocopy, photography, magnetic or other record, without the prior written permission of the publisher.

Library of Congress Card Number: 78-73741 ISBN Number: 0-89588-013-X Printed in the United States of America Printing 10 9 8 7 6 5 4 3 2 1

Figure 4: Programming the Z80 publishers page

TABLE OF CONTENTS

I.	BASIC CONCEPTS1
	Introduction, What is programming?, Flowcharting, Information Representatio
II.	Z80 HARDWARE ORGANIZATION4
	Introduction, System Architecture, Internal Organization of the Z80, In struction Formats, Execution of Instructions with the Z80, Hardware Summar
III.	BASIC PROGRAMMING TECHNIQUES9
	Introduction, Arithmetic Programs, BCD Arithmetic Multiplication, Binar Division, Instruction Summary, Subroutines, Summary
IV.	THE Z80 INSTRUCTION SET 15
	Introduction, Classes of Instructions, Summary, Individual Descriptions
V.	ADDRESSING TECHNIQUES
	Introduction, Possible Addressing Modes, Z80 Addressing modes, Using th Z80 Addressing Modes, Summary
VI.	INPUT/OUTPUT TECHNIQUES 460
	Introduction, Input/output, Parallel Word Transfer, Bit Serial Transfe Peripheral Summary, Input/Output Scheduling, Summary
VII.	INPUT/OUTPUT DEVICES 51
	Introduction, The Standard PIO, The Internal Control Register, Program ming a PIO, The Zilog Z80 PIO

Figure 5: Programming the Z80 table of contents page 1

~**	APPLICATION EXAMINE
VIII.	Introduction, Clearing a Section of Memory, Polling I/O Devices, Getting Introduction, Clearing A Character, Bracket Testing, Parity Generation, Code Characters In, Testing A Character, Bracket Testing, Parity Generation, Code Characters In, Testing A Character, Bracket Testing, Parity Generation, Code Characters In, Testing A Character, Bracket Testing, Parity Generation, Code Characters In, Testing A Character, Bracket Testing, Parity Generation, Code Characters In, Testing A Character, Bracket Testing, Parity Generation, Code Characters In, Testing A Character, Bracket Testing, Parity Generation, Code Characters In, Testing A Character, Bracket Testing, Parity Generation, Code Characters In, Testing A Character, Bracket Testing, Parity Generation, Code Conversion: ASCII to BCD, Convert Hex to ASCII, Finding the Largest Ele- Conversion: ASCII to BCD, Convert Hex to ASCII, Finding the Largest Ele- Conversion: ASCII to BCD, Convert Hex to ASCII, Finding the Largest Ele- Conversion: ASCII to BCD, Convert Hex to ASCII, Finding the Largest Ele- Conversion: ASCII to BCD, Convert Hex to ASCII, Finding the Largest Ele- Conversion: ASCII to BCD, Convert Hex to ASCII, Finding the Largest Ele- Conversion: ASCII to BCD, Convert Hex to ASCII, Finding the Largest Ele- Conversion: ASCII to BCD, Convert Hex to ASCII, Finding the Largest Ele- Conversion: ASCII to BCD, Convert Hex to ASCII, Finding the Largest Ele- Conversion: ASCII to BCD, Convert Hex to ASCII, Finding the Largest Ele- Conversion: ASCII to BCD, Convert Hex to ASCII, Finding the Largest Ele- Conversion: ASCII to BCD, Convert Hex to ASCII, Finding the Largest Ele- Conversion: ASCII to BCD, Convert Hex to ASCII, Finding the Largest Ele- Conversion: ASCII to BCD, Convert Hex to ASCII, Finding the Largest Ele- Conversion: ASCII to BCD, Conversion: ASCII to BCD
IX.	DATA STRUCTURES 539
	PART 1—THEORY Introduction, Pointers, Lists, Searching and Sorting, Section Summary PART 2—DESIGN EXAMPLES Introduction, Data Representation for the List, A Simple List, Alphabetic Set, Linked List, Summary
x.	PROGRAM DEVELOPMENT 579
	Introduction, Basic Programming Choices, Software Support, The Program Development Sequence, Hardware Alternatives, The Assembler, Conditional Assembly, Summary
XI.	CONCLUSION
	Technological Development, The Next Step
APP	ENDIX A
APP	ASCII Conversion Table
APP	ENDIX C
API	Decimal to BCD Conversion PENDIX E
AP	PENDIX F
AP	280 to 8080 Equivalence PENDIX G
INI	DEX

Figure 6: Programming the Z80 table of contents page 2

LIST OF ILLUSTRATIONS

Figure	1.1:	A Flowchart for Keeping Room Temperature Constant
Figure	1.2:	Decimal-Binary Table
Figure	1.3:	2's Complement Table
Figure	1.4:	BCD Table
Figure	1.5:	Typical Floating-Point Representation
Figure	1.6:	ASCII Conversion Table
Figure	1.7:	Octal Symbols
Figure	1.8:	Hexadecimal Codes
Figure	2.1:	Standard Z80 System
Figure	2.2:	"Standard" Microprocessor Architecture
Figure	2.3:	Shift and Rotate
Figure	2.4:	The 16-bit Address Registers Create the Address Bus
Figure	2.5:	The Two-Stack Manipulation Instructions
Figure	2.6:	Fetching an Instruction from the Memory
Figure	2.7:	Automatic Sequencing
Figure	2.8:	Single-Bus Architecture
Figure	2.9:	Execution of an Addition—R0 into ACC
Figure	2.10:	Addition—Second Register R1 into ALU
Figure	2.11:	Result Is Generated and Goes into R0
Figure	2.12:	The Critical Race Problem
Figure	2.13:	Two Buffers Are Required61
Figure	2.14:	Internal Z80 Organization65
Figure	2.15:	Typical Instruction Formats
Figure	2.16:	The Register Codes
Figure	2.17:	Instruction Fetch—(PC) Is Sent to the Memory
Figure	2.18:	PC Is Incremented
Figure	2.19:	The Instruction Arrives from the Memory into IR
Figure	2.20:	Transferring C into D
Figure	2.21:	The Contents of C Are Deposited INTO TMP
Figure	2.22:	The Contents of TMP Are Deposited into D
Figure	2.23:	Two Transfers Occur Simultaneously
Figure	2.24:	End of ADD r78
Figure	2.25:	Fetch-Execute Overlap during 11-12
Figure	2.26:	Intel Abbreviations
Figure	2.27:	Intel Instruction Formals
Figure	2.28:	Transfer Contents of HL to Address Bus
Figure	2.29:	LD A, (ADDRESS) Is a 5- word instruction
Figure	2.30:	Before Execution of LDA
Figure	2.31:	After Execution of LDA
Figure	2.32:	Second Byte of Instruction Goes into 211111
Buie	2.33:	Z80 MPO Pinout

Figure 7: Programming the Z80 list of illustrations page 1

Figure	3.0:	Fight-Bit Addition RES = OP1 + OP296
Figure	3.1:	LDA, (ADR1): OP1 is Loaded from Memory
Figure	3.2.	ADD A, (HL)
Figure	3.3:	LD (ADR3), A (Save Accumulation in Weinory)
Figure	3.4.	16-Bit Addition—The Operands
Figure	3.5.	Storing Operands in Reverse Order 102
Figure	3.0.	Pointing to the High Byte 103
rigure	3.8.	A 32-Bit Addition104
Figure	3.0.	16-Bit Load—LD HL, (ADR1)106
Figure	3.10.	Storing BCD Digits
Figure	3 11.	Packed BCD Subtract: NI+N2 - NI111
Figure	3.12.	The Basic Multiplication Algorithim—Flowchart114
Figure	3 13.	8 x 8 Multiplication Program115
Figure	3.15.	8 x 8 Multiplication—The Registers116
Figure	3.14.	1 D BC. (MPRAD)
Figure	3.16.	LD DE (MPDAD)
Figure	3.17.	Shift and Rotate
Figure	3.17.	Shifting from E into D
Figure	3 19.	Form for Multiplication Exercise
Figure	3.20.	Multiplication: After One Instruction
Figure	3 21.	Multiplication: After Two Instructions
Figure	3.21.	Multiplication: After Five Instructions
Figure	3 22.	One Pass Through The Loop
Figure	3 24.	Improved Multiply, Step 1
Figure	3 25.	Registers for Improved Multiply
Figure	3 26.	Improved Multiply Step 2
Figure	3 27.	16 x 16 Multiply—The Registers
Figure	3 28.	16 x 16 Multiplication Program
Figure	3.29.	16 x 16 Multiply with 32 Bit Result
Figure	3.30:	8-Bit Binary Division Flowchart
Figure	3.31.	16 x 8 Division—The Registers
Figure	3 32.	16 x 8 Division Program
Figure	3.33.	Form for Division Program
Figure	3.34.	Non-Restoring Divisor The D
Figure	3.35.	Subrouting Coll
Figure	3.36.	Nested Colle
Figure	3.37.	The Subroutine Call
Figure	3.38.	Stack vs. Time
Figure	3.39:	Multiplication A.C.
Figure	3.40:	The Multiplication: A Complete Trace
Figure	3.41:	Two Internet Two Internet
Figure	4.1:	Shift and Basis
Figure	4.2:	Fight Big Land Rotate
Figure	4.3:	16 Bit Load Group—'LD'
Figure	4.4:	Exchanges (Dut) - 'LD', 'PUSH' and 'POP'
Figure	4.5:	Block Transf
Figure	4.6:	Block Search G
Figure	4.7:	Eight-Bit Asia
		low on Arithmetic and Logic16

Figure 8: Programming the Z80 list of illustrations page 2

	10.	Sixteen Bit Arithmetic and Logia
Figure	4.8:	Shift and Rotate 170
Figure	4.9:	Potates and Shifts
Figure	4.10:	Nine Bit Pototion
Figure	4.11:	Fight Bit Potation
Figure	4.12:	Digit Potate Instructions
Figure	4.13:	Digit Kotate Instructions
Figure	4.14:	Bit Manipulation Oroup
Figure	4.15:	The Elece Desister
Figure	4.16:	The Flags Register
Figure	4.17:	Summary of Flag Operations
Figure	4.18:	Jump Instructions
Figure	4.19:	Restart Group
Figure	4.20:	Output Group186
Figure	4.21:	Input Group 186
Figure	4.22:	Miscellaneous CPU Control 187
Figure	5.1:	Basic Addressing Modes
Figure	5.2:	Addressing (Pre-Indexing)
Figure	5.3:	Indirect Indexed Addressing (Post-Indexing)
Figure	5.4:	Indirect Addressing
Figure	5.5:	Indexed Addressing Has 2-Byte Opcode
Figure	5.6:	Character Search Flowchart
Figure	5.7:	Block Transfer: Initializing the Register
Figure	5.8:	A Block Transfer-Memory Map453
Figure	5.9:	Adding Two Blocks: BLK1 = BLK1 + BLK2456
Figure	5.10:	Memory Organization for Block Transfer
Figure	6.1:	Turning on a Relay
Figure	6.2:	A Programmed Pulse
Figure	6.3:	Basic Delay Flowchart
Figure	6.4.	Parallel Word Transfer: The Memory
Figure	6.5:	Parallel Word Transfer: Flowchart
Figure	6.6.	Bit Serial Transfer-Flowchart
Figure	6.7:	Serial-to-Parallel: The Registers
Figure	6.8.	Handshaking (Output)
Figure	6.82	Handshaking (Input)
Figure	6.9.	Printer—Data Paths
Figure	6 10.	Seven Segment LED
Figure	6.11.	Hevadecimal Characters Generated with a Seven-Segment LED 481
Figure	6.12.	Format of a Teletype Word
Figure	6.12.	TTV Input with Echo
Figure	0.15:	Talatuna Brogram
Figure	0.14:	Teletype I rogram
Figure	0.15:	Teletype Input
Figure	0.16:	Deletipe output
rigure	6.17:	Printing a Melliol y Block
Figure	6.18:	Pulling Lear Flowchart 494
Figure	6.19:	Polling Loop Flowchart Tape Reader
Figure	6.20:	Reading from a Paper-Tape Reader
Figure	6.21:	Printing on a Punch of Printer
rigure	6.22:	Z80 Stack After Interruption
Figure	6.23:	Saving Some Working Registers
rigure	6.24:	Interrupt Sequence

Figure 9: Programming the Z80 list of illustrations page 3

		ematic Vectoring
		MI Forces Automatic
	6.25:	NMIT Mode 0
Figure	6.26:	Interior the Registers
Figure	6.27:	Saving the Interrupt
Figure	6.28:	Mode 2 Interrupt
Figure	6.29:	Mode 2 A Practical Example
Figure	6.30:	Mode 2. Vectored Interrupt
Figure	6.31:	Polled vs. Polled vs. May Use the Same Interrupts
Figure	6.32:	Several During Multiple Interrupts
Figure	6.33:	Stack Contenter
Figure	6.34:	Interrupt Logic
Figure	7.1:	Typical PIO -I oad Control Register
Figure	7.2:	Using a PIO Load Data Direction
Figure	7.3:	Using a PIO – Load Status
Figure	74:	Using a PIO-Keau Status The
Figure	7.5:	Using a PIO-Read INPOT
Figure	7.6:	Z80 PIO Pinout
Figure	7.7.	Z80 Block Diagram
Figure	8 1.	Largest Element in a Table
Figure	0.1.	Sum of N Elements
Figure	0.2.	BCD Block Transfer-the Memory
Figure	0.3.	Comparing Two Signed Numbers
Figure	8.4:	Pubble Sort Examples: Phases 1 to 12
Figure	8.5:	Bubble Sort Example: Phases 13 to 21
Figure	8.6:	Bubble-Soft Example: 1 hases 15 to 21
Figure	8.7:	
Figure	8.8:	Bubble-Sort
Figure	9.1:	An Indirection Pointer
Figure	9.2:	A Directory Structure
Figure	9.3:	A Linked List
Figure	9.4:	Inserting a New Block
Figure	9.5:	A Queue
Figure	9.6:	Round Robin is Circular List
Figure	9.7:	Genealogical Tree
Figure	9.8:	Doubly-Linked List
Figure	9.10:	Typical List Entries in the Memory
Figure	9.11:	The Simple List 550
Figure	9.12:	Table Search Flowshort
Figure	9.13:	Table Insertion Flore 1 557
rigure	9.14:	Deleting an Entry (G)
rigure	9.15:	Table Deletion III
rigure	9.16:	Simple Line Towchart
rigure	9.17:	Simple List- The Programs
Figure	9.18:	Binaru S. 550
Figure	9.19:	A Biner of Flowchart
Figure	9.20:	Insert (ip
Figure	9.21:	Delate up 563
Figure	9.22:	Delation BAC", 564
Figure	9.23:	Binan of Flowchart (Alphater 565
Figure	9.24:	Alphal
oule	9.25;	Linkola 569
		List Structure 571
		and the second s

Figure 10: Programming the Z80 list of illustrations page 4

Figure	9.26:	Linked List—A Search
Figure	9.27.	Example of Deletion (Linked List)
Figure	9.29:	Linked List-The Programs
Figure	9.30:	Linked List-A Sample Run 577
Figure	10.1:	Programming Levels
Figure	10.2:	A Typical Memory Map
Figure	10.3:	Microprocessor Programming Form
Figure	10.4:	Assembler Output-An Example
Figure	10.5:	Operator Precedence

Figure 11: Programming the Z80 list of illustrations page 5