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"This market, this industry, is poised for a fundamental transformation," Raj Hazra, Vice President and General Manager of Intel's High Performance Computing division, told a group at the company's SC14 briefing on their future investments in HPC.

The comment came as a counterpoint to the lack of news around stunning changes in the Top 500 list of supercomputers as well as the general sentiment at the show that HPC momentum had suddenly ground to a halt. While many recognize that this is a temporary standstill, including Hazra, who is seeing the industry on track to upend the current performance, efficiency, and code trends, the insight from the top chipmaker about what the future holds was welcome.

While many already may be aware that Intel finally let loose on some details around the upcoming Knights Landing chips, which are due in 2015 and are already set to be outfit on large-scale supercomputers including Trinity, Cori, and the newly announced KAUST machines, it's worth asking why these revelations are being made at this early stage. There are more of a wonder following their SC14 news of a the next-next generation Xeon Phi, codenamed Knights Hill.

"We're making a sustained, multi-generational investment in the Xeon Phi family," said Charles Wuischpard, General Manager of Workstations and HPC at Intel. "A lot of that has to do with the fact that we have customers like one who told us that they've put half a billion dollars into each of six codes over the last twenty years and are now planning to support many more architectures with the Knights family. That's a big responsibility and we want to make it clear this isn't a one-shot deal."

Wuischpard made it clear that it's essential for their customers to see clearly that the Knights family will be bestowed with many years of investment. "We're showing adoption and readiness for Knight's Landing," he explained. "So far over 50 system providers are signing on to design boards and chassis to incorporate it and we have over 100 petaflops customer commitment and more in the wings waiting on future procurements." He also noted that while most have been thinking of it as a socketed part (which will be binary compatible with current Xeons) there are use cases on the horizon that might benefit from having a card—something that will be around the corner at a different time than the official release.

As presented at ISC 14

Unveiling Details of Knights Landing

(Next Generation Intel® Xeon Phi™ Products)

- Platform Memory: DDR4 Bandwidth and Capacity Comparable to Intel® Xeon® Processors
- Compute: Energy-efficient IA cores²
 - Microarchitecture enhanced for HPC³
 - 3X Single Thread Performance vs. Knights Landing
 - Intel Xeon Processor Binary Compatible
- On-Package Memory:
 - up to 16GB at launch
 - 1/3X the Space⁴
 - 5X Bandwidth vs. DDR4⁷
 - 5X Power Efficiency⁸

Jointly Developed with Micron Technology

(http://6lli539m39y3hpkelqsm3c2fg.wpengine.netdna-cdn.com/wp-content/uploads/2014/11/FutureKL.png)

While Intel still hasn't dished on exactly how many cores will appear on the Knights Landing chips, stating only that there will be more than 60, it was revealed earlier in the week that the OmniPath fabric (formerly known as OmniScale) will be integrated on the nanometer part. The expectation is that it will hit 3 teraflops of peak double-precision capability. This is matched with the news we carried earlier last year about Intel's work with Micron to bring the Hybrid Memory Cube on board, pushing it close to the processor in a much smaller space than current generation Xeon Phis.

There is very little available about Knights Hill and how soon it will follow on the heels of Knights Landing, it is expected to follow a 10 nanometer trajectory, although Wuischpard says that there are various elements, not the least of which are the memory and interconnect pieces, that will determine the specs for the future architecture. So far, other than the expense (and some great speculation here) this is what we're left to work with. For Intel, however, it doesn't seem to be critical at this time to share details, but rather to show that as per usual, well before a new product rolls out to general availability, there are already teams at work developing its next generation. This takes us back to Wuischpard's point about showing high-value customers that all of their investments in code and future manycore architectures is placed well with Intel.

wire/nsa-releases-new-technology-open-source-community/) Gidel Unveils Proc10A (http://www.hpcwire.com/off-...)



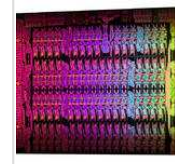
Along These Lines



Amazon Lead Highlights HPC Cloud Progress (http://www.hpcwire.com/2014/08/11/amazon-lead-highlights-hpc-cloud-progress/)



NERSC Launches Exascale Readiness Program with Intel, Cray (http://www.hpcwire.com/2014/08/11/nersc-intel-cray-prepare-manycore-transition/)



New Intel HPC Lead Tracks Phi Momentum (http://www.hpcwire.com/2014/06/20/top-intel-hpc-lead-tracks-phi-momentum/)



Top Session Picks for ISC14 (http://www.hpcwire.com/2014/06/20/top-session-picks-isc14/)

HPC Tweets

ANSYS, Inc. @ANSYS_Inc 49m
Startup's Wristband Can Track Seizures bit.ly/1zCBG7h
Show Summary

Mount Burnett Obsvry @MBObservatory 1h
Daniel Armstrong talking about "Art and Cosmos" showing Percival Lowell's drawings of canals on Mars. pic.twitter.com/Avj55W7FNC
Retweeted by Chris Samuel

Satoshi Matsuoka @ProfMatsuoka 1h
Alteraの売り上げは年間2500億程度

Feature Articles

A Rare Letter from the Editor (http://www.hpcwire.com/2014/11/27/rare-letter-editor/) In the five years I've been here, one would be hard



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Intel® Xeon Phi™ Product Family
Industry and User Momentum

Announcing

- Knights Corner**: 1 TFLOPS¹
- Knights Landing**: 3+ TFLOPS²
- Knights Hill**: 2H'15 First Commercial Systems

3rd Generation Intel® Xeon Phi™ Product Family
2nd Generation Intel Omni-Path Architecture
10nm process technology

>50 systems providers expected³
>100 PFLOPS customer system compute commits to-date⁴

(http://llis39m39y3hpkelqsm3c2fg.wpengine.netdna-cdn.com/wp-content/uploads/2014/11/FutureKnightsHill.png)

The critical part of these efforts will be on the code modernization and development front, which has been a sustained focus for Intel with its on-site work with customers who have custom proprietary codes, to large national labs and academic centers, including NERSC, which will need to get its codes primed for the eventual Knights Landing-based machine transition.

According to Hazra and his colleague, Charles Wuishpard, it's time to stop thinking of Intel in its chip box and recognize how they're taking a platform approach to the entire system. From their current investments at the Lustre, Omni Path fabric, and code modernization levels all the way up the systems chain, the pair were adamant that Intel is set to take a lead through continued integration and codesign in both hardware and software.

"In HPC we're not just a chip company," said Hazra. "If the data is computed on, if it's being moved, if it's being stored, we're engaged in it. This isn't just a business aspiration or model—it's the way scalable systems have to be designed... For balanced systems that are highly optimized and workload targeted, they must be designed at the system level and have interplay between the parts."

"We are looking at systems at multiple scales and looking for more efficient compute, more programmable efficient compute, and ease of deployment," noted Hazra. Of their current Knights family, he says while they've shared what is new in the roadmap generally, Intel's strategies are set and now they're executing along those lines with the expectations of feeding the ecosystems around the many layers of the next generation of HPC systems. We're confident about having made some bets in the manycore space a couple of years ago that's starting to pay off. It's a steady continuance of building and engagement to get the ecosystem up and running."

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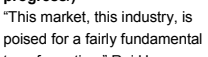
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pressed to find a letter from the editor, especially one that uses the dreaded personal Read more... (http://www.hpcwire.com/2014/11/24/intel-etches-future-process-hpc-progress/)

NASA Debuts Stunning CO2 Visualization (http://www.hpcwire.com/2014/11/25/nasa-debuts-stunning-co2-visualization/) In keeping with the SC spirit of HPC matters, we wanted to share another amazing example of supercomputing in action. Last week, NASA officials Read more... (http://www.hpcwire.com/2014/11/25/nasa-debuts-stunning-co2-visualization/)

Intel Etches Future Process for HPC Progress (http://www.hpcwire.com/2014/11/24/intel-etches-future-process-hpc-progress/) "This market, this industry, is poised for a fairly fundamental transformation," Raj Hazra, Vice President and General Manager of Intel's High Read more... (http://www.hpcwire.com/2014/11/24/intel-etches-future-process-hpc-progress/)

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Short Takes

Weekly Twitter Roundup (http://www.hpcwire.com/2014/11/24/weekly-twitter-roundup-16/) Here at HPCwire, we want to help keep the HPC community as up-to-date as possible on some of the most captivating news items that were Read more... (http://www.hpcwire.com/2014/11/26/weekly-twitter-roundup-16/)

UChicago Life Science Cluster Gets \$2M Makeover (http://www.hpcwire.com/2014/11/26/uchicago-life-science-cluster-gets-2m-makeover/)

Beagle, the Cray XE6 supercomputer that has served University of Chicago biology and medical researchers for the last three years, is about to Read more... (http://www.hpcwire.com/2014/11/26/uchicago-life-science-cluster-gets-2m-makeover/)

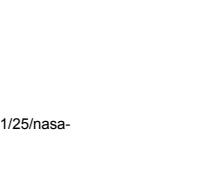
New Intelligence Test Asks What It Means to Be Human (http://www.hpcwire.com/2014/11/26/intelligence-test-asks-means-human/)

The primary definition of artificial intelligence (AI), specifically strong AI, is the power of a machine to exhibit intelligence Read more... (http://www.hpcwire.com/2014/11/26/intelligence-test-asks-means-human/)

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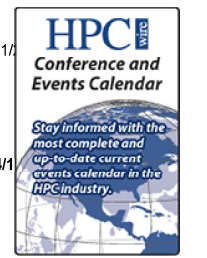


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South Africa