IMP-00A/520 MOS/LSI register and arithmetic logic unit (RALU)

general description

The IMP-00A/520 is a member of a new family of microprocessor elements, and is a monolithic MOS/LSI circuit utilizing standard P-channel, enhancement mode, silicon gate technology. It provides a 4-bit slice of the register and arithmetic portion of a general purpose controller/processor. RALU's may be stacked in parallel for longer word lengths. The RALU is designed to be used with other members of National's IMP family (in particular the CROM) to form a complete processor. Each RALU provides 96 bits of storage in the form of 4 bits in each of 7 general registers, a status register and a 16-word last in, first out (LIFO) stack. The arithmetic and logic unit performs ADD, AND, OR and exclusive OR operations on true and complemented data from the registers at nearly 10^6 operations per second. A shifter is provided for single bit left or right shifts and an I/O data multiplexer for communication with an external data bus. Control is provided over a 4-bit, time multiplexed command bus.

The RALU operates on +5V and −12V supplies with 4-phase, non-overlapping clocks. Signals which are intended for interface with the MM5751 CROM are MOS level, while those which are intended for interface with the rest of the processor system are TTL levels.

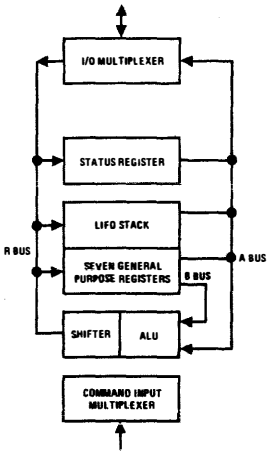
features

■ 4-bit slice of register and arithmetic logic block	Expandable to 32-bit word
■ Arithmetic and logic operations	ADD, AND, OR, Exclusive OR
■ 7 general purpose registers	Functions not pre-assigned
■ 4-bit status register	Overflow, Link, Carry, general flag
■ 16 word stack	Last in, first out
■ Multiplexed I/O data bus	4-bit, bipolar compatible
■ Multiplexed command bus	4-bit MOS levels
■ High speed operation	~ 700 kHz
■ Standard supplies	+5V, −12V
■ Bipolar compatibility	Drives TTL
■ 4-phase clock	Non-overlapping
■ Standard package	24-pin DIP

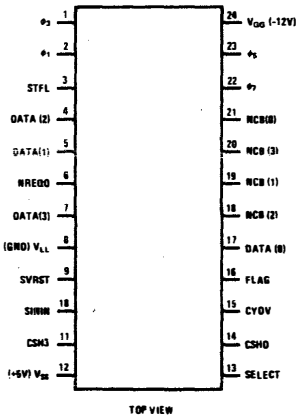
applications

- General purpose processor
- Distributed and multiprocessors
- Process controllers
- Machine tool controllers
- Small business machines
- Terminal controllers
- Test system and instrument control
- Traffic controller

block and connection diagrams



Dual-In-Line Package



absolute maximum ratings

All Input or Output Voltages With Respect to Most Positive Supply Voltage V_{SS}	+0.3V to −20V
Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation	1W Maximum at +25°C

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

dc electrical characteristics

(T_A = 0°C to +70°C, V_{SS} = +5V ±5%, V_{GG} = −12V ±5%, V_{LL} = GND)

PARAMETER	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNITS
Logic "1" Input (MOS and TTL) ($V_{IN(1)}$) (Note 1)		V_{SS} − 0.8			V
Logic "0" Input (MOS) ($V_{IN(0)}$)				V_{SS} − 7.0	V
Logic "0" Input (TTL) ($V_{IN(0)}$)				V_{SS} − 4.2	V
Logic "0" Input Current (TTL) ($I_{IN(0)}$)	V_{IN} = 0V			−1.75	mA
Input Leakage Current (MOS) (I_L)	V_{IN} = +5.0V to −12V			2	μA
Logic "1" Output (MOS) ($V_{OUT(1)}$)		V_{SS} − 0.7			V
Logic "0" Output (MOS) ($V_{OUT(0)}$)		V_{SS} − 8.0			V
Logic "1" Output (TTL) ($V_{OUT(1)}$)	I_{OUT} = 0.2 mA	2.4			V
Logic "0" Output (TTL) ($V_{OUT(0)}$)	I_{OUT} = −1.6 mA			0.4	V
Pull-up Transistor "on" Resistance ($P_{PULL-UP}$)(Note 1)	V_{IN} = V_{SS} − 1.0V	3.0		5.0	kΩ
Signal Line Input Capacitance (C_S) for SELECT, SVRST, SININ, DATA (0), (1), (2), (3)	V_{IN} = V_{SS}, f_T = 700 kHz		7.0	10	pF
CSH0, CSH3 Input Capacitance (C_S)	V_{IN} = V_{SS}, f_T = 700 kHz		11	14	pF
Clock Input Capacitance (C_C)	V_{IN} = V_{SS}, f_T = 700 kHz	30	40	55	pF
Clock "1" Level ($V_{\phi(1)}$) (Note 4)		V_{SS} − 1.0		V_{SS}	V
Clock "0" Level ($V_{\phi(0)}$)		V_{GG}		V_{GG} + 1.0	V
Load Capacitance for DATA(0), (1), (2), (3), CSH0, CSH3 (C_L)	V_{IN} = 0V, f_T = 700 kHz			25	pF
CYOV, FLAG				20	pF
STFL, NREQ0				30	pF
Current Sinking Resistors Required on CYOV, STFL, NREQ0 (R_{SINK}) (Note 3)	From Pin to V_{GG}	4.6		5.8	kΩ
Power Dissipation (P_D) (T_1 − T_8 Equal Width)	f = 700 kHz		600	800	mW

Note 1: Internal pull-up provided for TTL inputs. Refer to Figure 3 and text.
Note 2: Max = most positive; Min = most negative.
Note 3: Required to drive 74H loads. Larger resistance values may be used to drive standard or low power TTL.
Note 4: Clamp diodes and series damping resistors may be required to prevent clock overshoot.

FUNCTIONAL DESCRIPTION OF RALU

A diagram of the RALU is shown in Figure 1. Seven general registers (labelled R_1−R_7) are provided. Any of the seven registers may be loaded onto the A- or B-bus for processing by the arithmetic and logic unit (ALU). The data on the A-bus may be complemented before being loaded on the IA-bus, which serves as the input to the ALU. The operations which may be performed by the ALU are ADD, AND, OR and exclusive OR. The ADD operation adds IA and B and the carry (CSH0) from pin 14. A carry output (CSH3) is provided by pin 11. The result of the ALU operation is available to the shifter via the S-bus. The shifter provides a one bit left or right shift (or no shift) and transfers the shift information in and out of pins 11 and 14. Output data from the shifter may be returned to any of the registers over the R-bus.

A 16 word last in, first out stack (LIFO) is provided and may be accessed over the A- and R-buses. When the bottom word of the stack becomes non-zero a stack full signal (STFL) is provided at pin 3. Status information is provided by a 4-bit status register. Link, Overflow, Carry and Flag indicators are provided in bit positions 3, 2, 1 and 0 respectively (where bit 3 is the most significant bit). The Link flag may be included in shift operations (under control of the Select input) and the Overflow and Carry flags provide information on the result of ADD operations. A general purpose status flag (Flag) is also provided which may be used for interrupt enable or other functions where it is desirable to save status bits on the stack. Also, the Link, Overflow and Carry functions may be disabled, allowing these flags to be used for general purpose application. This is

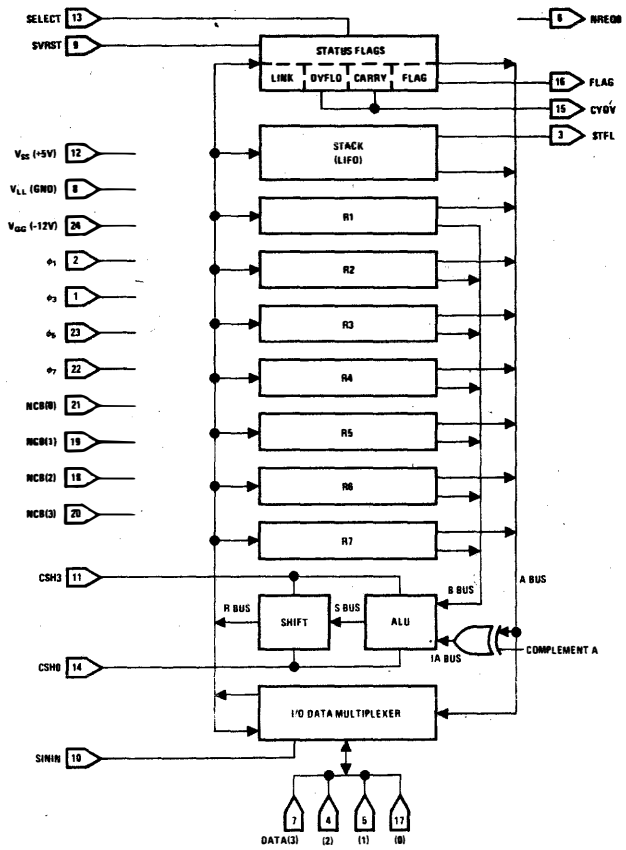


FIGURE 1. RALU Block Diagram

described in the section detailing control signals for the RALU.

Communication between the RALU and the rest of the system is provided by the I/O data multiplexer. This logic provides for loading the R-bus from the external data bus, as well as sending data from the A- and R-buses. Details of signal functions and timing are presented in the following sections. Positive true logic signals are used ("1" = most positive voltage, "0" = most negative voltage). Signal names beginning with N are complemented signals.

FUNCTIONAL DESCRIPTION OF SIGNALS

Signal timing for the RALU is shown in Figure 2. The timing diagram is divided into 8 time intervals (T_1-T_8) based on the 4-phase non-overlapping clocks. The clock inputs have MOS levels of +5V and −12V and occur during the odd time intervals. Thus phase 1 clock is a logic "0" (−12V) during T_1 and a logic "1" (+5V) during T_2-T_8.

Commands

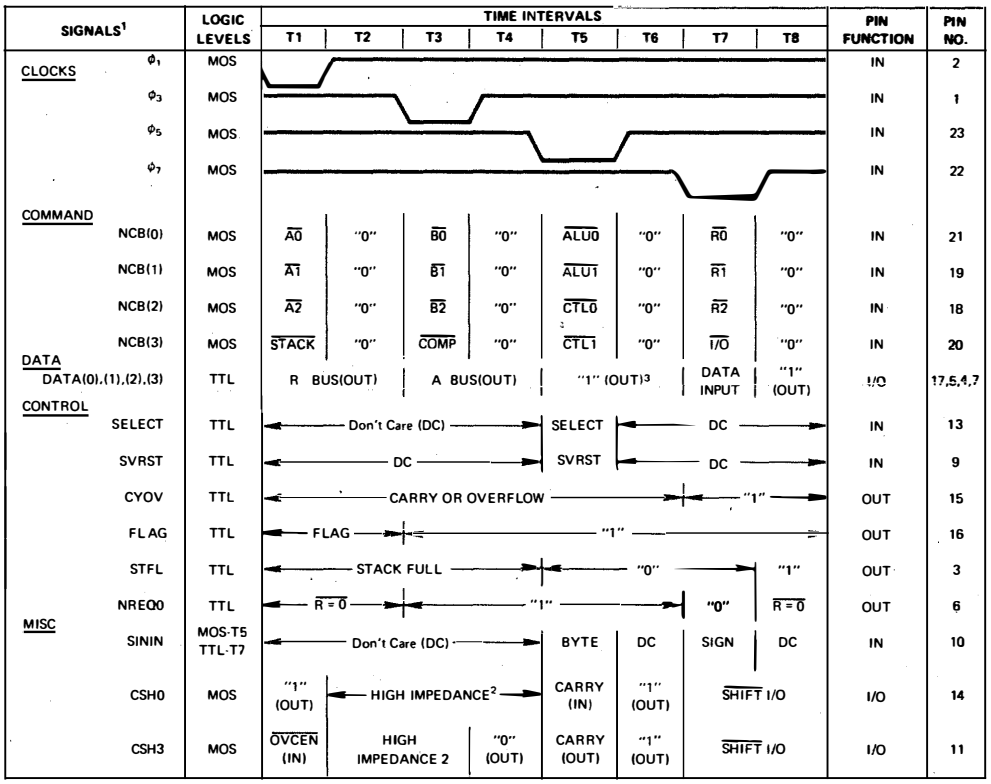
The command inputs to the RALU occur on pins 21, 19, 18, and 20 which correspond to command bits NCB(0), (1), (2), and (3) respectively. The command inputs are complemented MOS signals and are multiplexed over the 4 odd time intervals in each RALU cycle (T_1, T_3, T_5, T_7). The inputs must be driven negative to logic "0" during the even time intervals. The command functions for each bit are indicated in the diagram. During T_1, the three least-significant command bits specify the address of the register (R_1-R_7) to be loaded on the A-bus. If NCB(0), (1), and (2) are all logic "1" the A-bus is set equal to zero. The fourth command bit NCB(3) is used to enable stack operations. If NCB(3) is at a logic "1" (most positive level) no stack operations occur. If it is a logic "0" stack operations are enabled, but will only occur if the A or R-bus address is zero. If the A-bus address is zero the stack will be pulled onto the A-bus. If the R-bus address is zero, the R-bus will be pushed onto the stack.

During T_3 the three least-significant bits specify the address of the register (R_1-R_7) to be loaded on the B-bus. (Note that stack and flags cannot be accessed over the B-bus. An address of zero always gives zero data, however, NCBX's = all 1's.) The most-significant bit specifies that the A-bus is to be complemented when it is transferred to the IA-bus.

During T_5, NCB(1) and NCB(0) specify the ALU operation to be performed as follows: 00-AND, 01-XOR, 10-OR, 11-ADD. NCB(3) and NCB(2) are used to specify control functions as follows: 00-No-OP, 01-R-bus control, 10-shift S-bus left 1-bit position during transfer to R-bus, 11-shift S-bus right 1-bit position during transfer to R-bus.

The R-bus control code is used in conjunction with the I/O control bit (NCB(3) at T_7) and the Byte input (SININ at T_5) to set the value of the R-bus as shown below and in Table I (RALU command code summary).

During T_7 the three least significant bits specify the address of the register (R_1-R_7) to be loaded



Note 1: A positive true logic convention is used for all signals (i.e., "1" = more positive voltage, "0" = more negative voltage). Signal names beginning with N are complemented signals.

Note 2: CSH0 and CSH3 high impedance state for intervals T_2 through T_4 is the TRI-STATE mode for output drivers.

Note 3: "1" (OUT) means RALU is driving this node to the "1" logic level during the defined interval. For bidirectional I/O lines the logic state is defined as "in" or "out."

FIGURE 2. RALU Timing Diagram

from the R-bus. The most-significant bit specifies that the R-bus is to be set equal to the output of the I/O multiplexer rather than the shifter (unless R-bus control was specified at T_5). Reference R-bus control states Table I.

Data

The data transfers between the RALU and memory or peripheral devices occur on pins 17, 5, 4, and 7 which correspond to data bits DATA(0), (1), (2) and (3) respectively. During T_1 and T_2 the data lines are driven with the value of the R-bus which occurred at the end of the *previous timing cycle*. This output may be used by the CROM chip for conditional branch inputs. During T_3 and T_4 the data lines are driven with the value that was loaded onto the A-bus during the current timing cycle. This output is typically used for address and data output to system memory or peripheral devices. During T_5 and T_6 the data lines are driven to a logic "1." During T_7 the data lines are used for input to the RALU from system memory or peripheral devices. *The data receivers are "zeroes catching" so the data lines must not be allowed to go negative during T_7 unless the data input is to be a logic zero.* During T_8 the data lines are again driven to a logic "1" by the RALU. As with all TTL inputs on the RALU a 3K–5K pull-up is provided on the chip to insure an adequate logic "1" level (see Figure 3). The pull-up is provided by an MOS transistor which is turned on only during the data input interval. At other times it is in the "off" or high impedance state.

Control Signals

The RALU control lines provide a means of using the RALU status flags. The SELECT line is used as an input at T_5 ("zeroes catching") and is unused at other times. If the SELECT line is a logic "1" at T_5 the Overflow status flag will be selected as the output on the Carry or Overflow (CYOV) line (pin 15) during the *following* cycle. If the RALU is in the most significant byte of a processor (as specified by the Byte input on the SININ line) the Link status flag will be included in any shift that occurs in the current cycle. The shift will be a five (5) bit shift with the Link in the most significant bit position. If the Select input is a logic "0" at T_5 the Carry status flag will be selected at the CYOV output and shift operations will not affect the Link.

The Save/Restore (SVRST) line is used as an input during T_5 ("zeroes catching") and provides a means of modifying the status flags over the data bus. If SVRST is a logic "1" during T_5 the status flags will be loaded onto the A-bus during the *following cycle (at T_1),* provided the A-bus address bits NCB(2), (1), and (0), at T_1 during that cycle are a logic "1." If a pull stack operation has been specified by NCB(3), (2), (1), and (0) at T_1, the SVRST input at T_7 will inhibit it and instead the status flags will be loaded on the A-bus. Table II specifies the control bits and the data that occurs on the A-bus at T_1. The SVRST line also causes the status flags to be loaded from the R-bus at the end of the following cycle. (The status of

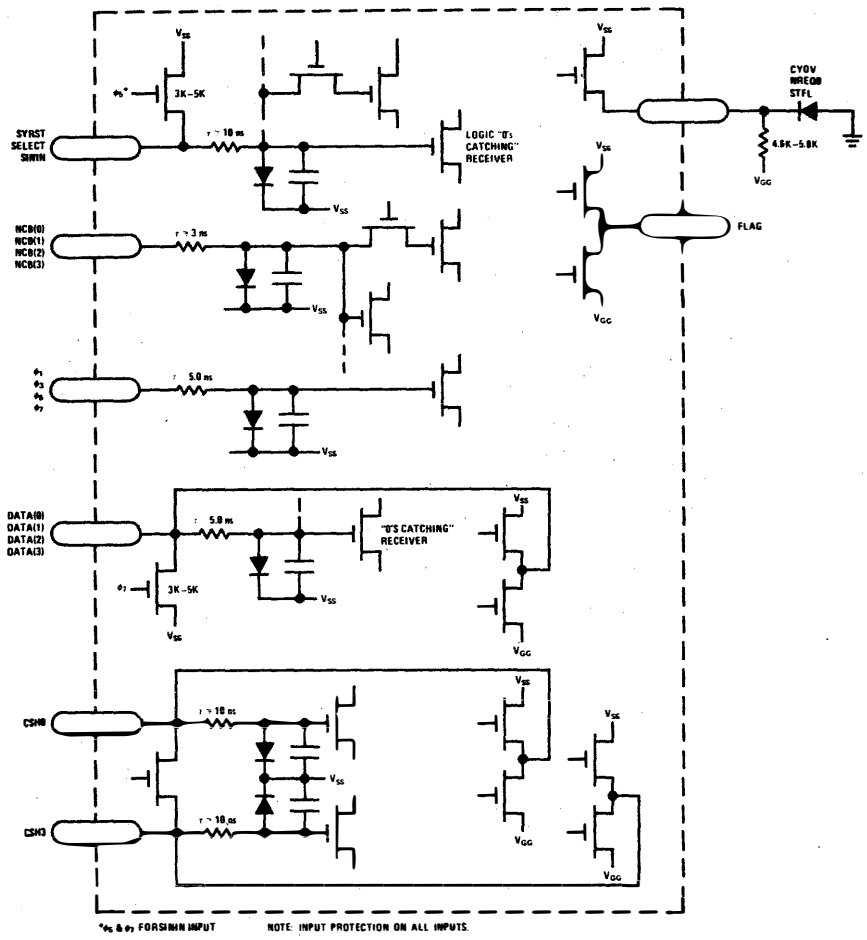


FIGURE 3. RALU Driver and Receiver Buffers

SVRST during *one cycle* only affects conditions in the *following cycle.*) This will occur in parallel with the loading of any other register specified by the R-bus address. Table III specifies the control bits and the results that occur on the R-bus.

The CYOV line provides an output signal indicating the state of the Carry or Overflow status flag as determined by the Select input. The Flag output indicates the state of the general purpose status flag. The stack full (STFL) output goes true when the bottom word of the stack is non-zero *at the start of the preceding cycle.* The result bus equals zero (NREQ0) output goes to logic "0" level when the R-bus contains all zeroes. The CYOV, STFL and NREQ0 outputs require an external resistor connected to V_{GG}.

Miscellaneous Signals

The SININ line is used to input information as to whether the RALU is in the most or least significant byte of a processor word (at T_5) and also the sign value which is propagated to the most significant byte (at T_7) when the R-bus control function is specified. If SININ is a logic "1" at T_5 the RALU will enable the functions of the most significant byte. The functions enabled are inclusion of the Link in shift operations and setting the R-bus to zero or sign as specified by the R-bus control code. If SININ at T_5 is a logic "0" the functions are not enabled.

The carry input (CSH0) and carry output (CSH3) lines are used primarily for transfer of carry and shift information between RALU's or between RALU and CROM. If an ADD operation is specified, the value of carry input (CSH0) at T_5 will be added to the IA and B-bus inputs to the ALU. The resulting carry output from the most significant bit will occur on CSH3 at T_5. When a left shift is specified, the shift output from the most significant bit occurs on CSH3 at T_7 and T_8 while the shift input ("zeroes catching") to the least significant bit must be provided on CSH0 during T_7 and T_8. The pins exchange roles for a right shift. During T_1 the CSH3 input (if a logic "0" at T_1) is used to enable the Overflow and Carry flags to be set to the result of an ADD operation, *if an ADD is specified for the current cycle.* The Carry flag is set equal to the value of the ripple carry out of the most significant bit of the ALU. The Overflow flag is set if there is a two's complement arithmetic overflow (i.e. sign of both operands was the same and the sign of the result is different). For systems using multiple RALU's the Overflow and Carry flags of all but the most significant RALU will be disabled by the logic "1" output of CSH0 generated by the adjacent RALU at T_1. These flags may therefore be used for general purpose functions.

TABLE I. RALU Commands

1.A Command Inputs

COMMAND BITS[1]

TIME INTERVAL	NCB(3)	NCB(2)	NCB(1)	NCB(0)
T1	STACK	← A BUS →		
T3	COMP	← B BUS →		
T5	← CTL →		← ALU →	
T7	I/O	← R BUS →		

1.B Command Codes[3]

ALU FUNCTIONS

NCB(1), (0) @ T5	FUNCTION
11	AND
10	XOR
01	OR
00	ADD

CTL FUNCTIONS

NCB(3), (2) @ T5	FUNCTION
11	NONE
10	R BUS CONTROL
01	SHIFT LEFT
00	SHIFT RIGHT

A, B & R BUS ADDRESSES

NCB(2), (1), (0)	ADDRESS
111	ZEROES, FLAGS, STACK[2]
110	R1
101	R2
100	R3
011	R4
010	R5
001	R6
000	R7

R BUS CONTROL

I/O (NCB(3) @ T7)	BYTE (SININ @ T5)	R BUS VALUE
1	0	OUTPUT OF SHIFTER
1	1	OUTPUT OF SHIFTER
0	0	OUTPUT OF I/O MUX
0	1	VALUE OF SIGN INPUT ON SININ @ T7

Note 1: Commands are complemented signals.

Note 2: See text and Tables II and III for addressing flags and stack. B bus only addresses zeroes.

Note 3: Logic values shown are values which must be applied to NCB inputs to get indicated results.

TABLE II. Binary Table for A Bus Addressing (Time Interval T_1)

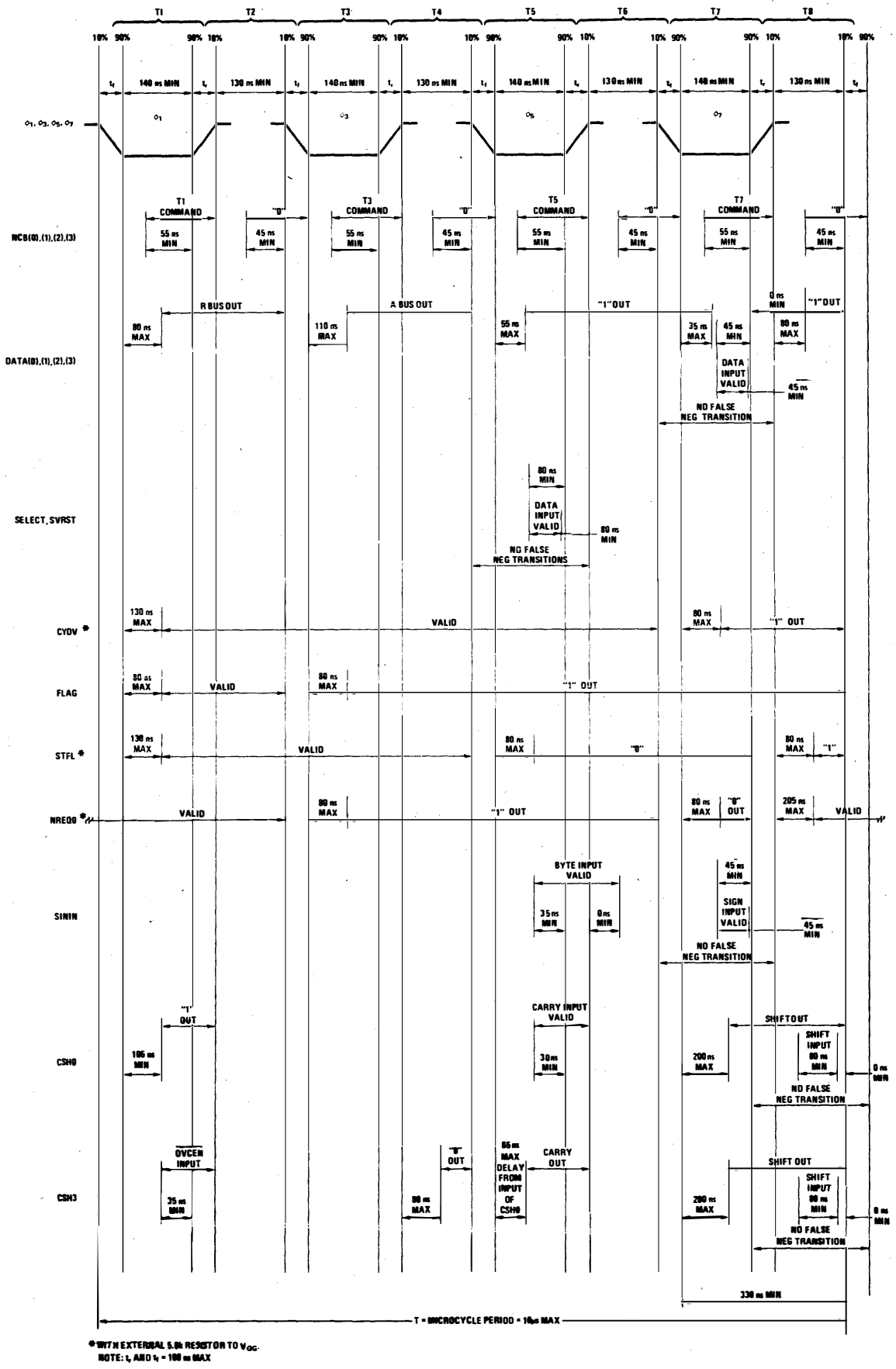
INPUTS		RESULTING DATA ON A BUS
SVRST @ Previous Cycle T_5	NCB (3), (2), (1), (0) @ Current Cycle T_1	
0	1 1 1 1	All Zero's
0	1 1 1 0	Contents of R_1
0	1 1 0 1	Contents of R_2
0	1 1 0 0	Contents of R_3
0	1 0 1 1	Contents of R_4
0	1 0 1 0	Contents of R_5
0	1 0 0 1	Contents of R_6
0	1 0 0 0	Contents of R_7
0	0 1 1 1	Pull Stack
0	0 1 1 0	Contents of R_1
0	0 1 0 1	Contents of R_2
0	0 1 0 0	Contents of R_3
0	0 0 1 1	Contents of R_4
0	0 0 1 0	Contents of R_5
0	0 0 0 1	Contents of R_6
0	0 0 0 0	Contents of R_7
1	1 1 1 1	Status Flags
1	1 1 1 0	Contents of R_1
1	1 1 0 1	Contents of R_2
1	1 1 0 0	Contents of R_3
1	1 0 1 1	Contents of R_4
1	1 0 1 0	Contents of R_5
1	1 0 0 1	Contents of R_6
1	1 0 0 0	Contents of R_7
1	0 1 1 1	Status Flags
1	0 1 1 0	Contents of R_1
1	0 1 0 1	Contents of R_2
1	0 1 0 0	Contents of R_3
1	0 0 1 1	Contents of R_4
1	0 0 1 0	Contents of R_5
1	0 0 0 1	Contents of R_6
1	0 0 0 0	Contents of R_7

Note: Logic values shown are what must be applied to NCB (which is a complemented signal) to get desired results.

TABLE III. Binary Table for R Bus Addressing (Time Interval T_7)

INPUTS		REGISTER LOADED FROM R BUS
SVRST @ Previous Cycle T_5	NCB (3) @ Current Cycle T_1 and NCB (2), (1), (0) @ Current Cycle T_7	
0	1 1 1 1	Not Stored
0	1 1 1 0	R_1
0	1 1 0 1	R_2
0	1 1 0 0	R_3
0	1 0 1 1	R_4
0	1 0 1 0	R_5
0	1 0 0 1	R_6
0	1 0 0 0	R_7
0	0 1 1 1	Push Stack
0	0 1 1 0	R_1
0	0 1 0 1	R_2
0	0 1 0 0	R_3
0	0 0 1 1	R_4
0	0 0 1 0	R_5
0	0 0 0 1	R_6
0	0 0 0 0	R_7
1	1 1 1 1	Status Flags
1	1 1 1 0	Status Flags and R_1
1	1 1 0 1	Status Flags and R_2
1	1 1 0 0	Status Flags and R_3
1	1 0 1 1	Status Flags and R_4
1	1 0 1 0	Status Flags and R_5
1	1 0 0 1	Status Flags and R_6
1	1 0 0 0	Status Flags and R_7
1	0 1 1 1	Status Flags and Push Stack
1	0 1 1 0	Status Flags and R_1
1	0 1 0 1	Status Flags and R_2
1	0 1 0 0	Status Flags and R_3
1	0 0 1 1	Status Flags and R_4
1	0 0 1 0	Status Flags and R_5
1	0 0 0 1	Status Flags and R_6
1	0 0 0 0	Status Flags and R_7

Note: Logic values shown are what must be applied to NCB inputs to get results shown.



*WITH EXTERNAL 5.0k RESISTOR TO V_{CC}.
NOTE: t_r AND t_f = 100 ns MAX

FIGURE 4. RALU Signal Timing Specifications

(T_A = 0°C to +70°C, V_{SS} = +5.0V ±5%, V_{GG} = −12V ±5%, V_{LL} = GND)

Recommended Start-up Conditions

Power supplies must be within specification for ten microseconds (10μs) before clocks are started. (Note: All internal nodes must be in a discharged state before start-up.) When power supplies are cycled on and off rapidly the nodes must be discharged by running the clocks for one (1) microcycle (T_1-T_8) after power is removed from the RALU. An internal initialize pulse causes the status flags, registers and the stack to be cleared at power on.

It is recommended that STFL and CYOV be tied to V_{SS} if not used.

SIGNAL TIMING SPECIFICATIONS

The timing specifications for all RALU signals are shown in Figure 4. These specifications apply over the complete range of recommended operating conditions (T_A = 0°C to +70°C, V_{SS} = +5V ±5%, V_{GG} = −12V ±5%). Time intervals are defined with respect to the 10% and 90% points of the four MOS clock inputs. The clocks have a maximum rise and fall times of 100 ns. The command inputs on the NCB lines must be valid a minimum of 55 ns prior to the end of the odd time intervals (see Figure 3). Data inputs to the RALU over the data lines must be valid for at least 35 ns during T_7 and *must never go falsely negative to a logic zero, during T_7, due to the "zeroes catching" nature of the receiver.* It will often simplify interface design if input data to the RALU is gated onto the data bus during parts of T_6 and T_8 as well as during the required interval T_7. The logic "1" outputs of the RALU data lines at T_6 and T_8 may be overridden by the data input drive; however, the increased power dissipation will lower the maximum allowable ambient temperature for the chip. (Note: The logic "1" output drive has a minimum impedance of 300Ω to V_{SS}.)

The specification of the carry output (CSH3) applies only when the carry input to CSH0 is valid prior to the start of T_5. If the CSH0 input is not valid at the start of T_5 then the CSH3 output will become valid a maximum of 65 ns after the input becomes valid. In a typical 16-bit application the carry input (CSH0) to the least significant RALU will be valid at the start of T_5, however, the carry input to the more significant RALU's will be delayed, since it must first be generated at the CSH3 output of the preceding less significant RALU.

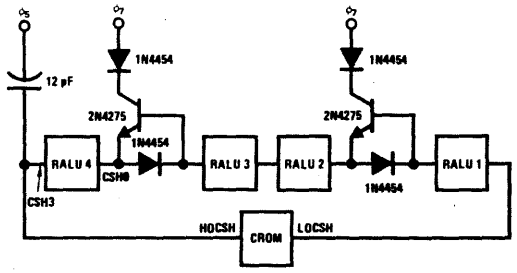
As indicated on the CSH0 timing specification, the latest the CSH0 input can become valid for a proper RALU ADD operation to occur is 30 ns before the end of T_5.

The output from CSH3 is valid within 65 ns of a valid input at CSH0. In a system with multiple RALU's the carry must propagate through each RALU and provide a valid input to the most significant RALU at least 30 ns before the end of T_5. For a system with N RALU's, the minimum width of T_5 to allow for carry propagation is 30 + 65N ($N \leq 8$). However, this is strongly affected by the carry line capacitance (this capacitance should be minimized as much as possible, especially for the high order bits).

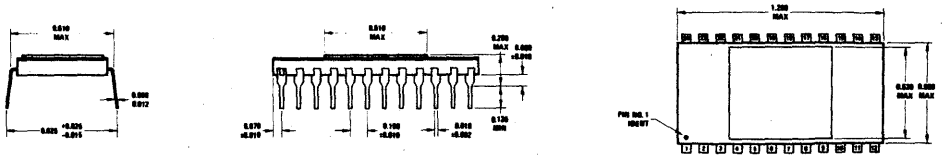
For systems where N is large, T_5 should be streched to provide the additional time. Alternatively the buffer circuit shown in the figure below may be used between RALU's. A single buffer between the center RALU's will typically reduce the carry propagation time by about 20%, however the noise margin is reduced somewhat.

Two carry speed up circuits may be used to allow operation of a 16-bit system at a 1.4μs microcycle time. The degradation of the carry signal's logic "1" level with two speed up circuits may be significant under adverse conditions. A simple circuit to improve this situation consists of a small capacitor (12 pF) between the ϕ_5 clock and the carry line out of the high order RALU (HOCSH).

A 16-bit system using two speed up circuits with the compensating capacitor is shown below. The minimum width of T_5 for this 16-bit system is 170 ns (valid over 0°C to +70°C).



physical dimensions



Cavity Dual-In-Line Package (D)
Order Number IMP-00H/520D

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