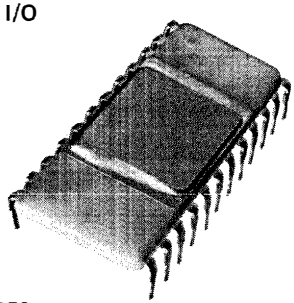
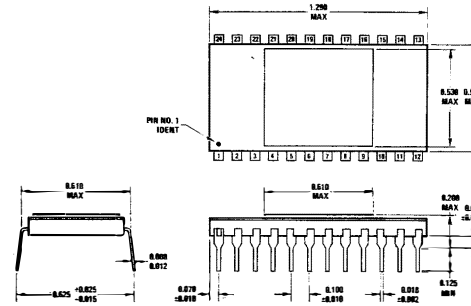
JUNE 1975

NATIONAL μSPEC 7

POWR I/O





FEATURES

- GREATER THROUGHPUT — high-speed transfer instructions provide marked improvements of input and output speeds — up to 97k words per second. Also, memory search functions are many times faster than equivalent macrocode functions.
- LOWER PROGRAMMING COSTS — in many cases, a single instruction replaces an entire subroutine; the Block Transfer Instruction is an example. With POWR I/O, you can do more in less time, and at reduced programming costs.
- LOWER SYSTEM COSTS — not only is the cost of software less with POWR I/O, the hardware costs are also less. More powerful instructions mean better memory efficiency; thus, less memory is required. Also, better performance of the CPU means fewer TTL circuits.

INTRODUCTION

Have you ever wished for an extension to the basic instruction set of your IMP-16 microprocessor — one that would include a wide range of input/output functions? Well, your wish has come true. The Power Input/Output Control Read Only Memory (designated the POWR I/O) chip provides a variety of peripheral Input/Output functions that can save you time, software, and, obviously, a considerable sum of money.

If your microprocessing system is geared to Input/Output devices, is heavily oriented toward interrupt subroutines, or if it must make extended memory searches, then you should definitely think "POWR I/O." More specifically, you should use POWR I/O — remember, it's ready for you when you're ready for it.

TECHNICAL DESCRIPTION

Instruction Set

The extended instruction set provided by the POWR I/O CROM chip is summarized in Table 1.

System Compatibility and Hardware Considerations

The POWR I/O can be used as a first, second, or even as a third CROM with any IMP-16 microprocessor system.

Both block transfer commands (BIN and BOUT) use JUMP CONDITION 14 as a READY sense input. The microcode that executes these two instructions tests the READY input status before each peripheral read or write cycle. If the READY input is low, the read or write instruction is executed; otherwise, the CPU waits. To obtain the maximum rate, the READY input must always be low; if it is not, the transfer rate is degraded.

Software Diagnostics

Diagnostic routine CRM3DI verifies each step in the POWR I/O microprogram. The CRM3DI program is available as a separate order item in either load-module format for prototyping systems or in PROM/ROM format. In either case, complete user directions are contained in the software listing.

ORDERING INFORMATION

To expedite delivery of your POWR I/O chip, order in accordance with the following product descriptions.

- IMP-16A/423D (Military): -55°C to +85°C; ceramic 24-pin DIP
- IMP-16A/423N (Military): -55°C to +85°C; molded 24-pin DIP
- IMP-16A/523D (Commercial): 0°C to +70°C; ceramic 24-pin DIP
- IMP-16A/523N (Commercial): 0°C to +70°C; molded 24-pin DIP

For additional information on this product, contact the nearest National Semiconductor Sales/Service Representative or communicate directly with our World Headquarters.

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B15M65/Printed in U.S.A.

μSPEC 7

Table 1. Instruction Set for POWR I/O

Mnemonic and Description	Opcode	Execution Time
BIN (Block INput to memory) Data from an input device is loaded into memory starting at address specified by AC2. Block length determined by AC1, inputting device by AC3. Data transfer synchronized by jump condition 14 (READY).	01F0	8N + 1W per word plus instruction fetch overhead of 2N + 1R (approximately 85.5k words per second)
BOUT (Block OUTput from memory) Same as BIN, except data is transferred from rather than to memory.	01E0	7N + 1R per word plus instruction fetch overhead of 3N + 2R (approximately 97.1k words per second)
MIN (Memory INput) Data from input device (address in AC3) is read and stored in memory location (address in AC2).	01D0	7N + 1R + 1W (approximately 10.8 μs)
MOUT (Memory OUTput) Same as MIN, except data is transferred from rather than to memory.	01C0	6N + 2R (approximately 9.4 μs)
SSAC (Save Status and ACcumulators) Contents of AC0/AC1/AC2/AC3, RALU Status Flags, and state of SEL flag successively stored in memory, beginning with the address contained in memory location 2 (software stack pointer). After execution, current contents of RALU flags are destroyed.	01B0	31N + 2W + 2R (approximately 47.9 μs)
RSAC (Restore Status and ACcumulators) Software Stack accessed to restore data saved by SSAC instruction.	01A0	26N + 1W + 8R (approximately 36.4 μs)
SSTK (Save STacK) Contents of RALU stack (16 words) stored in software stack (beginning at the contents of memory address 2).	0190	74N + 18W + 3R (approximately 115.1 μs)
RSTK (Restore STacK) Software stack accessed to restore data saved by SSTK instruction.	0180	41N + 1W + 18R (approximately 66.9 μs)
SRCH (SeaRCH and compare) Memory block searched for presence of a bit pattern – beginning at address specified by AC3 and ending with address held in AC2. Bit field specified by mask in AC1; bit pattern located in AC0. Bit pattern tested for "ones" – if match is found, the match address is stored in AC3 and next instruction is skipped. If no match is found, AC3 equals AC2, and the next sequential instruction is executed.	0550	7N + 1R (for each word searched) plus instruction fetch overhead of 2N + 1R
SCAN (SCAN right for "ones") Shift AC0 right until a "one" is shifted out – increment AC2 once for each shift. If no "ones" are present, AC2 is unaffected and the next sequential instruction is executed. If a "one" is found and shifted out, the next instruction is skipped and AC0 contains the shifted contents of the original AC0. SEL flag is reset.	0540	(5 to 85)N + 1R
MSCAN (Mask, then SCAN right for "ones") Same as SCAN instruction, except that now AC1 contains a mask of which each "one" indicates those bits to be tested in the 16-bit word (similar to SRCH). SEL flag is reset.	0560	(6 to 86)N + 1R

NOTE: To calculate execution time, make the following substitutions for N, R, and W:
N (microprogram cycle time) = 1.4 μs for IMP-16C
R (nonoverlapped read delay time) = typically 0.25 μs for IMP-16C
W (nonoverlapped write delay time) = typically 0.25 μs for IMP-16C

Manufactured under one or more of the following U.S. patents: 3063252, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408642, 3421025, 3426423, 3440498, 3518750, 3519887, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3583069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248

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