M32632 32-bit Processor

Details

Name: m32632
Created: Jun 24, 2015
Updated: Dec 2, 2018
SVN Updated: Jan 25, 2021
SVN: Browse
Latest version: download (might take a bit to start...)
Statistics: View
Bugs: 0 reported / 0 solved

Project maintainers

- Moeller, Udo

Other project properties

Category:Processor
Language:Verilog
Development status:Stable
Additional info:FPGA proven
WishBone compliant: No
WishBone version: n/a
License: LGPL

Description

M32632 is an implementation of the Series 32000 architecture of National Semiconductor. This 32-bit architecture was popular in the 1980's and began to disappear in the beginning of the 1990's. The first microprocessor was the NS32016. The third generation CPU was the NS32532. This processor is the basis of M32632. In addition M32632 implements the functionality of the NS32381 floating point unit.

Current status

- 27 June 2015 - initial version 1.0 .
- 14 August 2016 - release of version 2.0 .
- 2 December 2018 - release of version 3.0 .

Links

- To learn more about Series 32000 visit http://cpu-ns32k.net.

Features

The M32632 has the following features:

- simple instructions are executed in one clock cycle,
- 8 kByte instruction cache,
- 8 kByte write-through data cache,
- one direct mapped TLB of 256 entries for each cache,
- basic floating-point instructions for 32-bit and 64-bit data types,
- coprocessor interface for custom instructions,
- small size of 15400 LEs,
- 50 MHz clock speed in Altera Cyclone IV FPGA.

Performance

The performance of M32632 at 50 MHz has been measured on a system running NetBSD 1.5.3 with the Dhrystone 2.1 Benchmark compiled with gcc. The source code of Dhrystone was taken from the link at the processor project ao486. The number is:

- 38601 which is equal to 21.97 VAX Mips optimized with -O2

The Linpack Benchmark is a well known program to measure the floating point performance of a computer. The original program was written in Fortran. It can be found here: http://www.top500.org/resources/frequently-asked-questions/ . Compiled with gcc with optimization level -O3 the M32632 achieves

- 3.02 double precision Mflop/s

TRIPUTER Demonstration System

In the past I used the DE0-Nano board for a demonstration system. Due to the limited capabilities of DE0-Nano I changed to another board from Terasic. The new board is the Cyclone V GX Starter Kit. The FPGA is much bigger, more memory is available and more interfaces are build in, for example a HDMI port.

In the Trunk directory you find a subdirectory named TRIPUTER. It contains a simple M32632 system which can be downloaded to the board and used immediately. This simple system is only the beginning of a large project. At the end three different computer systems should be running on the Starter Kit (of course not at the same time). For any further information about the project and the status please visit cpu-ns32k.net/TRIPUTER.