Preliminary

INS8900 Single-Chip 16-Bit N-Channel Microprocessor

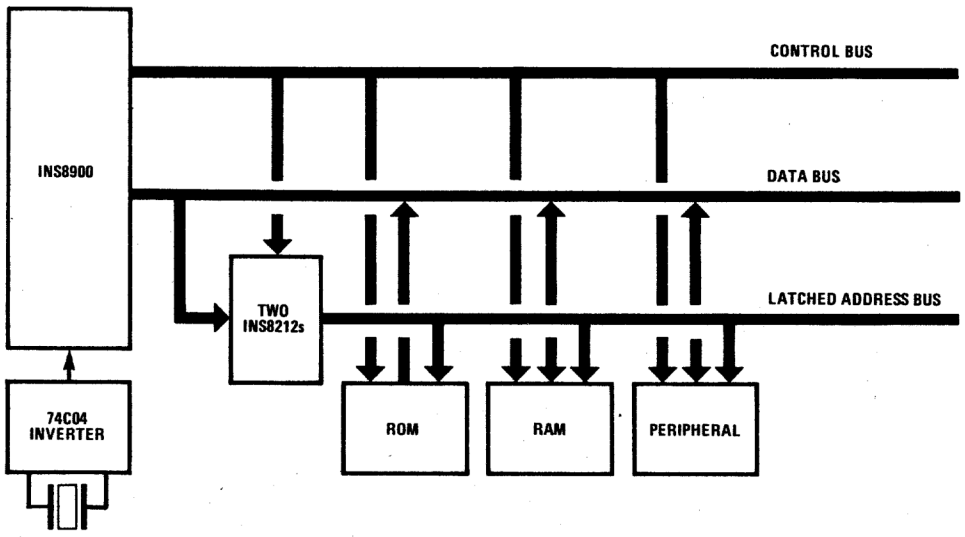
General Description

The INS8900 is a single-chip 16-bit microprocessor housed in a standard hermetically sealed 40-pin ceramic dual-in-line package. The INS8900 is fabricated using N-channel silicon gate MOS technology. The INS8900 is intended for use in applications where the convenience and efficiency of 16-bit word length is desired while maintaining the low cost inherent in single-chip fixed instruction microprocessors. The INS8900 is a true 16-bit central processor unit: it makes use of 16-bit instruction words and 16-bit data words, and features a powerful, efficient, and flexible set of 46 instructions. All instructions use a single-word 16-bit format, thus reducing memory accesses and program storage requirements. A unique feature of the INS8900 is the ability to operate on both 8-bit and 16-bit data words: this extends the inherent efficiency and power of a 16-bit processor to 8-bit applications.

Features

- 46 Instruction Types
- All Instructions Single Word
- Multiple Addressing Modes
  - Program-Counter Relative
  - Base Page
  - Indexed
  - Direct and Indirect
- Four General-Purpose Accumulators
- Byte and Word Processing
- Common Memory and Peripheral Addressing
- Six Hardware-Vectored Priority Interrupts
- 10-Word On-Chip Stack
- Three Control Flag Outputs
- Three Sense Inputs
- Four I/O Control Strobe Signals
- Single-Phase 2 MHz Clock
- Low-Power Schottky Compatible Outputs

INS8900 Minimum System Block Diagram



Absolute Maximum Ratings

Voltage at Any Pin with Resepct to
Most Negative Supply (V_{BB}) . . . . . -0.3 V to +20 V
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range. . . . . -65°C to +150°C
Lead Temperature (soldering, 10 seconds) . . . . . +300°C

Electrical Characteristics

(T_A = 0°C to +70°C, V_{SS} = 0 V, V_{DD} = +12 V ± 5%, V_{CC} = +5 V ± 5%, V_{BB} = −8 V ± 5%)

Symbol	Parameter	Conditions	Min	Max	Units
OUTPUT SPECIFICATIONS					
	D00-D15, F11-F14, ODS, IDS, NADS (These are low-power Schottky-compatible push-pull outputs.)				
V_{OH}	Logic "1" Output Voltage	I_{OUT} = −500 μA	2.4		V
V_{OL}	Logic "0" Output Voltage	I_{OUT} = 900 μA		0.4	V
	NHALT, CONTIN (low-power Schottky outputs)				
V_{OH}	Logic "1" Output Voltage	I_{OUT} = −250 μA	2.4		V
V_{OL}	Logic "0" Output Voltage	I_{OUT} = 600 μA		0.4	V
INPUT SPECIFICATIONS					
	D00-D15, NIR2-NIR5, EXTEND, JC13-JC15, NINIT, CONTIN, NHALT (low-power Schottky inputs)				
V_{IH}	Logic "1" Input Voltage		2.4	V_{CC} + 1	V
V_{IL}	Logic "0" Input Voltage		−1.0	+0.8	V
I_L	Input Leakage Current (except NHALT, CONTIN, JC13-JC15)	$V_{SS} \leq V_{IN} \leq V_{CC} + 1$		40	μA
I_{IL}	Logic "0" Input Current, NHALT, CONTIN (Note 2)	V_{IN} = 0.4 V		−7.0	mA
I_{IL}	Logic "0" Input Current, JC13-JC15 (Note 2)	V_{IN} = 0.4 V		−3.0	mA
	BPS (This is an MOS level input.)				
V_{IH}	Logic "1" Input Voltage		V_{DD} − 1	V_{DD} + 1	V
V_{IL}	Logic "0" Input Voltage		−1.0	+0.8	V
I_{IH}	Logic "1" Input Current (Note 3)	V_{IN} = 13.6 V		750	μA
	CLKX (This is an MOS level input.)				
V_{CIL}	Clock "0" Voltage		−1.0	+0.8	V
V_{CIH}	Clock "1" Voltage		V_{DD} − 1	V_{DD} + 1	V
C_{IN}	Input Capacitance			20	pF
I_{DD}	Average Supply Current (V_{DD}) (Note 4)	t_P = 500 ns, T_A = 25°C		100	mA
I_{CC}	Average Supply Current (V_{CC}) (Note 4)	t_P = 500 ns, T_A = 25°C		10	mA
I_{BB}	Average Supply Current (V_{BB})	V_{BB} = −8 V		−200	μA

Timing Specifications

Symbol	Parameter	Conditions	Min	Max	Units
	CLKX				
t_r, t_f	Rise and Fall Times (Note 5) (Referenced to 10% and 90% amplitude)		5	30	ns
t_P	Clock Period		500	650	ns
t_{CLK}, t_{NCLK}	Pulse Width (Referenced to 50% amplitude)		$t_P/2 - 5\%$	$t_P/2 + 5\%$	ns
	EXTEND				
	Individual Extend Duration			2	μs
t_{ES}	Extend Setup Time (Note 6)		70		ns
t_{EH}	Extend Hold Time (Note 6)		120		ns
	Propagation Delay				
t_{DD1}	NHALT, CONTIN (Note 7)	C_L = 40 pF, 1 low-power Schottky load		200	ns
t_{DD2}	NADS, IDS, ODS, D00-D15 (Note 7)	C_L = 40 pF, 1 INS8208 load		200	ns
	D00-D15				
t_{DS}	Input Setup Time (Note 6)		50		ns
t_{DH}	Hold Time (Note 8)		0		ns
t_{FW}	F11-F14 Pulse Flag (PFLG) Pulse Width		$4t_P - 300$	$4t_P + 300$	ns
t_{NW}	NINIT Initialization Pulse Width		8		t_P
t_{IRW}	NIR2-NIR5 Input Pulse Width to Set Latch		1		t_P

Note 1: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.

Note 2: NHALT, CONTIN, and JC13-JC15 logic "0" input currents specified when the internal chip loads are putting out a logic "1."

Note 3: Pull-down transistor provided on chip.

Note 4: Supply currents measured with 40 pF and INS8208 loads.

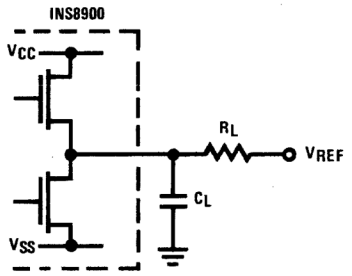
Note 5: Clamp diode and series damping resistor may be required to prevent clock overshoot.

Note 6: Measured with respect to appropriate valid logic level of CLKX.

Note 7: Delay measured from valid logic level on CLKX edge initiating change to valid output voltage level.

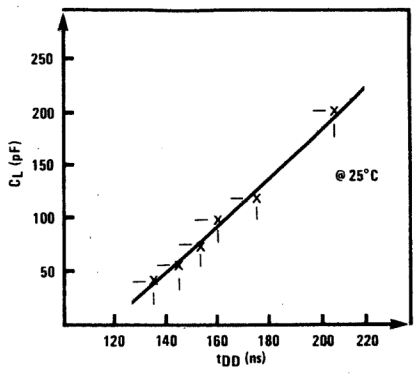
Note 8: With respect to the valid "0" level on the falling edge of Input Data Strobe (IDS).

Note 9: Typical load circuit:

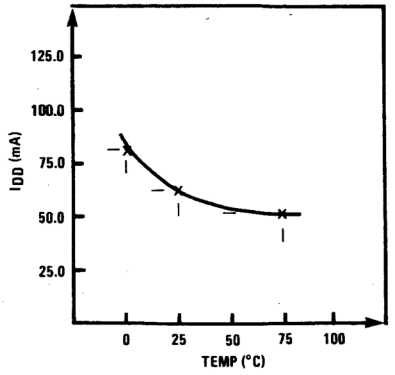


R_L = 3.6k (3.3k for testing)
C_L = 40 pF
V_{REF} = 1.72 V

Note 10: Typical output delay versus load capacitance C_L for load circuit in Note 9:



Note 11: Typical V_{DD} supply current versus temperature.



Timing Waveforms

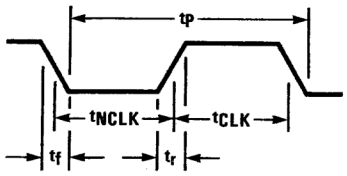


Figure 1. External Clock Timing (CLKX)

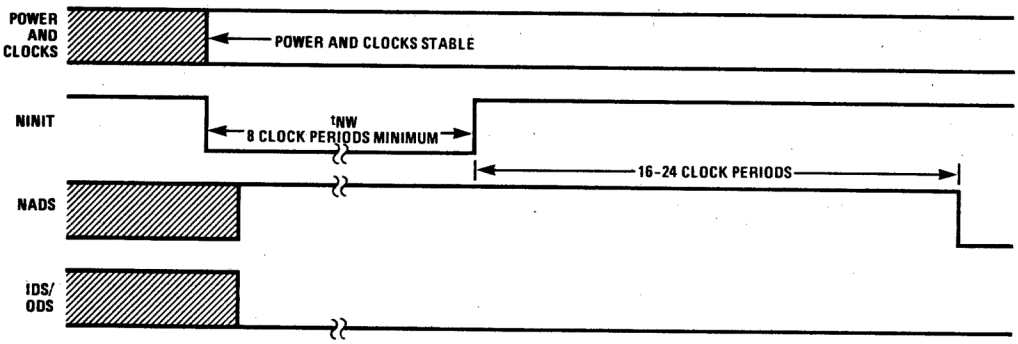
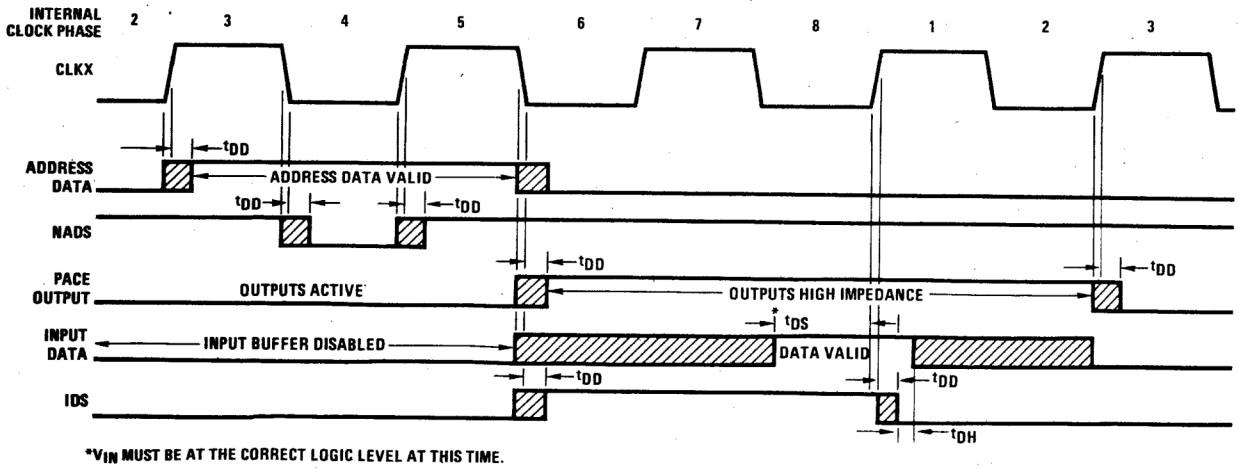


Figure 2. Initialization Timing



*V_{IN} MUST BE AT THE CORRECT LOGIC LEVEL AT THIS TIME.

NOTE: SIGNALS ARE REFERENCED TO VALID LOGIC LEVELS ON CLOCK INPUT. INTERNAL CLOCK PHASES ARE SHOWN FOR REFERENCE ONLY; THEY ARE NOT AVAILABLE EXTERNALLY.

Figure 3. Address Output and Data Input Timing

Timing Waveforms (continued)

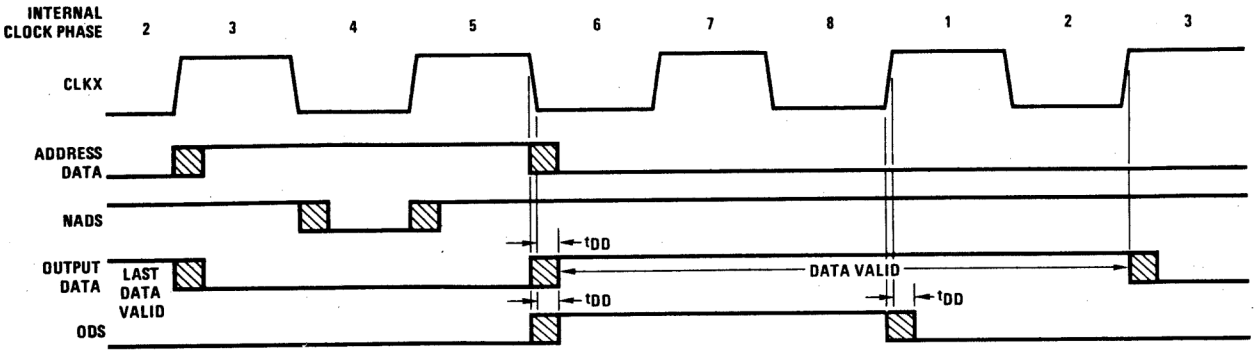


Figure 4. Data Output Timing

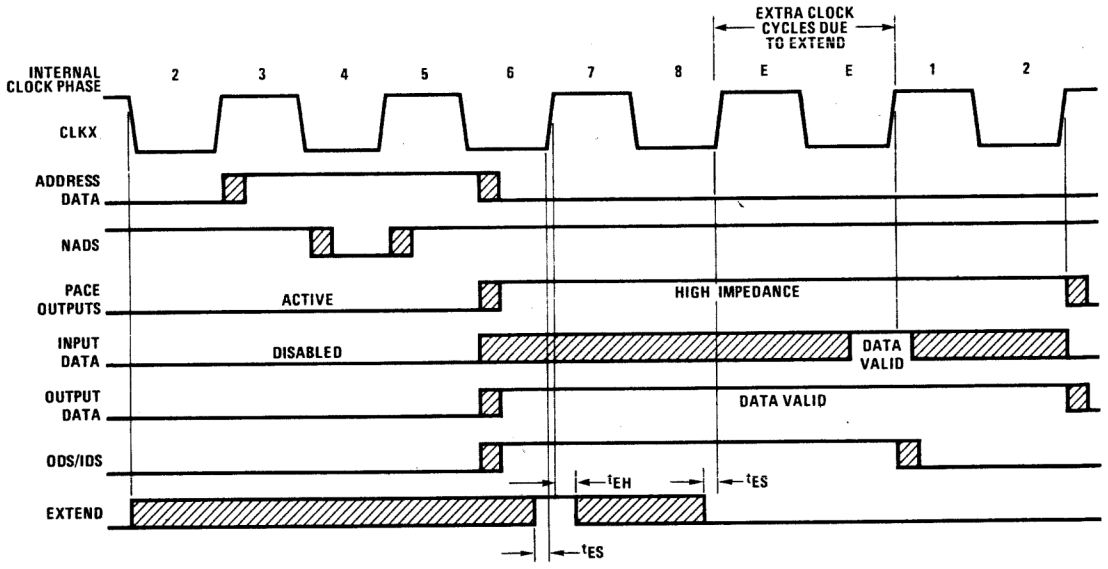


Figure 5. Extend I/O Signal Timing

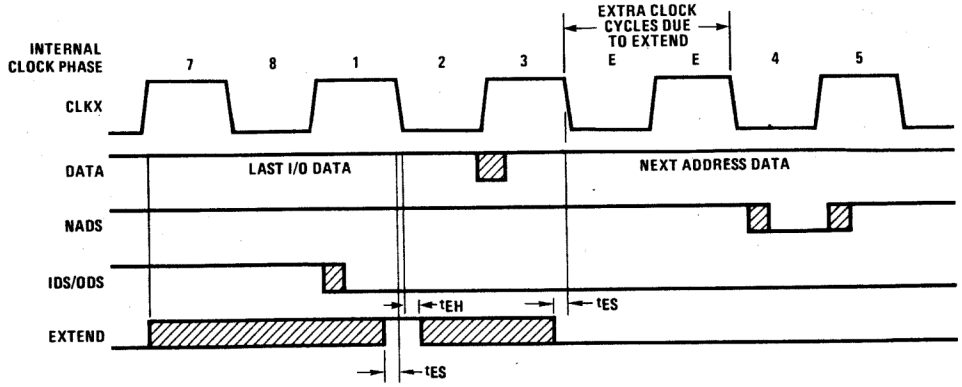
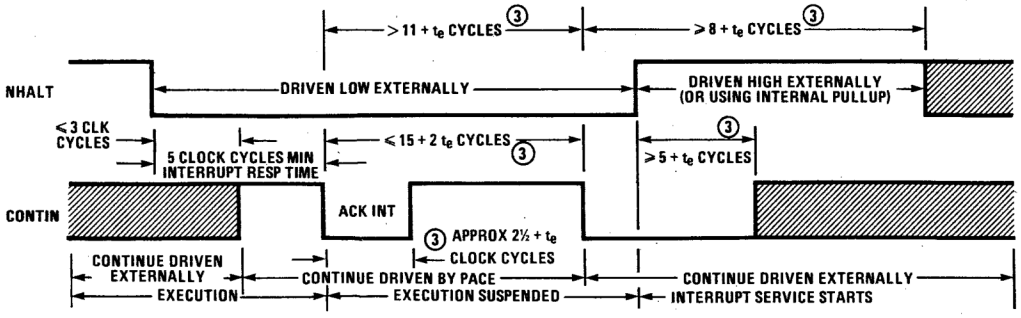


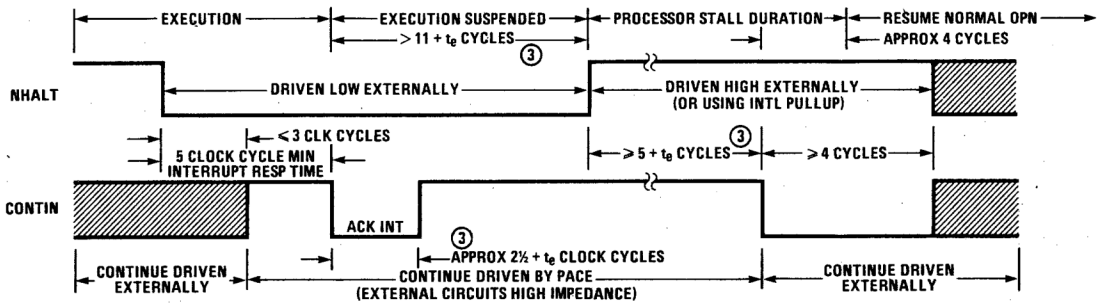
Figure 6. Suspend I/O Signal Timing

Timing Waveforms (continued)



NOTES:
1. EXTERNALLY GENERATED TTL INPUTS OVERRIDE PACE OUTPUTS.
2. ▨ CROSSHATCH INDICATES "DON'T CARE" INPUT STATE.
3. t_e = DURATION OF EXTEND DURING PACE I/O CYCLES TIMING ASSUMES NO OTHER EXTENDS AND NO SUSPENDS.

Figure 7. Relative Timing for Level-0 Interrupt Generation



NOTES:
1. EXTERNALLY GENERATED TTL INPUTS OVERRIDE PACE OUTPUTS.
2. ▨ CROSSHATCH INDICATES "DON'T CARE" INPUT STATE.
3. t_e + DURATION OF EXTEND DURING PACE I/O CYCLES TIMING ASSUMES NO OTHER EXTENDS AND NO SUSPENDS.

Figure 8. Relative Timing for Processor Stall

The architecture of the INS8900 (shown in Figure 9) features a number of resources to minimize system program and read/write storage, increase throughput, and reduce the amount and cost of external support hardware. Principal resources that allow these efficiencies to be achieved include:

Four 16-bit general purpose working registers available to the user reduce the number of memory load and store operations associated with saving temporary and intermediate results in system memory.

An independent 16-bit status and control flag register automatically and continuously preserves system status. The user may operate on its contents as data, allowing masking, testing, and modification of several bit fields simultaneously.

A ten-word (16-bit) last-in, first-out (LIFO) stack inherently decreases response time to interrupts while eliminating both program and read/write system storage overhead associated with storing stack information outside the microprocessor chip.

Stack full/stack empty interrupts are provided to facilitate off-chip stack storage in those applications where additional stack capacity is desirable.

A six-level vectored priority interrupt system internal to the chip provides automatic interrupt identification, eliminating both program storage overhead and the time normally required to poll peripherals in order to identify the interrupting device.

Three sense inputs and four control flag outputs allow the user to respond directly to specific combinations of status present in the microprocessor-based system, thus eliminating costly hardware, program overhead, and throughput associated with implementing these functions over the system data bus.

A comprehensive set of input/output control signals provided by the internal control logic simplifies interfaces to memory and peripherals and allows flexible control of INS8900 operations.

Single-phase 2.0 MHz clock input is easily generated with a minimum of external components.

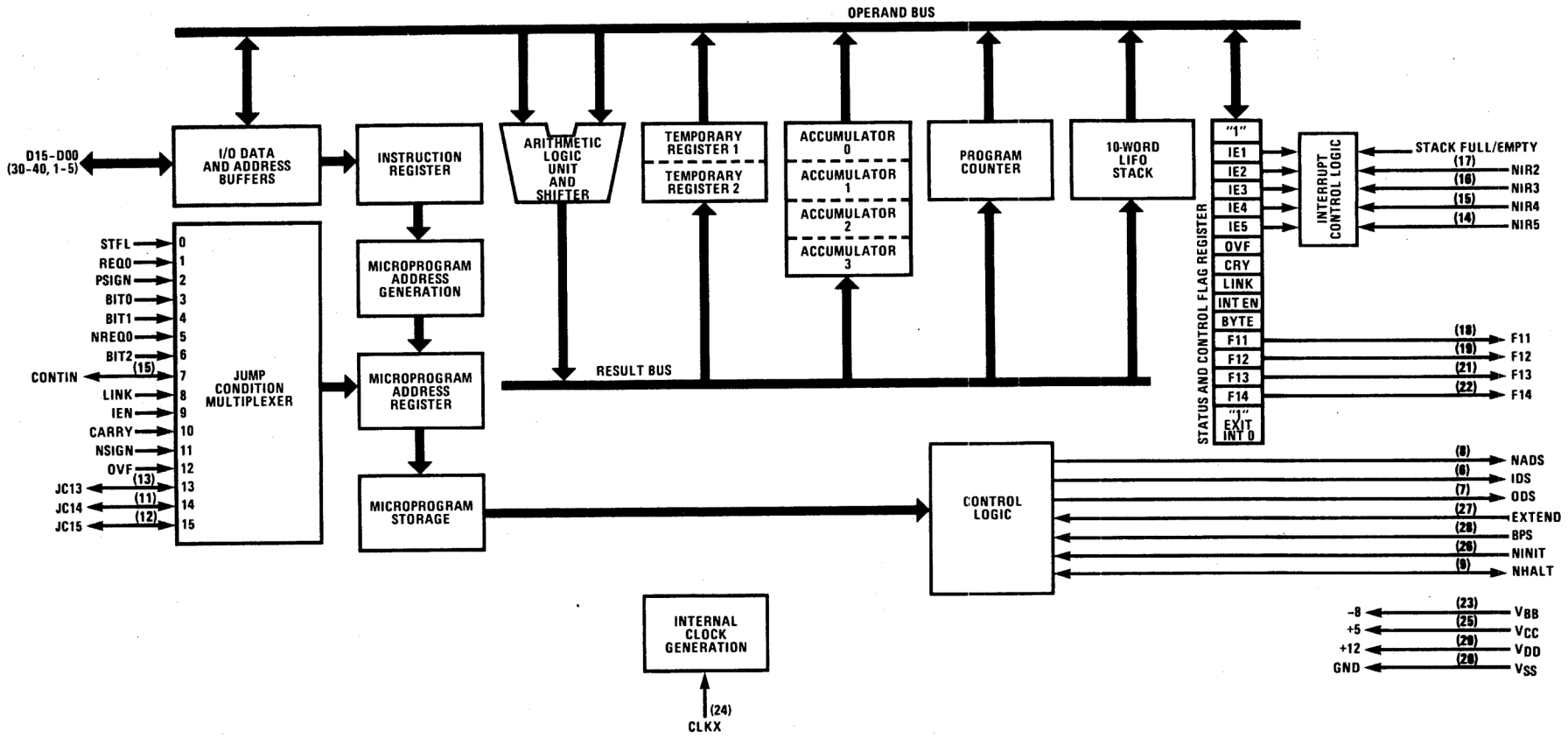


Figure 9. INS8900 Detailed Block Diagram

INS8900 FUNCTIONAL PIN DEFINITIONS

The functions of each of the INS8900 signals are described below. Voltage and timing specifications for the signals are provided in the table of electrical characteristics and the timing diagrams, respectively.

CLKX (Input): External clock input (single-phase).

D00–D15 (Input/Output): Data bus lines. Bidirectional low-power Schottky-compatible lines used for input and output of data and for output of 16-bit addresses on I/O cycles.

NADS (Output): Address Data Strobe. The negative-true NADS signal is sent out at the beginning of every data input/output cycle and indicates that a memory or peripheral address has been output on the data bus lines. The address is stable on the data bus while the NADS signal is active low.

ODS (Output): Output Data Strobe. The ODS signal indicates to external circuits that the data bus contains valid output data.

IDS (Output): Input Data Strobe. The IDS signal indicates to external devices that the INS8900 is performing a data input cycle. The signal should be used by memory or peripheral devices to gate data onto the INS8900 data bus lines.

EXTEND (Input): Extended Data Transfer. The EXTEND signal is used by slower memory or peripheral devices to temporarily increase the time duration of data input/output transfers. The EXTEND signal should be driven high at the beginning of an ODS or IDS signal and held high until output data has been captured or input data is made available to the data bus. The EXTEND signal can also be used to suspend input/output operations by applying the signal after the end of ODS or IDS.

JC13, JC14, JC15 (Input): Jump Conditions 13, 14, and 15. JC13, -14, and -15 are user-specified inputs that can be tested using the Branch-On-Condition (BOC) Instruction. If the jump condition input specified in the BOC Instruction is high, a program branch is effected. The JC13–JC15 signals are useful for testing status of external devices and receiving serial data.

F11, F12, F13, F14 (Output): General-purpose control flag outputs from the INS8900 Status and Control Flag Register. Individual flags may be set by the Set Flag Instruction (SFLG) and pulsed or reset by the Pulse Flag Instruction (PFLG). The F11–F14 signals may be used for direct control of system functions or serial data output.

NIR2, NIR3, NIR4, NIR5 (Input): Interrupt Requests 2, 3, 4, and 5. When these negative-true input signals are low for 1 clock period, minimum, the associated internal Interrupt Request Latch is set if the corresponding interrupt enable has been set by the user's program. The interrupt will be serviced after completion of the current instruction if the Master Interrupt Enable is set. Interrupt Requests are prioritized, with NIR5 having lowest priority.

NHALT (Input/Output): Halt. When the negative-true NHALT signal is driven low by external logic, it effects a microprocessor stall or Level-0 Interrupt, depending on timing of the CONTIN signal. When not controlled by external logic, NHALT is driven low by the INS8900 for 7/8 of a duty cycle while a programmed halt condition exists. Programmed halt is initiated by the Halt Instruction and terminated by pulsing the CONTIN line via external logic.

CONTIN (Input/Output): Continue. The CONTIN signal is used in the input mode to terminate a programmed halt, or to exercise microprocessor stall and Level-0 Interrupt, or as a jump-condition input that can be tested using a BOC instruction. In the output mode, CONTIN transmits an interrupt acknowledge pulse to acknowledge CPU response to an active interrupt input.

BPS (Input): Base Page Select. The BPS signal enables one of two base-page addressing schemes to be selected. When BPS is low, the first 256_{10} words of memory constitute base page (page zero). When BPS is high, the first 128_{10} memory words and the last 128_{10} memory words constitute base page.

NINIT (Input): Initialize. Initialize is applied after power supplies and clock are stable. While the negative-true NINIT signal is low, the INS8900 operation is suspended, and the IDS/ODS signals are set to the inactive state. After NINIT completes a low-to-high transition, the program counter is set to zero, the internal stack pointer is cleared, and all flags and interrupt enables are set low except Level-0 Interrupt Enable, which is set high. All other registers contain arbitrary values.

POWER SUPPLIES

V_{SS}: Ground.

V_{DD}: +12 volts.

V_{CC}: +5 volts.

V_{BB}: –8 volts.

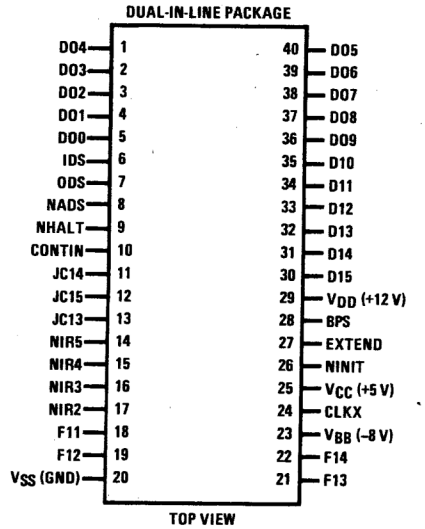


Figure 10. INS8900 Pin Assignment

INTERRUPT SYSTEM

The INS8900 microprocessor provides a six-level, vectored, priority interrupt structure. This allows automatic identification of an interrupting device's level and allows all devices on an interrupt level to be enabled or disabled as a group, independent of other interrupt levels. An individual interrupt enable is provided in the status register for each level, as shown in figure 11, and a master interrupt enable (IEN) is provided for all 5 lower priority levels as a group. Negative true interrupt request inputs are provided to allow several interrupts to be wire ORed on each input. When an interrupt request occurs, it will set the interrupt request latch if the corresponding interrupt enable is true. The latch will be set by any pulse exceeding one clock period in duration, which is useful for capturing narrow timing or control pulses. If the master interrupt enable (IEN) is true, then an interrupt will be generated. During the interrupt sequence an address is provided by the output of the priority encoder and is used to access the pointer for the highest-priority interrupt request (IR0 is highest priority, IR5 is lowest priority). The pointers are stored in locations 2-7 (see table 1) for interrupt requests 1-5 and 0, respectively. The pointer specifies the starting address of the interrupt service routine for that particular interrupt level. Before executing the interrupt service routine, the program counter is pushed on the stack and IEN is set false. The interrupt service routine may set IEN true after turning off the interrupt enable for the level currently being serviced (or resetting the interrupt request). [The interrupt enables may be set and reset using the SFLG and PFLG instructions.]

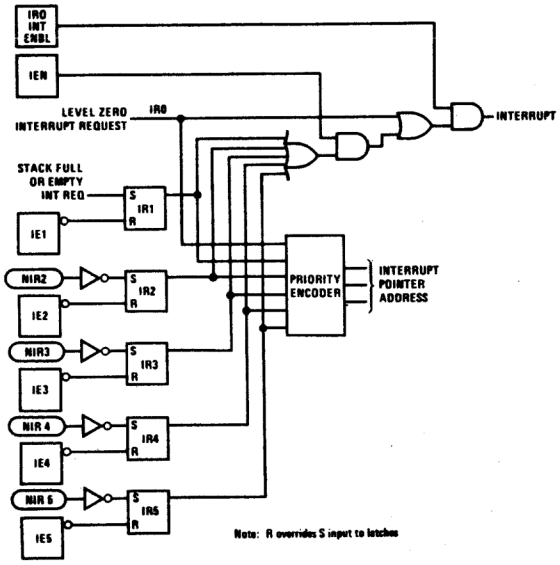


Figure 11. Interrupt System

Table 1. Interrupt Pointer Table

8	Int 0 Program
7	Int 0 PC Pointer
6	Int 5 Pointer
5	Int 4 Pointer
4	Int 3 Pointer
3	Int 2 Pointer
2	Int 1 Pointer
1	Not Assigned
Loc 0	Initialization Inst

The non-maskable level zero interrupt (IR0) is an exception to this interrupt procedure. It has a program counter storage location pointer (The program counter is not stored on the stack for this particular interrupt in order to preserve the processor state.) which is followed by the level zero interrupt service routine. The IR0 interrupt enable is cleared when a level zero interrupt occurs (IEN is unaffected) and may be set true by setting (non-existent) status flag 15. This allows execution of one more instruction (typically JMP@) to return from the IR0 interrupt routine before another interrupt will be acknowledged. This interrupt level is typically used by a control panel, which then can always interrupt the application program and does not affect system status.

Level zero interrupts are generated by exercising the NHALT and CONTIN lines as shown by the relative timing in figure 7. Note that the CONTIN Signal can be used as an interrupt acknowledge to indicate that the interrupt is being processed by the INS8900.

A processor stall may be implemented by driving the NHALT line low. Microprocessor operation is then suspended upon completion of the instruction presently under execution. The suspension may last indefinitely without loss of CPU status and may be terminated by use of the CONTIN Signal as shown by the relative timing in figure 8.

DRIVERS AND RECEIVERS

Equivalent circuits for INS8900 drivers and receivers are shown in figure 12. All inputs have static charge protection circuits consisting of an RC filter and a voltage clamp. These devices should still be handled with care, as the protection circuits can be destroyed by excessive static charge. Pullup transistors on the jump condition inputs are turned on during one of the eight internal clock phases.

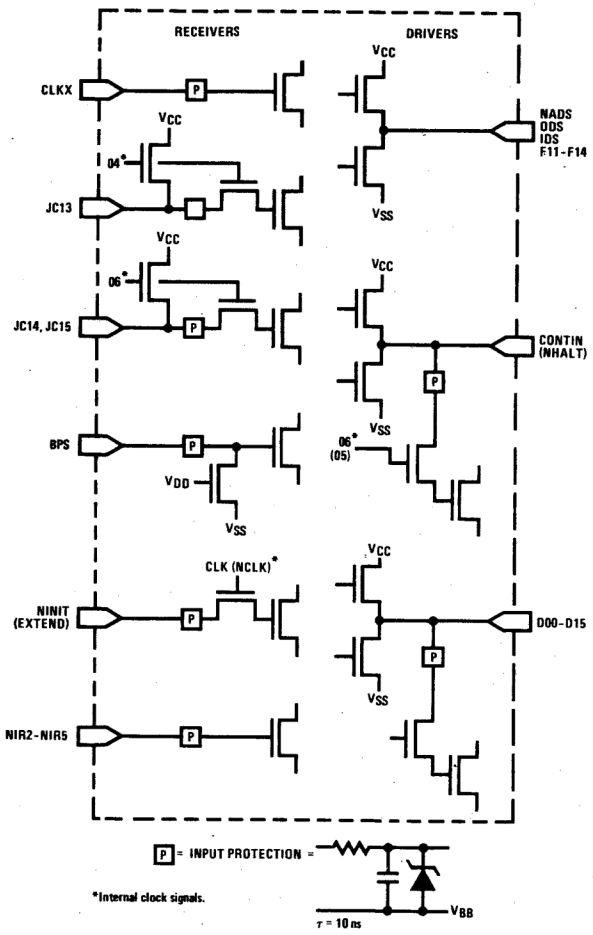


Figure 12. INS8900 Driver and Receiver Equivalent Circuits

EXTERNAL CLOCK TIMING

The INS8900 requires a single-phase clock as shown in figure 1. Refer to the electrical characteristics table for timing specifications.

INITIALIZATION

The INS8900 control circuitry may be initialized at any time by use of the NINIT input signal. The effects of the NINIT signal are described under "INS8900 Interface Signal Descriptions." The NINIT signal should always be used to initialize the processor after applying power. The minimum pulse width for NINIT is 8 clock periods (see figure 2). The INS8900 data strobes (NADS, ODS, IDS) are inactive for 16 to 24 clock periods after the trailing edge of the NINIT signal. After the 16 to 24 clock periods, the first NADS signal occurs and the first instruction is accessed from memory location zero.

Note: If the NINIT signal is held low while clock and/or power are first being applied, the NADS and NHALT outputs may have an undefined state for 8 clock periods after the trailing edge of NINIT.

DATA INPUT/OUTPUT OPERATIONS

All data transfers between the INS8900 and external memories or peripheral devices take place over the 16 data lines. These transfers are synchronized by the NADS, IDS, ODS, and EXTEND signals. Timing for address data output is shown in figure 3. Where signal timing is referenced to CLKX, the reference is to valid logic "1" or logic "0" clock levels. Cross-hatched areas indicate uncertainty of output transitions or "don't care" (optional) states for data inputs. Address data becomes valid one clock phase prior to the Address Data Strobe (NADS) and remains valid for one clock phase afterwards. Typically, NADS will be used to strobe the address data into a latch, either internal or external to the memory chips, or to clock decoded peripheral addresses into a flip-flop.

The INS8900 address output drivers assume a high-impedance state during the data input interval as shown in figure 3. The IDS signal may be used to disable output buffers and enable TRI-STATE® input buffers. Increased power supply current may occur during the transition period of the TRI-STATE enable signal, when several devices may be simultaneously enabled. Therefore, good power, ground layout, and bypass filtering practices should be observed. The data lines must be driven to valid input data logic levels by the end of IDS as specified by t_{DS}. TTL devices should actively drive the input to the right logic level. LS devices, for example, will drive the input to 2.7 V for a logic "1" level. Typically, this data input timing will allow operation of the microprocessor in a system at maximum speed if the access time of the system memory is less than 2 clock periods. For memories with longer access times, the clock frequency may be reduced or the I/O cycle extend feature may be used, as described below.

Data output timing is shown in figure 4. Output data becomes valid at the leading edge of ODS and remains valid for one clock period following the trailing edge. The Output Data Strobe is typically used as a read-write signal for memory and an output data latch strobe for peripheral interfaces.

For systems utilizing memories with access times greater than 2 clock periods it may be desirable to use the EXTEND input to lengthen the I/O cycle by multiples of the clock period. Timing for this is shown in figure 5. In the case of either input or output operations, the extend should be brought true prior to the end of clock phase 6. The timing shown in figure 5 will provide the minimum extend of one clock period. Holding EXTEND true for n additional clock periods will cause an extension of n+1 clock periods.

In DMA or multiprocessor systems it may be desirable to prevent I/O operations by the INS8900 when the bus is in use by another device. This may be done immediately following an IDS or ODS signal (a data I/O operation) as shown in figure 6 or at any clock phase 6 regardless of whether a data I/O operation is in progress (as shown in figure 5).

INSTRUCTION SUMMARY

The instruction set is divided into eight instruction classes as listed in table 3. The branch instructions provide the means to transfer control anywhere in the 16-bit addressing space. Conditional branches are effected using the BOC instruction, which allows testing any one of 16 conditions, including status flags, the contents of AC0, and user inputs to the chip. Additional testing capability is provided by the skip instructions, which provide memory or peripheral to register comparisons without altering data. The memory data transfer instructions provide data transfers between the accumulators and memory or peripheral devices. The load with sign extended is provided to convert 8-bit twos complement data to 16-bit data, allowing 16-bit address modification when the 8-bit data length has been selected.

The memory data operate instructions provide operations between the principal working register (AC0) and memory or peripheral data. This includes both binary and BCD arithmetic instructions. The register data transfer instructions provide a very complete set of transfer possibilities between the accumulators, flag register, and stack, and include the capability to load immediate data. Register data operate instructions provide logical and arithmetic operations between any two accumulators. They may be used for address and data modification and to reduce the number of (time-consuming) memory references in a program. The shift and rotate instructions allow 8 different operations which are useful for multiply, divide, bit scanning, and serial input/output operations. The miscellaneous instructions include the capability to set or reset (pulse) any of the 16 bits of the status flag register individually.

The power of the instruction set is further enhanced by a flexible memory addressing scheme that provides three floating memory pages and one fixed page of 256 words each. Instructions which use both direct and indirect memory addressing are included in the instruction set. Three modes of direct memory addressing are available: base page, program counter relative, and index register relative. The direct addressing modes available are summarized in table 2. The mode of addressing is specified by the XR field of the instruction shown in the "Instruction Format" column of table 3.

Indirect addressing consists of first establishing an address in the same fashion as with direct addressing (by either the base page, relative to PC, or indexed [relative to AC2 or AC3] mode). The 16-bit contents of the memory location at this address is then used as the address of the operand, allowing any memory location to be addressed. The Branch Conditions of the INS8900 are listed in table 4 and the Status and Control Flags are listed in table 5.

Table 2. Direct Addressing Modes

XR Field	Addressing Mode	Effective Address
00	Base Page	EA = disp
01	Program Counter Relative	EA = disp + (PC)
10	AC2 Relative (indexed)	EA = disp + (AC2)
11	AC3 Relative (indexed)	EA = disp + (AC3)

Note 1: For base page addressing, disp is positive and in the range of 000 to 255 if BPS = 0, and is a signed number in the range of −128 to +127 if BPS = 1.

Note 2: For relative addressing, disp has a range of −128 to +127.

INS8900 BUFFERED SYSTEM

A block diagram of a fully buffered INS8900 system is illustrated in figure 13. Detailed schematics of the buffered INS8900 Microprocessor, Clock Generator, and Initialize Circuit are illustrated in figures 14, 15, and 16, respectively. The circuits as shown constitute a fully operational CPU module that can be used as the basis for a variety of systems regardless of their application.

NOTE

A 2.0 MHz crystal (Part No. NS209, Package Type HC-6U) for use with the INS8900 may be obtained from:

Electro Dynamics
5625 Foxridge
Shawnee Mission, Kansas 66201
(913) 262-2500

Table 3. INS8900 Instruction Summary

Mnemonic	Meaning	Operation	Maximum Execution Time (Note)	Instruction Format
1. Branch Instructions				
BOC	Branch On Condition (Table 4)	(PC) ← (PC) + disp if cc true	5M + E_R + 1M if branch	0 1 0 0 | cc | disp
JMP	Jump	(PC) ← EA	4M + E_R	0 0 0 1 1 0 | xr
JMP@	Jump Indirect	(PC) ← (EA)	4M + 2E_R	1 0 0 1 1 0 |
JSR	Jump To Subroutine	(STK) ← (PC), (PC) ← EA	5M + E_R	0 0 0 1 0 1 |
JSR@	Jump To Subroutine Indirect	(STK) ← (PC), (PC) ← (EA)	5M + 2E_R	1 0 0 1 0 1 |
RTS	Return from Subroutine	(PC) ← (STK) + disp	5M + E_R	1 0 0 0 0 0 | 0 0
RTI	Return from Interrupt	(PC) ← (STK) + disp, IEN = 1	6M + E_R	0 1 1 1 1 1 | 0 0
2. Skip Instructions				
SKNE	Skip if Not Equal	If (ACr) ≠ (EA), (PC) ← (PC) + 1	5M + 2E_R + 1M if skip	1 1 1 1 r | xr | disp
SKG	Skip if Greater	If (AC0) > (EA), (PC) ← (PC) + 1	7M + 2E_R + 1M if skip	1 0 0 1 1 1 |
SKAZ	Skip if And is Zero	If [(AC0) ∧ (EA)] = 0, (PC) ← (PC) + 1	5M + 2E_R + 1M if skip	1 0 1 1 1 0 |
ISZ	Increment and Skip if Zero	(EA) ← (EA) + 1, if (EA) = 0, (PC) ← (PC) + 1	7M + 2E_R + E_W + 1M if skip	1 0 0 0 1 1 |
DSZ	Decrement and Skip if Zero	(EA) ← (EA) − 1, if (EA) = 0, (PC) ← (PC) + 1	7M + 2E_R + E_W + 1M if skip	1 0 1 0 1 1 |
AISZ	Add Immediate, Skip if Zero	(ACr) ← (ACr) + disp, if (ACr) = 0, (PC) ← (PC) + 1	5M + E_R + 1M if skip	0 1 1 1 1 0 | r
3. Memory Data Transfer Instructions				
LD	Load	(ACr) ← (EA)	4M + 2E_R	1 1 0 0 r | xr | disp
LD@	Load Indirect	(AC0) ← ((EA))	5M + 3E_R	1 0 1 0 0 0 |
ST	Store	(EA) ← (ACr)	4M + E_R + E_W	1 1 0 1 r |
ST@	Store Indirect	((EA)) ← (AC0)	4M + 2E_R + E_W	1 0 1 1 0 0 |
LSEX	Load With Sign Extended	(AC0) ← (EA) bit 7 extended	4M + 2E_R	1 0 1 1 1 1 |
4. Memory Data Operate Instructions				
AND	And	(AC0) ← (AC0) ∧ (EA)	4M + 2E_R	1 0 1 0 1 0 | xr | disp
OR	Or	(AC0) ← (AC0) ∨ (EA)	4M + 2E_R	1 0 1 0 0 1 |
ADD	Add	(ACr) ← (ACr) + (EA), OV, CY	4M + 2E_R	1 1 1 0 r |
SUBB	Subtract with Borrow	(AC0) ← (AC0) + ~ (EA) + (CY), OV, CY	4M + 2E_R	1 0 0 1 0 0 |
DECA	Decimal Add	(AC0) ← (AC0) $+_{10}$ (EA) $+_{10}$ (CY), OV, CY	7M + 2E_R	1 0 0 0 1 0 |
5. Register Data Transfer Instructions				
LI	Load Immediate	(ACr) ← disp	4M + E_R	0 1 0 1 0 0 | r | disp
RCPY	Register Copy	(ACdr) ← (ACsr)	4M + E_R	0 1 0 1 1 1 | dr | sr | 000 000
RXCH	Register Exchange	(ACdr) ← (ACsr), (ACsr) ← (ACdr)	6M + E_R	0 1 1 0 1 1 | dr | sr
XCHRS	Exchange Register and Stack	(STK) ← (ACr), (ACr) ← (STK)	6M + E_R	0 0 0 1 1 1 | r | 0 0
CFR	Copy Flags Into Register	(ACr) ← (FR)	4M + E_R	0 0 0 0 0 1 |
CRF	Copy Register Into Flags	(FR) ← (ACr)	4M + E_R	0 0 0 0 1 0 |
PUSH	Push Register Onto Stack	(STK) ← (ACr)	4M + E_R	0 1 1 0 0 0 |
PULL	Pull Stack Into Register	(ACr) ← (STK)	4M + E_R	0 1 1 0 0 1 |
PUSHF	Push Flags Onto Stack	(STK) ← (FR)	4M + E_R	0 0 0 0 1 1 | 0 0
PULLF	Pull Stack Into Flags	(FR) ← (STK)	4M + E_R	0 0 0 1 0 0 | 0 0
6. Register Data Operate Instructions				
RADD	Register Add	(ACdr) ← (ACdr) + (ACsr), OV, CY	4M + E_R	0 1 1 0 1 0 | dr | sr | 000 000
RADC	Register Add With Carry	(ACdr) ← (ACdr) + (ACsr) + (CY), OV, CY	4M + E_R	0 1 1 1 0 1 |
RAND	Register And	(ACdr) ← (ACdr) ∧ (ACsr)	4M + E_R	0 1 0 1 0 1 |
RXOR	Register Exclusive OR	(ACdr) ← (ACdr) ⊻ (ACsr)	4M + E_R	0 1 0 1 1 0 |
CAI	Complement and Add Immediate	(ACr) ← ~ (ACr) + disp	5M + E_R	0 1 1 1 0 0 | r | disp
7. Shift And Rotate Instructions				
SHL	Shift Left	(ACr) ← (ACr) shifted left n places, w/wo link	(5 + 3n) M + E_R, n = 1 – 127; 6M + E_R, n = 0	0 0 1 0 1 0 | r | n | ℓ
SHR	Shift Right	(ACr) ← (ACr) shifted right n places, w/wo link		0 0 1 0 1 1 |
ROL	Rotate Left	(ACr) ← (ACr) rotated left n places, w/wo link		0 0 1 0 0 0 |
ROR	Rotate Right	(ACr) ← (ACr) rotated right n places, w/wo link		0 0 1 0 0 1 |
8. Miscellaneous Instructions				
HALT	Halt	Halt		0 0 0 0 0 0 0 0 | 0 | 0000000
SFLG	Set Flag (Table 5)	(FR)$_{fc}$ ← 1	5M + E_R	0 0 1 1 | fc | 1
PFLG	Pulse Flag (Table 5)	(FR)$_{fc}$ ← 1, (FR)$_{fc}$ ← 0	6M + E_R	0 0 1 1 | fc | 0
NOP	No Operation	(PC) ← (PC) + 1	4M + E_R	0 1 0 1 1 1 0 0 | 0

Note: M = Machine cycle time = 4 clock periods
n = number of shifts
E_R = Extend time for read cycle
E_W = Extend time for write cycle
External interrupt response time is 7M + E_R plus time to finish current instruction.

Table 4. Branch Conditions

Number	Mnemonic	Condition
0	STFL	Stack full
1	REQ0	(AC0) equal to zero(1)
2	PSIGN	(AC0) has positive sign(2)
3	BIT 0	Bit 0 of AC0 true
4	BIT 1	Bit 1 of AC0 true
5	NREQ0	(AC0) is non-zero(1)
6	BIT 2	Bit 2 AC0 is true
7	CONTIN	CONTIN (continue) input is true
8	LINK	LINK is true
9	IEN	IEN is true
10	CARRY	CARRY is true
11	NSIGN	(AC0) has negative sign(2)
12	OVF	OVF is true
13	JC13	JC13 input is true
14	JC14	JC14 input is true
15	JC15	JC15 input is true

Note 1: If the selected data length is 8 bits, only bits 0-7 of AC0 are tested.
Note 2: Bit 7 is the sign bit (instead of bit 15) if the selected data length is 8 bits.

Table 5. Status and Control Flags

Register Bit	Flag Name	Function
0	"1"	Not used—always logic 1
1	IE1	Interrupt Enable Level 1
2	IE2	Interrupt Enable Level 2
3	IE3	Interrupt Enable Level 3
4	IE4	Interrupt Enable Level 4
5	IE5	Interrupt Enable Level 5
6	OVF	Overflow
7	CRY	Carry
8	LINK	Link
9	IEN	Master Interrupt Enable
10	BYTE	8-bit data length
11	F11	Flag 11
12	F12	Flag 12
13	F13	Flag 13
14	F14	Flag 14
15	"1"	Always logic 1, set for Interrupt 0 exit

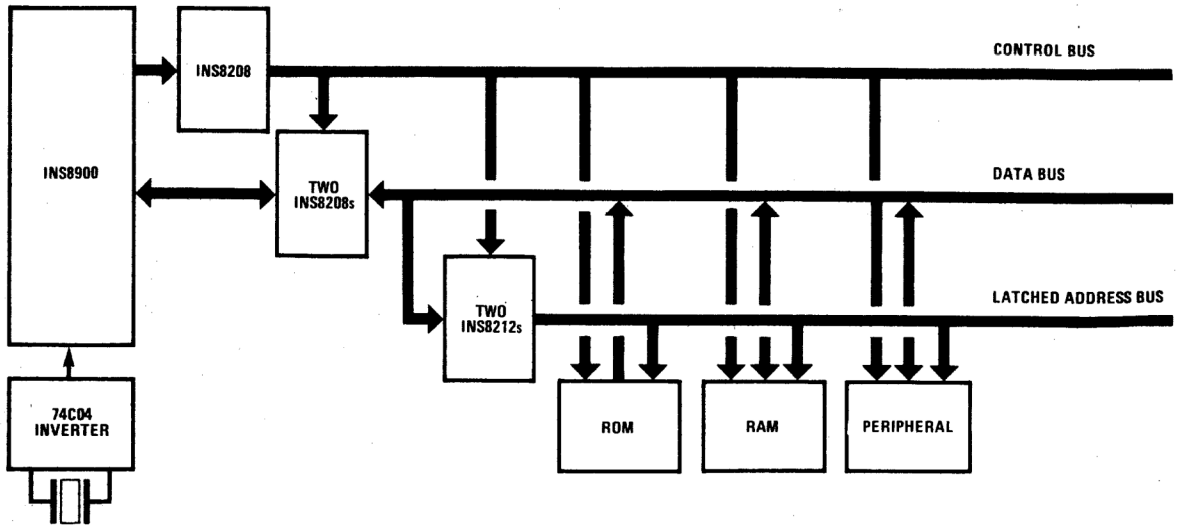


Figure 13. Fully Buffered INS8900 System

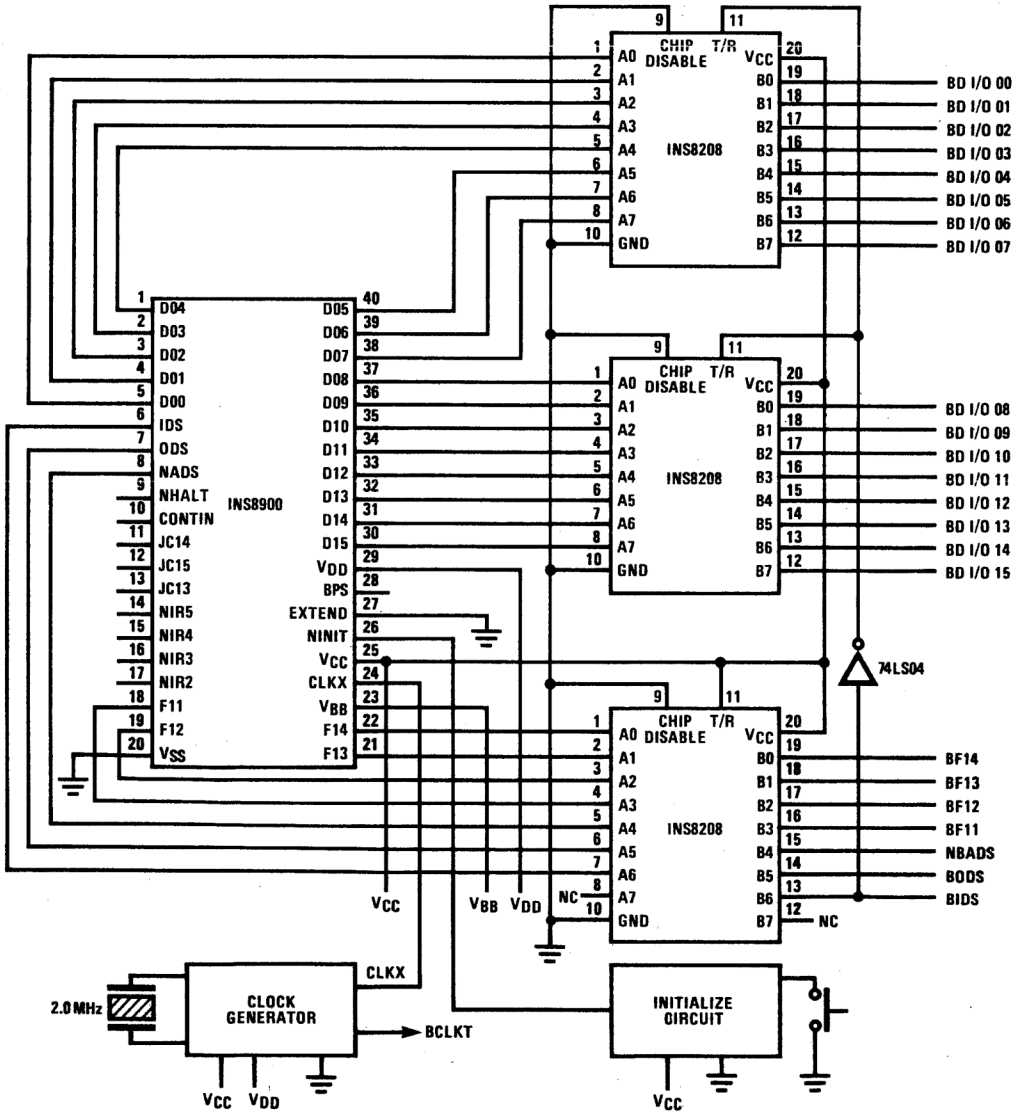


Figure 14. Fully Buffered INS8900 CPU Module

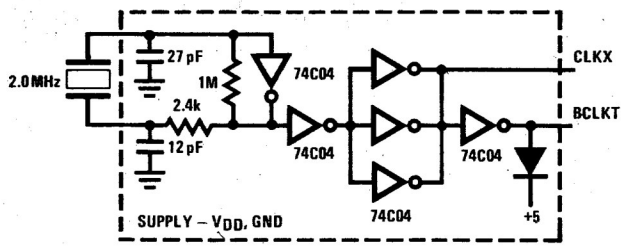


Figure 15. Clock Generator

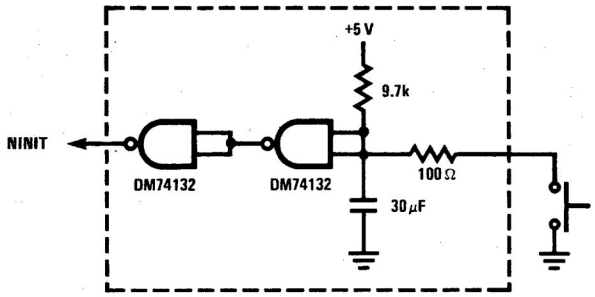
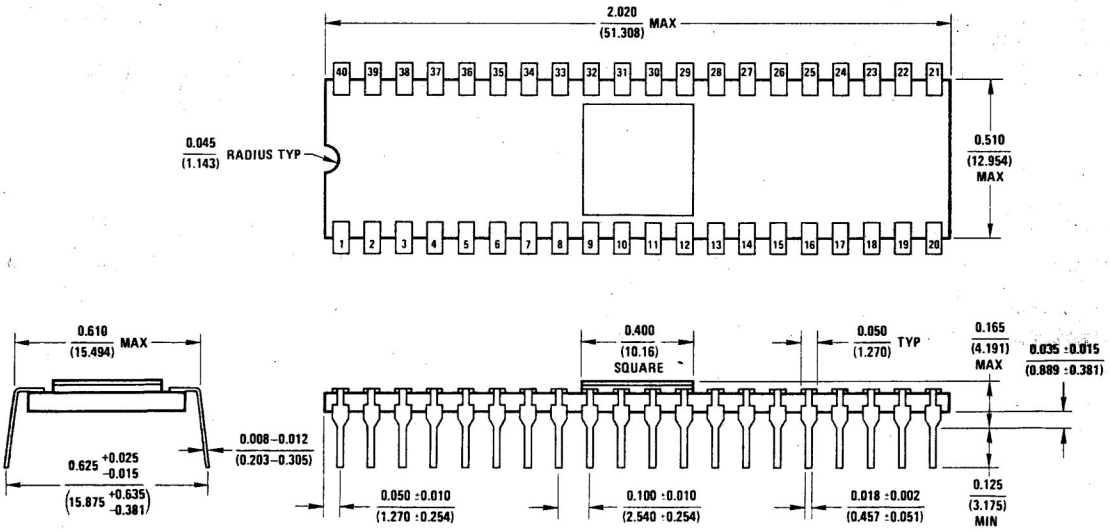


Figure 16. Initialize Circuit

Physical Dimensions



Cavity Dual-In-Line Package (D)
Order Number INS8900D
NS Package D40D

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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