SILICON DESTINY

THE STORY OF APPLICATION SPECIFIC INTEGRATED CIRCUITS AND LSI LOGIC CORPORATION

ROB WALKER
WITH NANCY TERSINI

In SILICON DESTINY, Rob Walker and other semiconductor pioneers tell the story of application specific integrated circuits (ASICs), and the emergence of the U.S. leader in ASICs, LSI Logic Corporation. As an electronic engineer and one of the founders of LSI Logic, Rob Walker is in a unique position to chronicle the history of Silicon Valley from the sixties to the present.

SILICON DESTINY is an oral history told in the words of the principals who created the ASIC industry. Wilf Corrigan recounts the threat and opportunity posed by Japan; Jim Koford describes the genesis of the modern ASIC computer-aided design; K.K. Yawata tells of the anguish of leaving lifetime employment at NEC for an American-based Japanese start-up; and Tsuyoshi Kawanishi, Senior Executive Vice President of Toshiba, describes the pluses and minuses of dealing with a U.S. start-up. In addition, Joe Costello shares his secrets of successful CAE mergers, and Doug Fairbairn shares his vision of the future of design automation.

Of course, we also learn from setbacks. Jack Carsten tells of the technical and business factors that derailed mighty Intel's ASIC program and Carver Mead describes his disappointment with the commercialization of his silicon compiler concept.

SILICON DESTINY, with its emphasis on ASIC silicon and software technology, is a valuable resource to the semiconductor, electronic, and computer communities. Venture capitalists and financial followers of the high tech scene will find the details of venture capital and Initial Public Offerings quite insightful. Finally, SILICON DESTINY offers a behind-the-scenes glimpse of what really goes on in Silicon Valley told in the words of the entrepreneurs who have contributed so much to our society.

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To the memory of my mother, Bernice Irene Walker,
who gave all the Walker kids her moral integrity,
sense of worth, and unqualified love.

LSI Logic could never have succeeded without the dedication of its people, now numbering more than 4,000 worldwide. They are fully prepared to take on the best of Japan, America and Europe, and prevail.

I'd like to express my appreciation to all the industry veterans who agreed to recount the story of the ASICs phenomenon; their words are the heart of this book.

In addition, I want to recognize the support of those who encouraged me in this project and made many valuable suggestions. I especially want to thank Susan Ayers, Sandra Byers, Mick Bohn, Julie Chen, Darlene Foster, Jim Koford, Nancy Petersilge, and Sally Wicker.

Kudos go to Pat Zolotar and Jeanne Kasper for the transcribing and typing, and to Larry Bender for the design.

SILICON DESTINY could not have been completed without the help of my friend and collaborator, Nancy Tersini, who translated chip technospeak into English.

Finally, my gratitude to Wilf Corrigan. He provided the vehicle for us to fulfill our destiny.

SILICON DESTINY tells the story of Application Specific Integrated Circuits (ASICs), a high-growth semiconductor industry. It is also the story of LSI Logic Corporation, the ASIC leader, and other organizations such as VLSI Technology, Altera, and Cadence Design Systems.

It is an oral history told in the words of the principals who created the ASIC industry. Wilf Corrigan recounts the threat and opportunity posed by Japan; Jim Koford describes the genesis of the modern ASIC Computer Aided Design System; K.K. Yawata describes the anguish of leaving lifetime employment at NEC for an American-based Japanese start-up; and Tsuyoshi Kawanishi, Senior Executive Vice President of Toshiba, describes the pluses and minuses of dealing with a U.S. start-up. In addition, Joe Costello shares his secrets of successful CAE mergers and Doug Fairbairn shares his vision of the future of design automation.

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I first started in ASICs in 1967, and in 1981 I was one of the founders of LSI Logic Corporation, now a Fortune 500 multinational semiconductor leader. I wrote this book for the

following reasons:

1. Application Specific Integrated Circuits is a seminal technology with estimated worldwide sales of $6.6 billion in 1991. Its real story has never been told.
2. LSI Logic operations in Silicon Valley, Europe, Japan, and Canada have all been uniquely financed, mainly with indigenous money. I wanted to document the innovative financing that LSI Logic has used.
3. LSI Logic's four closest ASIC competitors are Japanese. Competing with them worldwide and, most importantly, in Japan, LSI has used every available strategy–initiating joint ventures, recruiting top Japanese management, keeping a long-range view (including heavy R&D investment) and encouraging the U.S. government to keep a level playing field. The LSI experience may show America how to keep its competitive edge.
4. Finally, Bob Noyce's recent death made all of us aware of our mortality. Co-founder of Fairchild and Intel, and co-inventor of the integrated circuit, Bob was a vibrant man and a hero to us all. The pioneers of Silicon Valley are now in their fifties and sixties; we had better tell our story while we can.

I graduated from Cal Berkeley in 1958, the same year the integrated circuit was invented. I started using ICs in 1965 and began my ASIC career in 1967. Over the last 20 years, I've watched the technology evolve from dream to mainstream. I didn't realize it, but for most of my professional career, I had been preparing myself to be a founder of LSI Logic. Hence the title SILICON DESTINY.

SILICON DESTINY is based on interviews done in 1991 and the first quarter of 1992 which have been edited for focus and readability. A glossary provided at the back defines key words and terms.

Rob Walker
Atherton, California
1992

A DREAM COME TRUE

1 LSI Goes Public

Friday, May 13, 1983, when LSI Logic Corporation went public, was probably the most significant day in the lives of those involved. LSI had proved its many critics wrong; the company was a success. Many of the LSI principals had worked their hearts out in the late sixties and early seventies to make custom ICs (now called application specific integrated circuits or ASICs) a commercial success. They failed, and figured their shot at the title was gone. Nine years later, fate gave them a second chance in the form of LSI Logic.

More than one so-called expert counted LSI out almost immediately. The four founders were middle-aged, 10 to 15 years older than those of a typical high tech start-up. LSI was committed to many politically incorrect technologies–CMOS, gate arrays, and proprietary computer-aided design using IBM mainframes. Despite the skeptics, LSI persevered, grew rapidly, and, on Friday the thirteenth, went public. Destiny had been fulfilled.

WILF CORRIGAN

The Initial Public Offering (IPO) marketplace was so unpredictable that we decided we couldn't control when the opportunity would occur. So we had a strategy during 1982 to be ready to go public when high tech IPOs came back into fashion. Even

though we had started LSI Logic primarily as an engineering company, I always felt that we could never be really big unless we manufactured our own wafers. The major customers wouldn't qualify us unless we had our own leading-edge manufacturing capability. I knew that at some point we'd have to build our own factory and do our own wafer-processing R&D which would require big capital investments. We knew that if we were going to make the next step and become a major semiconductor supplier, we needed to raise lots of money, and that meant the public market.

Throughout 1982, we kept our books in order so that we were ready to act. Our target was to get the company profitable and to demonstrate a steady growth of revenues. Normally, you'd expect to need to demonstrate two or three quarters of profitability before you can take a company public, but we decided to position ourselves to be ready if the opportunity presented itself.

Late in 1982, the market for IPOs suddenly got hot and we observed a number of other companies successfully going public. In the first quarter it looked as if the window had arrived. We had $5 million in revenues in 1982, and our target was to do $5 million in the first quarter of 1983, make a profit and go public in the second quarter. We got Morgan Stanley and Hambrecht & Quist to handle the IPO. I remember one particular meeting with several of the directors and Bill Hambrecht. I said, "I think we should go now." VLSI had just gone public in February and several other local companies had just gone out. Bill Hambrecht replied, "Well, the ducks are quacking."

Although I didn't want to seem ignorant about what this meant, I asked, "Bill, forgive me, but what do you mean, `the ducks are quacking'?" "Well," he said, "they're quacking because they want food. The market demands new offerings. There's a

huge demand out there and there isn't enough product to supply the high tech market. I agree with you, now is the time." Our board was reluctant–I think it was Don Valentine and Tom Perkins who suggested we wait a quarter. But my feeling was that things could radically change in three months. Finally everyone agreed to a second-quarter 1983 IPO.

I spent a lot of time keeping the lawyers and the investment bankers happy and talking to each other. Finally we got the IPO all together and we were doing the prospectus amendments on the fly. Throughout the previous week, we'd done the road show which seemed to go pretty well.

We always took our own projector and slides for the road show because we couldn't trust the investment bankers to have everything set to go. "It's all wired, you just walk in the room, you press the button and go," they would say. But sure enough, everywhere we went, their advance guy had screwed up and the projector wouldn't work, or there wouldn't be the right bulb or, in European hotels, the voltage was wrong.

The road show was always the same: an hour here, run and grab a plane, get to the new location, and do another presentation. In a typical day, we'd start in the morning from New York, then we'd go to Boston, then Chicago, and by evening we land in Los Angeles.

The investment bankers were out creating market demand for the stock. They would ask an investor how many shares he would take at $27, to see what demand there was. If demand was low, they would try $25. The institutions (the quacking ducks) still felt the price was high, but were worried that if they acted too slowly they wouldn't get a piece of the action. The SEC was supposed to approve the deal Monday, May 9, 1983. The investment bankers had whipped demand to a frenzy; our offering was three times oversubscribed.

MICK BOHN

Before we started our U.S. road show, I met with Wilf and Bill O'Meara at the 21 Club in New York. Over dinner, I told Wilf and Bill how I thought we could turn our public offering into at least $150 million. At the time, our preliminary prospectus proposed something like four million shares at $14 to $16 each, corresponding to a $60-$75 million IPO. I thought that if we went out and sold the deal ourselves rather than sit back and let the investment bankers carry it, we could increase interest in the offering. The demand would then be so large that it could only be satisfied by raising the price and doubling the number of shares sold. If we could get $20 a share, increase the shares from four to seven million and then sell the shoe–the 10 percent demand override on which investment bankers always have an option–we would end up selling something like 7.7 million shares, bringing in more than $150 million. Wilf and Bill were skeptical that we could bring in that much.

Market conditions were right and we sold the hell out of the deal. We had good book demand–at one time, we had orders for over 22 million shares for our proposed offering of four million shares. Our biggest problem was getting the SEC's approval for going public because they knew that the IPO was around $160 million and thought it highly speculative. LSI revenue the previous year, 1982, was just under $5 million. In the first quarter of 1983, revenues reached $5 million. I remember flying on Mike Markkula's private jet overnight early that week to Washington, D.C. to convince the SEC that we were legitimate; the input we were getting from Morgan Stanley was that the market was just about at its peak and they were afraid that it was going to crash at any time. I spent days and nights at the SEC and, in fact, from Wednesday morning to Friday night I got no sleep.

The SEC had a rule that they wouldn't let a principal of the company actually see the people who were reviewing the deal.

You communicated with them by telephone and by paperwork in their lobby. I think I was the only principal who actually got to go upstairs and meet the reviewers to encourage them to act on the offering. The SEC was obviously wary, and kept coming up with more questions; they were afraid that some security shyster might be behind one of our investment groups, and they didn't want to be embarrassed by it all collapsing. I had to call England Friday morning to find out details on some of our investors.

WILF CORRIGAN

We had planned to come out on Monday, May 9, but problems at the SEC stretched the approval process to Tuesday. Some of the investors who had committed the previous week were starting to drop out with comments like, "Hey, I think there is something wrong with this deal." We brought the price down to $23 and then it was delayed yet another day. Mick parked himself in the lobby of the SEC and stayed glued to a pay telephone trying to hold the deal together.

Meanwhile the IPO looked like it was collapsing; really it wasn't, but there was some crumbling going on at the edges. The investment bankers were getting nervous because they were getting all the heat from the customers and they decided to blame the lawyers. Friday, May 13, we finally got out, but if we had been able to go on Monday at $25 a share, we would have raised $40 million more.

MICK BOHN

We got final approval from the SEC just minutes before the 10 a.m. East Coast stock market opening. By noon, the seven million shares were sold. At 12:15, I persuaded Morgan Stanley to sell the shoe since the demand and the price were holding up. They took the last 700,000 shares for a total offering of 7,700,000. We went public at $21, raising a total of $161.7 million gross, out of which we netted $152,306,000.

ROB WALKER

I got the call at 7:00 a.m., Friday, May 13, 1983. It was my boss, Wilf Corrigan, CEO of LSI Logic. "We're going out today; I just talked to Mick and the SEC has finally approved the public offering."

The dream of every Silicon Valley engineer had come true for us. Two years and three months after founding LSI Logic we had gone public and some of us were millionaires, at least on paper. At the office there was a feeling of excitement; virtually every employee had stock or stock options. Not a lot got accomplished that morning, and at lunch a group of us went to the Weibel Winery. Sitting outdoors at picnic tables, we sprayed each other with champagne. Someone started kissing the secretaries. I believe it was me.

That evening Keith Lobo, his wife Susan, and my girlfriend Dotti and I had a quiet dinner at the Adriatic, a charming European restaurant in Saratoga. By that time we were emotionally drained, so we split up early and headed home. Quite a day.

BILL O'MEARA

On our going-public day, I had to meet with four or five customers so I wasn't able to goof off like Rob, but I stepped out of the meetings from time to time to check on how the offering was progressing. By evening, I was so beat that I went straight home, shared some champagne with my wife Joyce, and crashed.

MICK BOHN

I flew back to California and landed at San Jose Airport about 5:00 p.m. I got to my car and thought, "I'll take my stuff to the office and chat with some of the guys." When I got to the office nobody was there, not a single soul. Talk about feeling alone–I knew all those bastards were out celebrating, and so I just went on home to bed. We were a public company!

WILF CORRIGAN

If we had waited another quarter I don't think we'd have been able to go out at that price or that amount. That was very important because we did raise $160 million which meant that we could start acting like a large company.

HISTORICAL PERSPECTIVE

2 ASICs– The Untold Story of Silicon Valley

ASICs are one of the hottest products in the semiconductor industry. In-Stat, the Scottsdale market research firm, estimates that in 1990 ASIC sales were $5.8 billion and that by 1995 the worldwide ASIC market will reach $13.2 billion. Many of the innovations of ASIC technology and its associated CAD (computer-aided design) tools came out of Silicon Valley, but surprisingly, there is virtually no mention of ASIC or CAD in historical accounts of Silicon Valley.

ROB WALKER

In 1966, Fairchild Semiconductor was flying high. Simple digital and analog integrated circuits (ICs) were shipped to customers at handsome prices with high profitability. Computers and digital systems of the day were made up of thousands of IC building blocks of just a few part types. The first logic IC line known as RTL (resistor-transistor logic) was still in volume production and a new, higher performance DTL (diode-transistor logic) IC family was just being introduced.

The number of resistor, diode, and transistor components (called "complexity") that could economically be put on a chip in 1966 was about 20. Dr. Gordon Moore, who was then in charge of Fairchild R&D, postulated that the number of components on an IC could double every year to 18 months. This later became known as "Moore's law."

At Fairchild, the ramifications of continually increasing levels of integration were disturbing. As the single logic block

(small-scale integration, or SSI) gave way to higher-complexity blocks, specialization would increase, and manufacturing volume of a specific circuit would decrease.

For example, simple SSI flip-flops could be hooked together to build a counter, shift register, or a state machine. To increase complexity, you had to uniquely configure circuits with multiple flip-flops as counters, shift registers or state machines that would cause the number of unique part types to climb, and, at the same time, reduce the production quantity of each part type. In other words, Moore's law meant that the existing product line of a few simple, high-volume, standard ICs would be replaced by many specialized, low-volume, medium and high-complexity ICs. Recognizing that this would mean a fundamental change in Fairchild's way of doing business, Moore assembled a team to prepare for the custom IC revolution.

Many unique designs would require developing more effective design techniques. In 1966 there were no commercially available computer-aided design (CAD) or computer-aided engineering (CAE) tools; that expertise was to be found only at a few universities and major computer manufacturers. A group of CAD specialists were recruited: Hugh Mays, Jim Koford, and Ed Jones–all Stanford Ph.D.s.

JIM KOFORD

When I was in graduate school at Stanford, Dr. Bernard Woodrow ran the adaptive systems laboratory where we worked on circuits later called "neural nets." On that project were a number of people who became well known, Paul Low who later ran IBM's semiconductor manufacturing operation; Ed Jones and Hugh Mays, who later became my associates at Fairchild; and the microprocessor inventor, Ted Hoff. As the circuit designer *par excellence* in the lab, Ted began to use transistors from a new company called Fairchild.

After I completed my Ph.D., I joined the IBM Design Automation Group in upstate New York where I got authorization for a project using graphics for computer-aided design. We didn't call it that at the time, but that is what it was; its purpose was to layout SLT, the small ceramic modules that IBM used to build their computers. The capability was basic: five or six transistors flip-chipped on a ceramic substrate with metalized interconnections and screened resistors and capacitors.

We had a CRT display left over from the SAGE Project. I built interface logic to an IBM 1620 computer, and designed a light pen and Calcomp plotter interface and a special cutting head for the Calcomp to allow us to make rubylith masks for the ceramic modules. The system had graphical input, screen menus, schematic capture and graphical output. I've often wondered if my system was the world's first workstation. I gave a paper on it in San Francisco at the 1965 Fall Joint Computer Conference.

Even though I had really enjoyed my IBM experience, I decided that I wanted to get back to California. Hugh Mays had gone to IBM just before me and had been recruited by Fairchild as the manager of computer-aided design. In the summer of 1966, I became the first employee in his group at Fairchild's Palo Alto R&D lab. Fairchild was a wonderful place because all the big names of Silicon Valley were there. Bob Noyce was President, Gordon Moore ran the R&D lab, Jerry Sanders ran Marketing, and Charlie Spork served as General Manager.

At Fairchild, we were trying to plan a CAD environment, and I came across a paper by Robert Ulrich at North American Aviation that detailed what has become the core simulation algorithm for logic simulators. That concept was what I needed to crystallize my thoughts. If we could simulate the logic of a digital logic chip, then why not take the database from the

simulation (which now described the correct logic network interconnections) and feed that into an automated system to layout the chip and give us a totally integrated design package.

From 1967 to 1969, Hugh Mays, Ed Jones, and I formulated the concept of integrated CAD and implemented our first system. I did the input language, the logic simulator and the netlister. Ed handled the early test programs and, ultimately, the layout system. Henry Sun, Ralph Bestock, Danielle Boaudvey, Pete Jacobsen, Linda Verdooven, and Bill Jenson also soon joined the Fairchild CAD group. Rob Walker, who had seen my paper and understood our vision, ran Application Engineering. During this period, Rob created another innovation which we now call design centers or the design factory, an organization which enables customers to create their own chips by interfacing to the software tools with appropriate application support.

ROB WALKER

Gordon Moore knew that to develop complex ICs and computer tools, a knowledge of digital system design was required. So, in 1966, I was recruited from Ford Aerospace, along with Bob Schreiner, Harold Vitale and Jim Downey from GE Computer, and Bob Ulrickson from Lockheed. To support the silicon design, experienced semiconductor designers Les Vadesz and Bob Nevala were assigned to the project from Fairchild R&D. This was the team that largely defined the ASIC structures, methodology, and CAD tools used today.

Our first product, known internally as FMGA, was what we now call a MOS (metal oxide semiconductor) gate array. In 1966, MOS was a revolutionary new semiconductor process. In gate-array form, a regular structure of transistors was prediffused on a "masterslice" of silicon. Two-layer metal was then used to form simple logic functions such as flip-flops and gates and to interconnect the simple logic elements into complex

functions. To the best of my knowledge, FMGA was the first MOS gate array. Unfortunately, the combination of two-layer metal and MOS was an unhappy one, and we never got working parts.

Arrays were also at the forefront of the more mature bipolar semicustom approach. Bob Nevala designed a diode-transistor logic (DTL) array known as the 4500 which provided 32 four-input NAND gates interconnected with two-layer metal. Because the proven bipolar technology was less sensitive to the metalization impurities of the two-layer metal process, the combination provided a viable yield. A number of custom designs, as well as several standard products, were implemented on the 4500 masterslice.

In 1967, CAD at Fairchild was progressing well. An event-driven logic simulator written by Jim Koford and known as "FAIRSIM" was debugged on customer 4500 designs. Auto-place and auto-route layout programs were being developed by Ed Jones. I specified 24 and 36-pin DIPS which at that time were considered high pin-count packages, and I modified a Fairchild Series 4000 20-pin tester to handle them.

The bipolar array family was enhanced with two new transistor-transistor logic (TTL) masterslices: the 4600 provided 48-gate complexity and the 4700, 96-gate complexity. A number of customer designs were implemented; yields were modest but viable. The 4700 was the last bipolar array from Fairchild until the ECL arrays of the late seventies. Bob Nevala was reassigned to bipolar RAMS, where the high performance of two-layer metal and bipolar technology translated directly to high-volume, high-margin business.

Meanwhile, the MOS group was busy inventing what is now known as standard cell. Since the weak link in the FMGA had been the two-layer metal, we needed a way to interconnect an IC with one layer of metal. That was easy. The standard

MOS IC process of the day utilized interconnections of metal for one layer and diffusion for the other. If the custom IC was fabricated from scratch, one-layer metal and one-layer diffusion could be used for interconnection. The result, which we named Micromosaic, had all of the attributes of a modern standard-cell design. Several were completed and yields were good, so we decided to take it to market.

Most of the development team moved out of the Palo Alto R&D facility to the new corporate headquarters at 464 Ellis Street in Mountain View. Known as the Rusty Bucket for its unpainted weathering steel construction, it stands today as an empty monument to toxic waste. Bob Ulrickson headed Test and Applications; Hugh Mays, Computer-Aided Design; and Jim Downey, Circuit & Cell Design.

By 1969, our computer tools had become remarkably sophisticated. The FAIRSIM logic simulator provided accurate, event-driven logic simulation with independent rise and fall delays. The simulation-control language was rich with powerful conditional statements. Once logic simulation was complete, layout using interactive and automatic placement and routing proceeded with the output displayed using a Calcomp plotter. As it is today, the layout was checked automatically against the netlist, so the layout was right by construction. Delays were calculated initially using estimated interconnection capacitance. In 1970, Henry Sun wrote an extraction program so that a final simulation using "post layout" delays could be used to verify the design.

At first, the mask artwork was done at 200X using rubylith, a sturdy transparent plastic mylar film covered by a soft, red film. Light areas were obtained by cutting the "ruby" and stripping off the appropriate red portion, then a common IC design technology. For hand-crafted circuits, the cuts were made using Exacto knives and straight edges; for automated layouts, we

replaced the pens in the Calcomp plotters with small, electrically activated knives. The cuts were made under computer control, and the areas were opened by pulling off the red film with tweezers. While the layout was "right by construction," the manual "pick-and-strip" operation was prone to error and required careful human inspection to maintain accuracy.

Punched cards were used for the netlist and SCL entries and a high-speed printer was used for the output. We experimented with CRT graphics terminals, but their million-dollar-plus price tag made them impractical at that time.

In 1969, we purchased one of the first David Mann pattern generators. Ed Jones wrote an optimized fracturing program and we converted to 40X photographic reticles. This was how the famous "PG Tape" was born.

It was apparent that the existing, hard-wired IC testers of the era were inadequate. Maurice O'Shea had made some feasibility studies of what an LSI tester might look like and cost. Bob Schreiner assigned the task of the production tester to Harold Vitale who, in 1970, produced the Fairchild 8000A, the first computer-controlled IC tester. Experience showed the 8000A had some deficiencies; it was redesigned as the 8000B and later became the Fairchild Sentry Series, without question the most successful LSI tester series in Silicon Valley history. Harold eventually left Fairchild and went on to design the Gen Rad and Trillium VLSI testers.

What emerged at Fairchild was the world's first integrated IC computer-aided design system complete with logic simulation, automatic/interactive layout, delay extraction, PG tape generation and close coupling to a computer-controlled tester, an approach closely resembling that used today.

Micromosaic, the Fairchild MOS standard-cell technology, continued to evolve. A different silicon-wafer orientation allowed 5-volt "TTL compatible" signal levels. In 1971, we introduced

silicon-gate Micromosaic with improved performance. Throughout the period, we used PMOS rather than the hot new NMOS technology which the late Bob Seeds was convinced was a blind alley.

At Richard Derickson's insistence, we developed a regular structure which could be embedded in the ASIC for large AND-OR functions, which we called a CLM. In later years, it became known as PLA and became an industry standard. We were also beginning to embed large RAM blocks in the standard cell layouts, so Ed Jones modified the layout program to accept what we now call "Megacells."

Change was brewing in the executive suite at Fairchild. Bob Noyce, Gordon Moore, and Andy Grove, weary of the interference from Fairchild Corporate Headquarters on the East Coast, left to start Intel. The story of how Les Hogan was recruited from Motorola to become president of Fairchild has often been told. Hogan, in turn, recruited dozens of Motorola people (including Wilf Corrigan) to key positions at Fairchild. Motorola sued Fairchild and lost.

At first, Hogan's cadre were favorably impressed with Micromosaic and CAD; both technologies were far more advanced than anything at Motorola. The problem was that Fairchild's MOS Division was losing money. With almost no standard products and the huge overhead of dedicated wafer fab, CAD, engineering, and a multimillion dollar computer, the division could not come close to breakeven. Interestingly enough, my ASIC engineering group was profitable: the Non-Recurring Engineering charges (NRE) more than covered the department's expenses. This up-front money concept was later used to good effect at LSI Logic.

At any rate, Fairchild MOS was losing money and something had to be done. Thus began what we insiders called the "VP-of-the-Year Program," which started with an industry veteran who was recruited to head up the MOS operation. The

new VP began with a flurry of activity: a reorganization, a new lineup of "hoped-for" standard products and the usual speech–"We're going to run MOS like a business." Unfortunately, the PMOS process was not performance competitive for memories, the major MOS standard product of the time. Because of inadequate staffing, the time to develop a new product exceeded the VP's staying power, and he would be replaced, thus beginning a new cycle. Jack Gates, Roy Pollack, Phil Thomas, and Leo Dwork were part of the parade.

Dissatisfaction with Fairchild led Mays, Koford, Jones, and me to approach Noyce and Moore at Intel in April 1971 with a business plan proposing to use Intel's processing, fabrication and assembly capability to support our ASIC start-up. We wanted to call it Intel Systems because the Intel name would give us instant credibility. Our new company would develop the ASIC design, CAD, and the specialized testing for custom devices.

Quoting from our 1971 business plan:

The purpose of this document is to propose a new business opportunity. The general area of proposed business is custom design and manufacturing of electronics devices, subsystems and systems. As a first endeavor, the development and tooling required for custom design, assembly, and test of nonmemory large-scale integrated (LSI) semiconductor products will be provided.

Custom LSI possesses many attractive business opportunities for the 1970s. The lower cost inherent with this technology is forcing many system designers to abandon techniques using standard integrated circuits and convert to LSI. Furthermore, the much lower cost per function obtainable with LSI is opening up entirely new markets in automotive, consumer goods, and control.

A typical customer LSI contract would begin with the analysis of the customer's request for quote (RFQ). A proposal would be made stating technical approach, engineering costs, and production

pricing. After the award of the engineering contract, one or more circuits are designed and verified by computer simulation. Next, mask artwork is designed and prototypes are manufactured; the engineering design charge is payable after prototype shipment. After the customer has received prototypes and verified the entire system, production quantities are ordered.

The advantages of custom LSI as a business venture may be summarized as follows:

- *Engineering charges for custom circuit design paid for by the customer*
- *High average selling prices for delivered products*
- *Sole-source position on many contracts, no worse than second-source on others*

With all the opportunities inherent in this technology, it is not surprising that many small firms are being formed to pursue custom LSI. However, the disadvantages for a small firm are formidable. Here are some major ones:

- *Conventional P-channel metal-gate MOS processes are being superseded with more advanced processes such as silicon-gate, ion-implantation, and N-channel. These new technologies require extensive R&D, characterization, and wafer fabrication.*
- *The sole-source nature of this business makes a customer extremely wary of selecting a new, unproven supplier. Even when design excellence is proven, it must be backed up with known production capability.*
- *For the firm to be competitive, an extensive computer-aided design capability is a must.*
- *After initial engineering contracts are received, an average of nine to twelve months elapse before production orders are received.*
- *The working relationship with each customer is unique.*
- *There are a variety of package types required.*

These hazards are sufficient in our view to cause most emerging firms to fail, and yet the semiconductor giants have unwieldy organizations with a huge stake in traditional technologies and

products. If the dangers are recognized and met, there is tremendous opportunity for an aggressive firm to establish a significant market position in the specialized custom LSI area. We feel that the business plan we are proposing is uniquely suited to succeed.

For the past five years, the principals in the proposed new company have been closely associated with the development and operation of the custom LSI design at Fairchild Semiconductor. This engineering organization has completed over 120 custom LSI designs of generally excellent quality. Problems of wafer fabrication and inconsistent management have limited Fairchild's market penetration to third place behind AMI and North American Microelectronics, but Fairchild's custom LSI design team is unmatched. With respect to a new business opportunity, the conclusion is obvious: a firm that can marry advanced semiconductor and wafer-fabrication technologies with the system-design and CAD expertise will have a clear competitive advantage.

The proposed new company will be associated with Intel Corporation, and it will utilize their semiconductor processes and wafer fabrication to produce nonmemory LSI. Intel has been an industry leader from its inception, and it now has the most advanced semiconductor technology in the industry. This capability is well recognized with LSI customers; Intel has far and away the best reputation in the semiconductor business. Although Intel has never solicited custom business because they have quite rightly chosen to devote all their energies to standard memories, Intel continues to receive large numbers of RFQs in the nonmemory area.

Some of the unique benefits that make the proposed new firm an attractive business venture are:

- *Proven CAD and custom LSI design expertise*
- *A rapidly expanding market for custom LSI*
- *Most large capital expenditures such as wafer-fab production area and R&D equipment are eliminated from the new firm's capitalization.*
- *Intel licensees are available to give the new firm a second-source*

wafer fabrication capability, i.e., all the production eggs are not in one basket.

- *The Intel name opens most doors and means an automatic inclusion on many RFQ lists.*
- *The Intel advanced semiconductor and packaging technology, proven in memories, is available for nonmemory custom designs.*
- *Intel's international field sales force and representatives are excellent and trained in LSI.*

Clearly it is not sufficient that benefits occur only to investors in Intel Systems. The new firm must also look attractive to Intel Corp.:

- *Capitalize on the heavy investments in process R&D required to be the industry leader.*
- *Incremental, multiple shift usage of Intel wafer-fabrication facilities.*
- *Add to Intel's total LSI capability by supporting and complementing the sale of its current standard products.*

Noyce and Moore were interested and offered to invest $1 million if we could get another million from outside investors. Unfortunately, we were unknowns, the venture capital industry was in its infancy, and our proposed Intel Systems didn't happen. It's ironic that when Intel did attempt to enter the ASIC business in the mid-eighties, the barriers to entry were then much higher and the effort turned into a very expensive failure.

Back at Fairchild, throughout the changes in management, customers exerted a stabilizing influence on the ASIC portion of our business. In spite of yet another internal reorganization and a new VP, customers still wanted the same design, thereby saving the Micromosaic group from the chaos of the rest of the organization. Our high point was 1972. We completed 70 designs of which 90 percent were right the first time and the other 10 percent were fixed on the first revision, and we racked

up more than $1 million dollars in NRE, which more than covered our engineering expenses.

Nevertheless, there were clouds on the horizon. The semiconductor industry was sliding into one of its downturns, and every program was under review. A number of factors argued for killing Fairchild's Micromosaic ASIC program:

- The MOS Division continued heavily in the red.
- Custom calculator chips, which made up over half of the Micromosaic business, were being replaced with one-chip standard calculator designs.
- The microprocessor had just been announced by Intel. The conventional wisdom was that it could replace custom ICs.
- Standard MSI/TTL "building blocks" were becoming available. They provided superior system performance to PMOS ASIC, but their $20-per-part price had made them a more expensive solution. In the economic downturn, price reductions quickly brought them down to the $2 range, making them price-competitive to our custom solution.

The Fairchild senior staff decided to shut down the CAD and Micromosaic operation. We all needed to find new jobs.

The statement, "it was ahead of its time," is a cliche, but in this case, an appropriate one. As we struggled to find new careers, it became apparent that the industry did not hold our work in semicustom ICs and design automation in high regard. The consensus was that it was a dumb idea and a dead end. In fact, this image problem is one of the major reasons that until now, ASIC has been the untold story of Silicon Valley. Most of us didn't want to own up to that failed period in our history. The team that had developed ASICs and CAD at Fairchild rewrote their resumes and went into different lines of work.

Regis McKenna and Don Hefler, probably two of the most influential contributors to the Silicon Valley story, didn't help matters any. Regis, of course, is the famous public relations

guru; he made Intel and Apple household words publicizing microcomputers. If he had done the same for ASICs, the story would be known.

The late Don Hefler never gave ASICs much ink in his weekly newsletter, *Microelectronic News*, before the advent of LSI Logic. When he did, what he had to say was all negative because of his longstanding enmity with Wilf Corrigan. He didn't like me any better. He said in his newsletter that "Rob Walker is indicative of the rag-tag nature of LSI Logic." At any rate, the seminal ASIC and CAD work accomplished at Fairchild from 1966 to 1972 became non-history.

By 1973, the major semiconductor players were out of ASIC and CAD. It was left to niche merchant-market and in-house captive suppliers to continue ASIC development. AMI continues to this day to supply small volumes of ASICs. In the late seventies, IBM, Amdahl and Digital Equipment Corporation all had internal bipolar ASIC manufacturing and Motorola and Fairchild had merchant-market bipolar (primarily ECL) ASIC capability.

In the computer-aided design arena, progress was made in graphical systems for IC physical design; Calma, Applicon, and Intergraph all developed computer-controlled systems. In addition, small companies such as NCA and Phoenix Data Systems developed mainframe-based design rule checkers (DRC) and pattern-generator (PG) tape programs. There was surprisingly little interest in logic simulation or automated layout software in the commercial area, although most of the large computer manufacturers had some capability in this technology. In the academic world, the SPICE circuit simulator was developed at UC Berkeley where interest then turned to a variety of layout and synthesis programs.

By 1980, a number of factors made ASICs a potentially commercial proposition:

- Since 1972, computing power, a key element of design

automation, had decreased in cost by an order of magnitude and was clearly destined to continue to improve.

- The performance limitations of general-purpose microprocessors for dedicated tasks were now generally understood.
- Both IBM and Amdahl were using in-house designed ASICs successfully in their mainframe computers.
- CMOS had developed into a high-density, medium-speed process.
- Standard TTL "glue logic" no longer offered competitive cost or performance.

The ASIC suppliers of 1980 were made up of four groups. Most major electronics houses had their own in-house captive ASIC suppliers. Companies such as Honeywell, CDC, Burroughs, Digital, IBM, Tektronix, Data General, Wang, TRW, and Hughes were examples of firms with in-house ASIC capability. In 1980, these programs were under internal review, as the cost of modern wafer fabrication plants was continuing to escalate, in many cases negatively affecting the parent company's profitability.

A second ASIC supplier group was made up of the major U.S. merchant-market semiconductor suppliers such as TI, Motorola, National Semiconductor, and Fairchild. They grudgingly provided ASICs as a service to their major customers, but low volume and high-engineering content made the ASIC business unattractive to them.

The third group of ASIC suppliers were the Japanese semiconductor houses. They provided ASICs to their system divisions, but were concerned about entering the U.S. and Europe merchant market. Distance, culture, and language made it difficult for supplier and user to communicate. Their computer tools were embarrassingly hard to use and tied to Japan-based mainframes.

Finally, there were the small U.S. ASIC niche suppliers like AMI, Zymos, California Devices, and Universal Semiconductor.

About the only good thing you can say for them is that they really wanted to be in the business. Unfortunately, because they only had access to second-rate semiconductor technology, CAD, and capitalization, most have gone under.

None of the ASIC players at that time had all the elements needed to make ASIC mainstream. In 1980, events were taking place that would allow two new U.S. ASIC suppliers–LSI Logic and VLSI Technology–to revolutionize the industry.

3 Wilf Corrigan– The Early Years

Wilf Corrigan has emerged as a senior statesman of America's semiconductor industry. From 1974 to 1980, he was CEO at Fairchild, and he is a cofounder of the Semiconductor Industry Association (SIA). As Chairman, CEO, and principal founder of LSI Logic Corporation, he guided the firm from a start-up to a Fortune 500 company in nine years.

WILF CORRIGAN

When I was 19, I was a chemical engineering student living in England. I decided I wanted to visit the States for the summer, so I worked in Canada to save enough money for six weeks of hitchhiking from New York to California and back. By the end of my travels, I decided that when I finished college I was going to try to get a job in the States. As my graduation was approaching, I had three offers: a gun-powder factory in Australia, a chemical firm in Germany, and Transitron, a semiconductor company in Boston.

The Transitron offer was the result of an interview set up by a buddy of mine who had gone to work there the year before and gave me a call. "The president of Transitron is going to be in London," he said. "Will you talk to him?"

It seemed a little strange that a president of a big American company wanted to talk to an engineering undergraduate. Anyway, I went to the Dorchester Hotel to interview for a job. Wearing my one and only suit and tie, I knocked and this little guy wearing only boxer shorts opened the door. We talked for maybe three minutes, and then he said, "Okay, you'll be hearing

from us," and I was back in the corridor again. Nothing is going to come of this, I thought, but I was wrong. Two weeks later I was amazed when I received a job offer. I later found out why he was in his shorts–he was in London for his honeymoon. I looked at my Australian, German and American offers and said, "Screw it; I'll go to America."

As soon as I graduated, I got on the next plane and headed to Boston. This was in the summer of 1960. George Wells had arranged for me to have a room in the boarding house where he and his wife were living, a three-minute walk to Transitron. Although Transitron was then the world's third largest semiconductor company after GE and TI, they had rudimentary employment forms. My first day, I went to work at 8 o'clock and by 8:30 I was all checked in and signed up and sitting down at my standard-issue steel desk.

Here I was, a chemical engineer with a brand new job as a semiconductor production engineer, and I knew nothing about the subject. I decided I had better learn something about transistors and, not knowing what else to do, I went to the small company library, checked out *Transistor I*, a text on semiconductors, and went back to my desk. I opened to the first page and started reading.

At 9:30 the door burst open. This guy says to me, "Are you the new production engineer?"

I looked up and blurted out, "Yeah."

"I've got a production line down and 200 workers with nothing to do and you're sitting here reading a book?" he said. "Get your ass out there and fix it." That was my introduction to my new boss and on-the-job training in the American semiconductor industry.

Many of the engineers at Transitron were European. Over the water cooler, we discovered that, at $5,200 a year, we were making 30 percent less than the American engineers. We were

being screwed by Transitron. Thinking we could do better, we contacted the other semiconductor houses along Route 128 just outside of Boston. In those days Route 128 was a hotbed of semiconductor companies: Sylvania, Clevite, CBS Hytron, and Raytheon. Sure enough, we all came back with job offers of 30 percent or more than what were making at Transitron.

Then Motorola came to town with big recruiting ads in the local newspapers. I had two advantages in my favor. First, Motorola was looking for people familiar with epitaxy, a subject I thought I knew something about since I had done a project in college on crystal growth in liquid. Second, I was interviewed by George Russell, later General Manager of General Instruments, who was also English. By the end of the day, he offered me a job with Motorola in Phoenix.

There was one minor complication: my girlfriend, Sigrun, hadn't planned to come to the United States until after Christmas, so I called her. "You've got to come to Boston before Christmas," I said. What I didn't tell her was that after she got here, we would be leaving for Arizona.

When she arrived, I had another surprise in store for her. "Now we've got to get married," I announced.

"Why?" she asked. "We should spend some time getting to know each other."

"We've got to get married because I'm broke and Motorola will only pay your plane ticket if we are man and wife," I said.

We were married on Boxing Day, the day after Christmas. George Wells was my best man.

When we got to Phoenix, the epitaxy project at Motorola was just starting. Working around the clock, we were having breakthroughs by the minute. Epitaxy gave us a big performance advantage over the competition and we quickly developed an automated epitaxy system which subsequently allowed Motorola to become the world's major manufacturer of transistors.

In those days, by locking up the critical processes you could hold on to an innovation for two or three years before the competition discovered what you were doing. That's nearly impossible today because the equipment comes from the independent semiconductor equipment industry and is available to everyone.

I almost went to work for Fairchild in 1962 when Charlie Spork came down to Phoenix and tried to recruit me to run their Materials Department. He had a cigar bigger than Churchill's. I was only 23 years old and thought this was a great opportunity, so I went back to the Motorola guys and said, "I got a terrific job offer at Fairchild, and I'm going to give it a try."

Les Hogan, then Executive Vice President and General Manager of Motorola asked me, "Why do you want to take this Fairchild job?"

"It has profit and loss responsibility," I said. I didn't know what the hell that meant but it sounded like a good thing.

"Suppose I give you a job with P&L?" Les said. And that's how I ended up running Motorola's Transistor Department.

In my new position, I was working for Leo Dwork, Chief of Operations who ran ICs, transistors, and all semiconductors at Motorola. Taking me out on the production line, Leo asked me if there was any way that he could help. "Why don't we start by you showing me how to use a Tektronix 575 curve tracer?" I said.

Les was somewhat taken aback–I was going to be running the Transistor Department and I didn't even know how to use the most basic transistor test instrument!

At Les Hogan's invitation, I went to Fairchild in 1968 to do essentially the same job I had at Motorola running the Discrete Operations and Offshore Manufacturing. Then, in 1970, I was made the General Manager of the Semiconductor Division, and

that's when I first got involved in integrated circuits. I became President and CEO in 1974, replacing Les Hogan, who was made Vice Chairman. In 1977, I was elected Chairman as well as CEO.

In 1979, Gould decided that they would make it a key part of their strategy to get into semiconductors, and so they went after Fairchild. From our stock movement, it became obvious that something was happening, but we didn't know what. We found out that Ivan Boesky had taken a major position in the stock. We now knew that we had become a takeover target.

We had previously brought in Kidder Peabody, investment bankers who, in those days, offered a kind of anti-takeover service. Their role was to analyze Fairchild from top to bottom and advise us what to do in the event of a hostile takeover, and act as our defenders. The guy heading that operation was Marty Segal, who was later convicted of insider trading involving Boesky. You have only three weeks to respond to a hostile takeover; with the Kidder Peabody tender defense, you pressed a button and the contingency plan was set in motion.

When a takeover attempt appeared imminent, I called Segal in New York. "Marty," I said, "You'd better come out to Silicon Valley. It's battle stations here. We believe we're the target of a hostile takeover."

"Um-m-m-m," he hesitated. "I might have a conflict here. You know, it's been more than a year since we signed that contract and it has run out."

"Marty, are you telling me it's possible you might be coming in on the other side?" I asked.

"Well, I didn't say that, but we might have a conflict."

"Marty, you better get your ass out here because if you don't, you're going to get hit with the biggest insider trading lawsuit you've ever seen. You came into Fairchild, you signed a contract that said you were going to be our defender, and now you're the fox that got into the hen house. Now, I'm no lawyer,

but I'm pretty sure I can nail you and Kidder Peabody on this one. You call me back within 24 hours and tell me your position. Otherwise, I'm going to start the legal tanks rolling."

He called me back exactly 24 hours later. "Hey," he said, "We can't represent you, but we will step back from it; we won't be on the other side."

"Who is the other side?" I asked.

"I can't tell you."

Then we brought in as our new defenders Salomon Brothers, another investment banking firm, and asked them for a list of all of Kidder's clients. Gould was their second or third biggest client, and I had a hunch they were the predator since Gould's CEO, Ylvisaker, had been attempting to get on Fairchild's board for some time. I was right. A week later, Ylvisaker called me to make an offer. It was a set-piece conversation with lawyers sitting in. In this scenario, the phone call is followed by a letter from the target to which the predator replies. Gould wanted a friendly takeover. We said no thanks.

At first I thought we could fight the buyout. I was working on a letter to the stockholders when I found out that over half of them had owned the stock less than two weeks. They were arbitrageurs like Boesky. So I gave up on fighting a buyout and set out to get the best price for the stockholders. Gould's first offer was $54 per share. Eventually, after much hectic activity, we were able to sell the company for $66 per share cash to Schlumberger, the giant French oil field services company.

Schlumberger has an unusual business culture, kind of a "French-Tex" combination of sophisticated Europeans and Texas rednecks. After the buyout, Schlumberger wanted to interview the senior Fairchild staff to talk about replacing some of our management. "Hold on a minute," I said. "You have to understand that you just paid a half-billion dollars for Fairchild, and I think the smart thing to do is to let me spread 200,000

shares of Schlumberger stock around to the top 100 people as a gesture of your good will so that bonding will take place. All the Fairchild people are cashing in their stock options against the $66 price, and you've got to give more stock to the group."

"That's not our policy," they said.

To interview all our key people Schlumberger sent out their human resources director, a guy from the oil patch. "Well, I'm going to want to talk to all these guys," he demanded.

I didn't want this redneck pissing off our people and so I said, "No you're not."

"How are you going to stop me?"

"Simple," I said. "I'm going to tell the guards to throw you out."

If this was how Schlumberger was going to handle us Silicon Valley types, I could see that this wasn't going to work.

In November 1979, in one of a series of discussions with Riboud, Chairman of Schlumberger, I said, "You know, I don't think that my staying at Fairchild is going to work." He agreed. "Okay," I said. "Let's talk about phasing me out."

Schlumberger was a foreign company, so they had to integrate all the U.S. military business into a separate entity with its own board of directors. I hung around to take care of that, but even though I kept my position as Chairman, I wasn't doing very much from November 1979 until I left in February 1980.

I left with a one-year agreement with Schlumberger "not to compete" in the semiconductor arena. Since the industry was moving into a recession, I didn't want to be in the business then, anyway. I asked Larry Sonsini for advice. "It's okay to prepare to compete as long as you don't actually compete," he said.

So I thought I'd take this time to decide what I wanted to do next. I asked my wife, Sigrun, "Now tell me, what have you been deprived of doing all these years? ... We'll make a list." Skiing in Switzerland, sitting on the beach in Mexico, visiting

her parents, cruising on the QE2, she wrote. We knocked them off, one right after the other, in about three months.

After Sigrun and I did everything on our list, I decided that with my Gould and Schlumberger experience, I should get involved in mergers and acquisitions. I had a few contacts, and I talked to several people about acquiring American companies for Europeans, but nothing came of it.

Then I thought I would get into venture capital. I got together with two partners to start a venture capital fund we called the Atlantis Fund which would raise European money for investing in high tech ventures in Silicon Valley. That ended when my would-be partners backed out.

My venture capital experience taught me that it was better to catch than to pitch; I remember commenting to Sigrun one night, "You know, I think I'm going to start a semiconductor company."

"You must be crazy," she said. "Three or four years ago, you told me it was too late."

"That was true then, but things have changed."

ROB WALKER

Wilf's instincts in bailing out of Fairchild when he did proved accurate. Schlumberger installed their own man, Tom Roberts, as CEO. He had no experience in semiconductors. Years later, having lost market share and hundreds of millions of dollars, Schlumberger sold what was left of Fairchild Semiconductor to National Semiconductor for pennies on the dollar. The company that invented the integrated circuit and ASIC was no more.

4 Japan Inc.– The Semiconductor Colossus

The United States invented the transistor, CMOS, the integrated circuit and DRAM. But today, the Japanese dominate these markets. What went wrong? How can the U.S. keep from losing more of these seminal technologies? LSI Logic may point the way to an answer.

LSI Logic has been a major player in Japan since 1983 and taught Toshiba the merchant market ASIC business. In return, they taught LSI Logic how to make high-density, high-speed CMOS. Wilf Corrigan, moreover, was a founder of the United States Semiconductor Industry Association (SIA), the principal American lobbying instrument for the industry. The SIA has influenced U.S. trade negotiations to obtain semiconductor trade concessions with the Japanese.

LSI's Japanese affiliate, LSI Logic K.K., is a major supplier of ASICs to Japan, while Nihon Semiconductor Inc., a joint venture of LSI Logic and Kawasaki Steel, manufactures semiconductors in Japan for the home market and for export.

WILF CORRIGAN

Motorola's interest in Japan as a market was virtually nonexistent because, after World War II, American semiconductor companies weren't allowed to operate there–Hong Kong was a much more important market. In 1966, on a trip to the

Far East, I visited several Japanese semiconductor corporations. By American standards, they were primitive. We thought them quaint: just like going into a Japanese restaurant, you had to take your shoes off before you went into the fab. Certainly we didn't think the Japanese were going to be a threat.

When I got to Fairchild, I learned they had licensed the Planar process to virtually everyone in the Japanese industry. Fairchild was not allowed to sell directly to Japanese customers, but had to use NEC as its agent. Consequently, we had no insight into the Japanese market. Never meeting our customers meant that we couldn't learn from them. The arrangement worked well for NEC. Today they are the number-one semiconductor company in the world.

In the seventies the Japanese really couldn't compete with the Americans in TTL. Although they participated in consumer transistors, they were never major suppliers in the U.S. market. We never dreamed they would ever become serious competitors.

One factor was their lack of flexibility. The manufacturing strategy initiated by Charlie Spork at Fairchild in the early sixties could be described as jet plane automation–you flew chips from San Francisco to the Far East where, for eight cents an hour, they assembled the product and sent it back within the week. We were doing a form of arbitrage. Since we were accessing a twenty-to-one savings in labor costs, we didn't have to bother with automation. Certainly Silicon Valley companies were not leaders in automation. Using Far East labor meant that as products evolved, we didn't have to worry about retooling costs, a major factor when products are changing rapidly.

This flexibility gave us a major advantage over the Japanese who used automation and found themselves trapped when the product changed every 12 months. No sooner would they tool up, when the product became obsolete. Several Japanese executives told me that they were not cost competitive. Like the Japanese, Motorola also used automation and built everything in

Phoenix. Over the long term, automation was the right strategy. The enormous crutch of using low-cost labor in the Far East ultimately did a disservice to the U.S. industry.

Japan's defeat in TTL triggered their VLSI project. In the seventies, MITI and Japanese companies in the industry put their heads together and decided they needed a giant leap forward if they were ever to make it in the semiconductor business. They put together a program that was an admission that they couldn't win in bipolar–the U.S. was too far down the learning curve. And so they decided to put all of their efforts into MOS memory and go like hell. After sending senior engineering people to work together at a central VLSI laboratory, they then set up VLSI laboratories in each of the major semiconductor companies. Ultimately, the central VLSI laboratory was dissolved and their engineers brought back their newly acquired technology to their own companies.

The Japanese decided to rapidly expand in the U.S. by focusing on quality and cost. That meant giving qualification parts for free. When the Americans were still trying to sell qualification quantities of memory chips, the Japanese would just walk in and hand them 5,000 pieces with a value of $50,000 to $100,000. It was dumping, really.

We are only now beginning to recognize that the massively overvalued dollar and undervalued yen was a major factor in their success. Nobody in those days talked about the relationship between the two. While our government was bragging about the strength of the dollar, it is now clear that the Japanese government was deliberately managing their economy to keep the yen undervalued. That gave them a tremendous advantage in the export drive in the seventies. The Japanese strategy forced most U.S. and European suppliers out of the DRAM business.

The semiconductor trade arrangement signed by the governments of Japan and the United States signifies an important victory for the principles of open markets and fair trade. It's

not protectionist because it does not limit Japanese semiconductor sales in the U.S. It simply asks for the Japanese to open their markets to us. The new pact, which went into effect August 1, 1991, builds on efforts initiated in 1986 to open the Japanese semiconductor market to foreign products and deter Japanese IC producers from repeating the predatory dumping that ravaged our industry in the 1980s.

Ironically, U.S.-Japan semiconductor trade relations taught us that free trade doesn't occur as a spontaneous result of market forces. Efforts to open the Japanese market and discourage dumping have required our concerted political effort. Strengthening free trade principles by the new semiconductor agreement was largely effected by a unified stand throughout the U.S. electronics industry and the U.S. government's determined effort to eliminate unfair trade practices.

The new trade accord continues the activities to increase foreign access to the Japanese market established under the 1986 semiconductor trade agreement. Historically, the U.S. share of the Japanese market has been limited to about 10 percent through Japanese government targeting, subsidies, administrative guidance and cartel-like behavior. This limited penetration contrasts with America's nearly 60 percent share of semiconductor markets outside Japan.

Privileged access to their own market has allowed Japanese producers learning curve advantages and a safe domestic haven to earn profits while dumping on foreign markets. Japan itself has become the world's largest semiconductor market, making it imperative for U.S. producers to seek access there.

In 1986, despite our government's attempting for 14 years to open the Japanese market and more than two decades of efforts by the U.S. industry to sell in Japan, the Japanese semiconductor market had essentially remained closed. But the 1986 pact instituted a novel approach to prying open the market. Like its predecessor, the new trade pact contains a 20 percent

market share goal that, if reached, will mean that Japanese users can no longer treat foreign vendors as residual suppliers.

The SIA came up with the 20 percent goal using two criteria. The goal should be achievable and be more than cosmetic. The European, American, and other non-Japanese share of the semiconductor market in Japan was around 10 percent in 1986. It seemed reasonable that they could double that commitment by 1992. In addition, we felt the 20 percent goal would require the Japanese to make a real commitment to their foreign suppliers–much as the American computer makers are totally dependent on the flow of DRAMs from Japan.

In 1991, the foreign share of the Japanese market was up to 14 percent from 8.6 percent in 1986. Much of this has been achieved in recent years, and we believe that the new trade agreement will build on the positive momentum that has developed toward opening the market.

During the 1980s, Japan dumped DRAMs and EPROMs, forcing nine of eleven U.S. DRAM makers out of the business and causing EPROM producers to lose hundreds of millions of dollars. By destroying competition, the Japanese were able to control the market, raise prices, and reap windfall profits.

The 1986 trade pact committed Japan to stop dumping in the United States and elsewhere. The Department of Commerce held dumping in check by collecting cost and price data from Japanese producers and setting quarterly foreign market values (FMVs) as minimum sales prices for DRAMs and EPROMs.

FMVs were based on the cost of production and set individually for each company so that more efficient firms could sell at lower cost. The latest trade arrangement eliminates the need for the government to issue FMVs; individual Japanese chip makers must maintain cost and pricing data and provide it to the U.S. government on an expedited basis if dumping is alleged. This approach reduces government intervention while providing a strong dumping deterrent through the discipline of maintaining

the proper data and the threat of a quick response to predatory pricing.

Part of the trade agreement is that foreign suppliers, including American, European, and Korean companies, would gain a 20 percent share in the Japanese semiconductor market by the end of 1992. Unfortunately, our market share has stagnated at about 14 percent through the first half of 1990 and all of 1991. Since Japan is not honoring the trade agreement, the SIA has actively lobbied the U.S. government with the message that we need help.

The lesson learned is that we need an active trade policy if we are to avoid having our trade managed by other nations. The new pact can be a model for what can be achieved through industry coalition building and by combatting unfair trade practices in a way that is effective, yet not overly intrusive in the marketplace.

THE GENESIS OF LSI LOGIC–1981

5 Writing the Business Plan

Wilf Corrigan was becoming restive. He had spent his entire professional career in semiconductors. His foray into venture capital had not excited him. He wanted to become a player again.

WILF CORRIGAN

Having decided to start a semiconductor company, I spent quite a few months visiting people I knew in the computer industry, both in the United States and in Europe. A pattern started to emerge: most of these companies needed custom circuits. I had flashbacks of when I was at Fairchild and good customers would ask me, "Would you do a custom program for us?" At Fairchild, I always said no, but in retrospect, I should have recognized that over the previous few years there was an opportunity bubbling up in custom circuits. People were upset at that time about Motorola's inability to deliver their ECL gate arrays. CMOS ASICs were also a problem–AMI was the largest supplier and was not highly regarded.

I thought about this for several months. Custom circuits–the big guys don't want to mess with them, the customers seem to need them, yet there don't seem to be any viable sources in spite of increasing demand.

It had also become apparent in the seventies that a surplus of semiconductor processing capability was emerging worldwide. You could find $100 million semiconductor plants in Korea, Germany, France, and England–lots of reasonably good, but relatively dumb capacity. Nearly every government considered semiconductors strategic, yet they lacked products. I figured they would be happy to fabricate some ICs for us, and

we could forego building a $100 million manufacturing plant for several years. Besides, a lot of money was available for investing in semiconductors.

I went to see Bob Ulrickson. "Bob, I'm thinking of starting a custom semiconductor company. What do you suggest? Who should I get to be the technical gurus?"

"Well," he said. "Why don't you get the best–Walker, Koford, and Jones? I don't know where Koford and Jones are, but Rob is local and consulting."

ROB WALKER

I was born and raised in California and graduated from UC Berkeley with a degree in Electrical Engineering. In 1958, I was running computer programs on Cal's IBM 701 mainframe and a Univac I. Computers were a little primitive in those days–the Univac had 256 words of high-speed memory; you had to go to mag tape or punched cards for additional storage.

I worked at UC's Lawrence Radiation Laboratory doing system and instrumentation engineering until 1963 when I moved to Ford Aerospace (then Philco-Ford) in Palo Alto. We did a lot of the design of Houston's Manned Spacecraft Center and eventually developed the first commercially available integrated circuit modules based around Fairchild DTL. In 1967, I went to Fairchild and started my ASIC career. After our downfall at Fairchild, I went to Intel in 1975. It was exciting early on, but as the company grew, it became less and less satisfying. Finally, in 1980, I cashed in my stock options and left.

I was looking for opportunities as a consultant and Bob Ulrickson put me in touch with Bob Hartman who was starting a gate array consulting company known as Source III. Hartman and I decided to upgrade our knowledge and get a little publicity by writing a survey article on gate arrays. We visited almost every gate array supplier, reviewing their products, methodology and computer aids. I couldn't believe it! Ten

years after our Fairchild work, the industry's ASIC capability had actually retreated.

True, semiconductor technology had progressed: HCMOS allowed over 1000 gates of random logic to be economically implemented on a single chip. Graphical design systems from Calma, Applicon, and Intergraph simplified IC topological layout. But our old Fairchild CAD capabilities of logic simulation, auto/interactive place and route, and design for testability were virtually unknown.

Reminiscing with the old Fairchild troops–Jim Koford, Ed Jones, and Bill Jensen–over lunch at the International Market in Mountain View, I commented that the Fairchild ASIC organization circa 1972 could overwhelm the 1980 ASIC competition.

Wilf's contacts allowed him entry into the top management of most of the major computer companies. When Wilf visited Burroughs, CDC, Univac, ICL, Amdahl, Digital and others with the question, "What kind of a semiconductor company would be of use to you?" They all said the same thing: they got good service in high-volume standard products from the semiconductor majors, but support for low volume ASICs was at best half-hearted. And so they invested heavily in their own captive semiconductor facilities. Unfortunately, they were not emotionally or financially prepared for the rapid progress in semiconductors with its devastating appetite for ever-more expensive factories. They wanted a high-quality semiconductor company that could quickly and accurately produce custom circuits, and would allow them to supplement or replace their in-house facility.

When Wilf contacted me, I had just completed the research with Bob Hartman on our gate array magazine article and I was completely up-to-date on the latest status of the ASIC players, products, and technology. I told Wilf I was confident we could assemble a technical team that would blow away the competition. To my surprise and probably Wilf's, we did exactly that in three years.

JIM KOFORD

In the late seventies I was running the Data Communications Development Lab in Sunnyvale for Boeing Computer Services. Rob Walker had been at Intel for a number of years. Now he was in a private consulting business, but he kept in contact. Over lunch we would speculate whether ASICs would come back.

At Boeing we were designing systems, and I began to get phone calls from some Boeing engineers about ASICs. Also, I interpreted what I was reading in the trade press as a resurgence in semicustom ASIC thinking. Due largely to the work of Carver Mead and his book, *VLSI Design*, ASIC had become a hot topic once again in universities like Berkeley, Stanford, and MIT.

One day I got a call from Rob I'll never forget. "Guess what?" he said. "I've decided to join Wilf Corrigan in a new ASIC start-up he's putting together." I was glad he had asked me if I was sitting down because Wilf Corrigan was not known as a friend of ASIC activity at Fairchild. But in retrospect, Wilf's closing down the activity in the seventies was justifiable.

I was reluctant to get involved in a start-up. I had a good job at Boeing and a nice little lab with some of my favorite colleagues working together on small, but interesting projects. But Rob was persuasive, and he got me to talk to Wilf. Wilf had been in venture capital for a year and was itching to get back into semiconductors. He was considering how to start a major new semiconductor company. He laid out a plan to manufacture gate arrays using only a metal fab; diffused wafers would be purchased outside. Developing a CAD system to supply gate arrays to the customer base was key and it was needed fast. A design service capability was also needed, because without one, his plan would never fly.

WILF CORRIGAN

As I talked to Walker, Koford, and Jones, the Micromosaic period at Fairchild came back into focus. In 1980 we could get

powerful computers cheaply, whereas ten years earlier, they were expensive. In addition, we thought that CMOS could replace TTL. I figured that we could easily go after the Motorola Macrocell ECL array business and wouldn't have any legal problems, but if we started to attack Fairchild ECL ASIC products, it could trigger a lawsuit.

Koford and Jones were unusual guys, and at first we had a few communications problems. It soon became evident that Walker, Koford, and those who had worked on Micromosaic at Fairchild had this great sense of unfinished business; they had successfully developed the technology for ASICs, but the timing and the market had been wrong. I was surprised that these conservative guys really wanted to do an ASIC start-up. Older guys weren't supposed to start up companies. The paradigm of a start-up was Apple Computer with two kids in a garage.

I had postponed decisions on marketing, manufacturing, and finance until we had a technical direction, but venture capitalists wanted to see a complete team of people. I was thinking in terms of a big company where you do the development, and then worry about the marketing, while in a start-up, you start selling from day one.

I had to get the marketing guy on board. My first choice was Bill O'Meara because I had great confidence in his energy and salesmanship. So I called him. "Bill," I said, "I'm starting a company. Rob Walker is coming and Koford and Jones, and we'd like you to be the marketing guy."

"Of course," Bill said.

"Okay, we'll call you in a week or so and fill you in on the details." And that was the entire conversation. We had so many things going on that I didn't have time to go into details.

BILL O'MEARA

After graduating from West Point, I spent five years as an Army helicopter pilot. After leaving the service, I had several sales jobs,

and in 1969 I started at Fairchild. Three years later I was a Regional Sales Manager in Florida.

One evening I got a telephone call from Wilf Corrigan. "Hey, Bill, we want you to come to California and head up the Fairchild MOS Product Marketing Group."

"Well, I'm really honored and pleased and proud," I said. "but I don't want to do that."

"Bill, you're not listening," he said, "we want you to come do this."

And I said, "I am listening and I hear you, and I appreciate it and I'm honored, but it's not something that I want to do."

"You are NOT listening," he said. "WE WANT YOU TO COME DO THIS."

"Oh," I said.

"Fine," he said. "I'll see you Monday morning."

I went home and told my wife that we were moving to California. Well, of course as a Midwestern girl her view was a little different than mine. "My God, Sin City?" she said. "Nobody stays married. Everybody gets divorced. Everybody has sex with everybody else. Everybody's on drugs. Is this where you want to raise our children? I have no desire to go to California. If you want to go, fine, but I'm not."

I eventually talked her into it, but she had great reservations. Ironically, we moved to Saratoga–more conservative by far than the community we left behind.

I headed Fairchild's MOS Product Marketing in Mountain View. My first year, except for weekends, I had dinner with my family only once. I never left the office before 9:00 p.m. Fairchild MOS Division was in deep shit and I was part of a team assembled to try to turn it around. Ultimately, we were unsuccessful, but it wasn't because we didn't try. At any rate, when I had been out there about two months, one night about 8 o'clock Wilf stopped by my office. "You still here?" he said.

"Hell yes," I replied.

"I know that you didn't want to take this job and that you took it because I asked you to," he said. "I'll never forget that." And he didn't.

A year and a half later, I decided that I was either going to quit Fairchild, commit suicide, or get a new job. I couldn't take the MOS Division: we had gone through three divisional managers; Phil Thomas was the current one. He was a wild man–screaming and ranting and raving. We had already been through Roy Pollack and Leo Dwork.

I was able to get out of MOS and had a succession of sales and management positions at Fairchild, ending up as Vice President of Sales. I had a lot of contact with Wilf and developed great respect for him. Later, I left Fairchild and became sales VP at Synertek, a subsidiary of Honeywell.

In August 1980, I got Wilf's twenty second call offering me a job in some unspecified new company. Without thinking, I agreed. After I hung up I thought, "Oh shit. What was this company going to build?" I called my wife and said, "I think I just committed to joining Wilf in a start-up and I don't even know what the product is!"

My immediate reaction was right-brain. Later I met with Rob and Wilf and we started mapping out some ideas.

WILF CORRIGAN

Bill O'Meara recommended Mick Bohn for our finance guy. Mick was VP of Finance at Synertek, and he was smart, hard-working and very ambitious.

MICK BOHN

I was born and raised in North Dakota, and went to school at the University of North Dakota. I came out West and went to work in San Francisco for Price Waterhouse where, through audit, I became acquainted with several electronics companies in Silicon Valley.

Bob Dahl, a friend of mine from Price Waterhouse, was then the Controller of Fairchild. Bob hired me into Fairchild but about two weeks before I started, Bob left and a new guy, Jim Hazle, took over as Controller. Probably against his better judgment, Jim hired me.

That was the first time in my life that I ever ran into the concept of layoff. I started around the first of November 1975, and within two weeks, I went to work on a Monday and one of the four financial analysts in the group wasn't there. So I asked my boss where was so-and-so?

"Oh, he got laid off Friday."

"What do you mean, got laid off?" I asked. He explained how you could have a job one day and not have a job the next. That was my welcome to the electronics industry.

This was before Thanksgiving. You have to remember that in the semiconductor business layoffs usually happen at Christmas. Less than a month later, I witnessed this when two additional analysts stopped coming to work a week before Christmas. I asked my boss, "Where are so-and-so and so-and-so?"

"They got laid off Friday," he said. I'm convinced that I kept my job only because of my low salary.

While I was at Fairchild, I got involved in a range of corporate-wide activities including the Far East assembly plants, European marketing and sales operations, and some acquisitions. It was really a great training ground. In fact, when Gould made their initial offer at about $54 a share to acquire Fairchild, I was involved with generating documentation to find a white knight (ultimately Schlumberger) who would bid a higher price.

While the stock price was wallowing around $18 or $19, my options were at $24 a share. Gould came in and offered $42. Ultimately, Schlumberger came in at $66 a share, and

suddenly my options were worth a lot of money. Having been involved in acquisition work at Price-Waterhouse, I knew that whoever buys the company wins and whoever is at the company loses, so after the Schlumberger acquisition I cashed in my options and left.

Then I went to work for Measurex Corporation, and from there Synertek, a company making custom circuits mainly for Apple and Digital Equipment Corporation.

I remember my first discussion over at Wilf's house about creating a new company to do custom semiconductors. I think Wilf was mildly uncomfortable with the idea of a custom business. He had never been really involved in that portion of semiconductors. Bill O'Meara and I were fairly knowledgeable since almost half the revenue at Synertek came from custom circuits.

I always found it curious that Synertek was able to maintain strong business relationships with companies such as Apple and Digital when, invariably, we screwed up every custom program we had. The work was never done on time. There were always lots of design iterations, and yet somehow our customers would continue to give us new programs. In addition, at Synertek we could only really do about 12 design programs a year, and so we had many discussions on how LSI Logic could make a big business out of ASICs. I think that's where Rob's experience in the automated approach toward custom silicon back in the Fairchild days came into play.

It was in those discussions that I first heard of Koford and Jones. I remember Rob saying to me, "Well, they're a little unusual, but they're good guys."

WILF CORRIGAN

Okay, we've got the engineering, marketing, and finance guys, now we've got to worry about manufacturing. I was sure that Bill Baker, then at AMI, was the right guy. Bill was top notch–

very high energy, and very much involved in the details on the manufacturing floor. I thought he'd be ideal, and when I talked to him he said, "Yep, sounds good to me." And so we had Bill Baker on the team.

Just before we got our funding Bill Baker called me and said he had financial commitments and he couldn't accept the pay we were offering. He finally dropped out and AMI made him a vice president.

Then I considered Jack Higbee at Fairchild MOS–he would be a great start-up guy. So I called him. "Jack," I said, "we're doing this start-up."

"Oh yeah," he said, "I read about it in the newspaper."

"I'd like you to be the manufacturing guy," I said.

"Hey, they've more or less put me out to pasture here at Fairchild and I come in to work at 9:00 and I leave at 4:00 and I don't do very much," he said. "I've been doing it for about a year and I'm getting so I like it. I think I'm a nine-to-four guy."

"Well," I said, "that's okay Jack, you can come in and you can work nine to four if that's what you want to do."

He paused. "Okay," he said, "but you understand, I'm not going to be one of those seven-day-a-week guys."

"No," I said, "that's fine–this is going to be a very relaxed sort of environment."

After he came on board, he was always there at seven o'clock in the morning and he stayed until eight or later at night.

6 First-Round Financing

It takes a lot of money to start a high tech company. Fortunately, there is a worldwide network of investors and venture capitalists who recognize that, while the risks are high, the reward from a successful start-up can be very profitable. These investors routinely risk millions on a team of technical people armed only with a business plan and a dream.

WILF CORRIGAN

I had it in the back of my mind that I should explore alternate sources of capital outside the Silicon Valley venture capital network. I went to England and I talked to a number of people including an old friend of mine, Arnold Weinstock of GEC.

"Look, I'll put up $5 million for you to finance your company," he offered.

"Yes, but that isn't the deal," I said. "The plan is that the money people put up the capital and the management gets a major piece of the equity and we take the company public in a few years, and everybody wins."

"No, no," he said, "we'll just do it all within GEC and I'll put up the $5 million; you can work through us." I never could get the venture capital concept over to him.

Then I went to San Diego and talked to Mr. Inamori, the founder of Kyocera. "Mr. Inamori," I said, "I'm going to start a semiconductor company. Would you be interested in being an investor?"

He thought about it for about five minutes, and then he said, "I will put in $1 million as long as I can invest at the same

price as everybody else. That's all I need to know. You've got my commitment for a million; when you put the deal together, come back."

After my first cut at a business plan, I took it out of town to try it on the minor league investors. I also began talking to Rob Walker, and soon after that the founder group started to form, and concepts began to gel. I figured that ultimately most of the money would come from the Silicon Valley venture capitalists. But I wanted at least to create some sense of a market and expose the deal to a number of out-of-town investors to reveal the obvious warts in the plan, just like you take a show off-Broadway first. That way we could hone the presentation and create some backup investors.

I figured that the discussion with the local venture guys would be like a sumo match–a little bit of sparring and then, wham-bam, we'd have a deal or not. To optimize our position, we had to polish our story. I quickly found that I needed names and faces and resumes before anybody would move off the dime. The individual with a concept quickly became a group that was an embryo company, and the plan evolved.

Fred Adler, the power behind Data General, was another friend of mine over the years. When I was in New York, I'd usually stop in and see Fred just to keep in touch. "Would you like to be an investor?" I asked him. Fred came back with a proposal that, had I been a girl, would have been a proposition: he wanted to invest a minimal amount of money up front and if we met every objective in the first three months, we would get more money–maybe. If we met the objectives for the second three months, we'd get more money. With this deal Fred obviously would have been calling the shots from day one, just like he did with Daisy, which he ran into the ground. So I politely told him, "No, Fred, we don't want to do a deal with you."

I talked to a couple of major venture capital friends in San Diego and Los Angeles and a couple of English venture capital-

ists. By then, we had a pretty polished story and a sense of our perceived worth. We deliberately started with a very high valuation with the out-of-town guys just to try it; so by the time I was ready to talk to the local venture capitalists, I had a pretty good idea of what was a realistic deal.

Eventually, it was time to see the local venture capital inner circle. I talked to Wally Davis of Mayfield Fund, who is a reasonable, rational sort of fellow. "We're interested," he said, "but would you mind if we brought in Don Valentine–he knows the semiconductor business."

"Fine," I said. Obviously the local venture capitalists were thinking, "For a semiconductor deal, you talk to Valentine." Don and I had known each other for a long time and he is a very tough negotiator. Before becoming a venture capitalist, he was VP of Marketing first at Fairchild in the mid-sixties, then at National Semiconductor. Our business plan was now under discussion, and a number of other investors were sniffing around.

One night Tom Sherby, who used to run the Test Systems Division of Fairchild for me, called me up at home. "Hey," he said, "the rumor is around that you're starting a new semiconductor company."

"That's true," I said.

"Well, Geoff Taylor, a friend of mine, is just visiting from England," he said. "Geoff would be very interested in the deal."

I didn't know who the hell Taylor was. "Well," I said, "I think the deal is pretty much closed."

"Well," Sherby said, "can we come over and talk to you for about 30 minutes?" Sherby practically lived next door, so they walked over, and he introduced me to Geoff, a very nice guy.

"What's the deal?" Geoff asked.

"I think LSI Logic's first round is going to be at a valuation of about $13 to $15 million," I said. "We're still negotiating the deal, and we're looking to raise about $5 or $6 million initially."

"Well, I could probably take half of that." Geoff said.

"No way," I said. "I've got lots of other people involved." I was now thinking this was the biggest bullshitter in the world–some guy from England just walks in off the street with a cockamamie story that he might make a $3 million investment.

"Well, give me some details on your outfit," I said. "I'll keep you informed and if there's any space in the deal, fine." I figured that I would talk to Sherby afterwards and find out this guy's real story; I didn't know if he was high or what.

Later I talked to Sherby, "What the hell is this with this Taylor guy that he's going to invest $3 million on 10 minutes of discussion in a field he knows nothing about, when we've been scratching around here and there, and nobody is putting out much money?"

"Oh yeah, Geoff is with this big venture capital fund in England and they really want to get active in Silicon Valley," he said.

I called Taylor back and said, "We've looked at it and maybe we can let you in for half a million. But you've got to make some sort of commitment because otherwise the local guys are going to take the whole deal."

"Put me down for a million," he said.

I went back to the negotiation with Valentine feeling a lot better; I could probably get a million or so from Geoff Taylor and another million from Inamori. At that time, the inner circle local venture community all invested together–they were either in or out. I had been pounding the pavement talking to the key players: Don Valentine, Reed Dennis, Gene Kleiner, and Tom Perkins, Menlo Ventures, Sutter Hill, Mayfield Fund, and others. For a time the venture capital fund of Standard Oil of Indiana was interested, and Steve Merrill of The Bank of America Venture Fund which later became Merrill Pickard. The line between an "expression of interest" and a "commitment" is

rather ill defined–you don't have the money until the checks clear.

One day, Valentine sat me down in his office and said, "Okay, we're going to negotiate the final deal." We agreed on a price corresponding to $10 million valuation. "Okay," he said, "I'll just let the guys know and see how much they want."

"Well, there's a couple of outside investors who want in," I said. "Inamori is in for a million, and Geoff Taylor should probably be in for another million." Eventually we had $9 million offered for $5 million on the table, so we took another $1 million, and then allocated it more or less on a *pro rata* basis. Inamori and Taylor each were in for $500K (which was worth $15 million each when we went public).

Eventually outside investors put in $6 million for 60 percent of the company. I personally came in for $500K on the venture capital side–all my liquid assets at the time. I wanted to make it clear that I was burning the boats. LSI Logic had to be a success.

7 Expanding the Team

In January 1981, LSI Logic consisted of Corrigan, Walker, O'Meara, Bohn, and Higbee. They had $6 million in the bank and were profitable just from the interest. They rented offices in Sunnyvale, and Sigrun Corrigan, Wilf's wife, was the part-time (and unpaid) secretary. Rob Walker immediately made offers to Jim Koford and Ed Jones; they would be responsible for developing the computer aids for logic and layout just as they had in 1967 at Fairchild.

JIM KOFORD

Ed and I were reluctant to give notice at Boeing because we knew that that would cause a lot of consternation since they had set up the lab specifically for us. Boeing came back with counteroffers and several of the key managers came down and tried to talk us out of leaving. It was painful because they had treated us very well. We agreed that we would not take any of the other key personnel and would try to keep the projects in the Boeing lab alive.

Leaving Boeing was one of the toughest things I ever did. I knew it was risky to embark on a venture like LSI Logic because by the eighties it was clear that the capital requirements of the semiconductor business were enormous, and the Japanese were beginning to come on very strongly. There was a real question as to whether a major new U.S. semiconductor company attempt would be successful. Furthermore, we had had an aborted ASIC effort at Fairchild and, although we were pretty

sure the conditions were different now, ASICs had not been a successful business.

I think in the end what convinced me (and I knew Rob felt the same way), was that we had a score to settle. We had seen the future, and it would be too painful to sit by and watch others implement it. It sounds corny, but ASICs were our destiny. You do things in life not necessarily for reasons you understand, but once you've made a commitment, it is something that you don't shake easily–at least I don't. We made a commitment in the seventies to ASICs and it didn't succeed. It was clear to us that the conditions had changed in 1980 and it was important for our destiny, if you will, to try it again. I guess in a way, I was so convinced it was going to happen that the opportunity to try it again was irresistible.

ROB WALKER

After lining up Koford and Jones, I started a search for two engineering managers who would head up our CMOS and ECL design groups. After being rejected by two senior ECL designers, I was fortunate to recruit Dan Wong, the Engineering Manager of Fairchild's 100K ECL design activity–at the time, the most advanced ECL capability in the world.

In 1981, CMOS was rare in the United States: none of the U.S. majors were pursuing it heavily. I recruited Ven Lee who was a CMOS memory design manager at Intersil to head up our CMOS effort. Richard Derickson came aboard from Ampex as our first logic designer and modeler.

VEN LEE

I accepted Rob's offer to join LSI, but I had deep reservations about this totally unproved company with no products, no fab, just a few guys in rented offices in Santa Clara. I had just built a home in Los Altos Hills, and the loan payments were overwhelming. I was in my car, heading to LSI for my first day of

work, and as I cruised down Lawrence Expressway, I wondered if I should take another job offer I had with a much larger and more stable company. Fortunately, I turned the wheel right and went to LSI; a left turn would have taken me to the larger company.

ROB WALKER

Meantime, Wilf hired Conrad Dell'Oca to head up process R&D. Mick hired Bonnie Schaefer to handle all personnel and clerical issues, and Susie Solner to handle payroll, reception, and telecommunications. Ven recruited Dottie Heim from Intersil. She was and is one of the most respected mask designers in Silicon Valley.

With this core team, in just one year we were able to develop and introduce leading-edge design automation, CMOS and ECL gate arrays, extensive logic libraries, and a customer training course.

It's amazing what a few dedicated people can accomplish when they have clear goals and a minimum of corporate bullshit.

8 Silicon and Software Development

Once the company was funded, LSI's challenge was to develop a product line and take it to market within a year.

ROB WALKER

Our 1981 business plan had detailed our product strategy. We had to develop in parallel:

- A line of ECL gate arrays to service the mainframe computer market. Gate array chips use identical "masterslices" of uncommitted transistors customized to a specific application by the deposition of unique metal interconnections. We intended to have masterslices manufactured by one or more outside semiconductor manufacturers, and then do the metalization ourselves in a low cost "metals fab."
- A line of CMOS gate arrays for the general purpose electronics market. Again, we would have the masterslices manufactured by others.
- A computer-aided design system to support both ECL and CMOS technologies. This system would be used to support LSI Logic designs and would be licensed to customers and other ASIC manufacturers.
- The necessary libraries of logic functions including many popular "standard product" TTL functions, along with documentation and ASIC classes to train customers in the use of the technology.
- A manufacturing capability, including metalization, assembly and test.

After we got funded in January 1981, we spent more time analyzing the business, and it became apparent that the

"design-in cycle," i.e., the period between the start of an ASIC design and volume production, was a year or two. Assuming it would take at least a year for us to develop our design and manufacturing capability, it would then be two more years before cash flow began from volume production. We didn't have the money to hang in there that long–we needed a jump start.

The answer was to license array families that had been around several years and were already in volume production. In CMOS it was simple, California Devices and AMI offered the gate array designed by Bob Lipp that had garnered many design wins. We were able to license Lipp's design which we called the LSI Logic LC Series.

The best choice for an ECL array was equally obvious: the Motorola Macrocell ECL arrays which had won many mainframe design wins. In fact, as we traveled around the country, customers pleaded with us to second-source it.

Wilf flew to Phoenix to discuss a licensing deal with his old friends at Motorola. They made it clear that they enjoyed their sole-source position and it would be a cold day in hell before they would license the Macrocell ECL technology to our unknown California company.

Fortunately, a potential customer had given us a Motorola Macrocell device. We popped off the lid and examined the chip. Guess what: no copyright notice, which meant we could legally copy the design! In fact, Motorola was so casual at protecting their intellectual property, they hadn't even bothered to trademark their Macrocell name, so we took it for our own.

I asked Dan Wong, our ECL design engineer, to copy the Motorola part in every detail. He pointed out a number of weaknesses in the design and wanted to improve it, but since that would compromise our second-source strategy, I convinced him to design a part that was identical in form, fit and function to Motorola's, warts and all. In both CMOS and ECL, we

planned to follow up the initial second-source designs with leadership products, as AMD had done in TTL so successfully in its early days.

Meanwhile, Ven Lee and Patrick Yin were pursuing our CMOS long- and short-term strategies in parallel. Ven was working jointly with Toshiba on our 3-micron leadership CMOS array, the 5000 Series. The family had up to 5000 usable gates and TTL speed. It would be our high-end CMOS product that would get us into computer accounts. Patrick Yin was charged with taking the California Device/AMI 5-micron array, which we had licensed from Bob Lipp, into a production-ready product. While it was obsolescent when we licensed it, there was immediate production available since it had been on the market several years. There was the added advantage that AMI had lost the process, which allowed LSI, the newcomer, to become dominant in the product line.

Ven and Patrick did their development with their usual brilliance and we had working silicon on both product lines by the end of 1981.

Our computer-aided design strategy was also a two-step development. Our initial product was called LSI Development System, LDS for short. To get a design capability as quickly as possible, we decided to go outside for all the software we could. We picked Fortran for its availability and maturity with a plan to write many of our own software tools in a more modern computer language later.

MICK BOHN

Our *modus operandi* was to buy elements of CAD tools which we would then bolt together in an integrated design system. Since we planned to license the system to others, we needed to get the rights to relicense the software. I flew out to Austin, Texas and visited a little CAD company called Comsat General

Integrated Systems. They were CAD guys out of the University of Texas at Austin who had developed TEGAS, a logic simulator. Koford had identified this logic simulator as the leading candidate for the LDS logic simulation engine.

The president of the company was Steve Sajimda, a funny guy who had a grandiose self-image. It was his considered opinion that he was the brightest CAD guy in the world and he had a fancy office to prove it. When you walked in, you felt as though you were visiting an English baron at his estate. There he was sitting behind a huge desk in a room with oak-paneled ceiling and walls and smoking a foot-long cigar. He reminded me of a young Groucho Marx.

After several negotiating sessions, we agreed on pricing for our version of TEGAS, a multiple copy price, and the rights to the source code. I saved for last that we wanted the rights to relicense TEGAS to other third parties as part of our LDS system. That turned out to be the deal breaker. Nowadays such OEM deals are commonplace, but in 1981 they were rare. Sajimda must have felt that we were going into competition with him with his own product. I left without a deal.

I told him I was on my way to his competitor in Arizona. I went to the Austin airport, turned in my rented car and was sitting in the lounge waiting for my plane when I was paged. It was Sajimda. "Mick," he said, "we've had a chance to talk about it. You've got a deal."

Ed Jones had picked a local company called Silvar-Lisco to supply our place and route software. I figured they would be easier to negotiate with than COMSAT because they were a local company in Palo Alto. I was wrong. Their president, Bill Von Klempets, had the same reservations as COMSAT about licensing his software to LSI Logic with rights to relicense. We got what we wanted–rights to resell–but pretty much on their terms.

ED JONES

Silvar Lisco's problem was that their turnaround for fixing bugs was a week or so and there were a lot of bugs to fix. We tried to develop this project on a shoestring. I figured out that I could speed up the whole layout process and so I started working in my spare time on a graphics editor program by reviving the Fairchild strategy with state-of-the-art graphics. At the same time I kept trying to use the Silvar-Lisco tools but without much success. In the meantime, we discovered a small company called Megatek in San Diego that was developing a low-cost color graphics terminal. We were their first customer for the terminal. The case wasn't even ready so our unit was just a chassis and separate monitor that was propped up on its packaging case and jury-rigged to our National mainframe.

We had bought the cheapest computer that had a chance in hell of doing the job–a used National Advanced Systems NS5000. We didn't have any raised floor so we stashed it in a back-corner office and stuffed air-cooling tubes hung from the ceiling into the machine to try to keep it from boiling away.

One day I was up on a ladder stringing cables through the ceiling to connect up the terminals in the office I shared with Jim; we were trying to get the National up and we only had the console to run programs. Bill O'Meara walked in with a couple of potential customers and asked me if we could demo anything. I happened to have a program that I had written just for fun when I was at Boeing, that generated a maze and then solved it. The maze was displayed on a simple alphanumeric terminal. It ran the maze and when it hit an obstacle it would pull back and then try another route. Our computer was slow enough so that you could watch the program move, find a blank wall, then pull back and try again. I turned it loose on the customers, telling them it was a maze router. They were impressed.

We finally got the Megatek up and I started working on the data structures that make up most of the code in a layout

system. Once I had gotten enough graphics to put a line on the screen, I didn't particularly worry about displaying more because the data structure was the key task. Wilf would come wandering by and find me typing. I was working mainly on building the data structures, but I had the graphics display with a line or a square or a cross to represent the various structures that I was getting ready to manipulate. Wilf was having difficulty making the connection between one line and the layout of a complex ASIC. Koford and I weren't bothered since we knew that if you could draw one thing, you could draw as many of them as you wanted.

JIM KOFORD

In those days, if a computer program used graphics, you had to define your algorithms and data structures, write the core routines, interface the graphics to the peripheral equipment to whatever computer environment you had, and make all the drivers work. If you had a pointing device such as a mouse, you would make certain that it interrupted your software processes properly. We couldn't buy this capability off the shelf, so we did that work ourselves in the first half of 1981.

Naturally, the other people in the company began to get curious about all this software and wanted to see it. Late in the summer, Ed and I put together a "presentation" to demonstrate our progress. We got Wilf, Rob and Bill into our office. We really hadn't paid a lot of attention to making things look particularly neat. Ed had cardboard boxes taped onto the display to shade it from the room lights, and the Megatek was stacked on packing boxes with the cables to the mainframe decoratively draped up the walls. Ed gave a brief chalktalk and then a short demonstration. When you are developing software at that rate, you don't spend a lot of time putting together anything fancy. We felt it was enough to show just the key features of the data structures and the software that we were

developing. Anyway, Ed got through his simple demonstration for Wilf in spite of a few glitches. Wilf seemed uncharacteristically subdued, but he was polite.

Later, Wilf confided to me, "You know, I really had a problem with Ed's demo. We're selling customers on this great new CAD system that's going to revolutionize the world, and all I saw was a red line, a blue line, and a yellow X on an otherwise blank screen being manipulated by an enthusiastic Ed Jones and Jim Koford. I don't know what I've gotten into." Well, of course, Ed had actually made a tremendous amount of progress and he hadn't wasted time putting a whole chip on the screen. He was far more interested in developing the software and showing a test case. I realize now how that must have looked to Wilf. He was betting the company on us.

9 We Do Our First ASIC Design

ASICs are typically sole-sourced–if the supplier can't deliver, the customer is shut down. That's why selecting an ASIC supplier is like selecting a heart surgeon–no one wants to be the first patient. That was LSI's problem in mid-1981. They had licensed Bob Lipp's CMOS arrays, lined up masterslice suppliers, and were ready to try out their software. Unfortunately, no one wanted to be the first to give them an order.

ROB WALKER

One day Halfon Hamoi showed up. He is a rotund entrepreneur who had worked for Wilf at Fairchild and held him in great respect. At the time, Halfon was President of 3H, a power supply tester company. He brought me his requirements; they were low-volume, low-complexity–about the worst ASIC application I could imagine. After reviewing the logic diagrams, I told Halfon and Wilf that this was an inappropriate use of ASIC technology and not cost effective. I thought we should turn him down.

Wilf took me aside. "Rob," he said, "we've been busting our asses for three months trying to book a design. And you want to turn these down?"

Good sense prevailed and we took the order and went to work. It was fortunate the ASICs were so simple because we had to debug everything on those three designs: libraries, software, metalization, and test–everything had to be right. Richard Derickson and I did the logic design and simulation using

TEGAS. Jim Koford wrote an interface to our Fairchild Sentry tester so we could test the parts. Ed Jones had enough of his system running to interactively generate the physical layout. By Christmas 1981, less than a year after our founding, we delivered our first three prototypes. All of them worked the first time.

John Duffy, an old friend, was 3H's VP of Marketing and Sales. Potential customers would ask us for references, and after a lot of hand-wringing we would give him John's name. 3H was, in fact, our *only* customer, and after a while John got a little tired of this honor. After being paged in a New York airport by one of our potential customers asking for a reference on LSI, he called us. "I wish you guys would book some other orders!" he said. "I'm spending a couple of hours a day just giving you references!"

Fortunately, other business was coming on board. We had broken the drought. Thanks, Halfon and John. We owe you!

LSI LOGIC COMES OF AGE–1981-1983

10 We Do a Deal With Toshiba

It was clear from the beginning that LSI needed a Japanese partner to fabricate CMOS master-slice wafers. In 1981, the Americans and Europeans had competitive bipolar and NMOS technology, but were years behind the Japanese in CMOS. For example, the CMOS LC series of gate arrays was licensed by LSI from California Devices and fabricated for them by U.S. suppliers such as General Electric. The family had a maximum complexity of 1200 gates and mediocre speed. In the same period, Fujitsu had a much faster 4800 gate array. Wilf Corrigan and Conrad Dell'Oca left for Japan, hoping to do a deal with Fujitsu.

WILF CORRIGAN

At Fairchild we had licensed most of the major Japanese semiconductor companies over the years, and, since I was a known entity, their top people were willing to meet with me. In 1981, I visited the CMOS leaders Hitachi, Fujitsu, and NEC. In those days, Toshiba and Oki were not nearly as prominent in semiconductor technology but, covering all our bases, we went to see them and Mitsubishi and Sanyo as well. Our conversation with each of them was similar: "We're going into the gate array business with software tools which our customers will have in their own hands. What we need is a state-of-the-art CMOS process and someone to fabricate masterslices for us."

NEC wasn't that interested because, at that time, they had all the ASIC business themselves. We finally got to the point where Toshiba, Fujitsu, and Oki all were willing to do a deal with us, but with different degrees of enthusiasm. Fujitsu felt it already had good CAD software. When I talked to Yasufuku at Fujitsu and told him that our plan was to put the software in the hands of the customers, he said, "That is a brilliant strategy. If you do that and the software is good, you will win."

"Why don't you do that?" I asked.

"Our software is so valuable that if we expose it to outsiders, they will steal it."

In fact, they had been unwilling to transfer the software even to their U.S. subsidiary because they were convinced that once they let the genie out of the bottle, they would never get it back again.

After three days of negotiation, we were close to a deal with Fujitsu, but from our standpoint, the terms weren't very attractive. Finally, they wrote a contract. Yasufuku signed it, and pushed it across the table to me. "Well," I said, "I'm just going to have to go away and think about this."

We had already spent two days with Oki and were offered more or less the same deal.

Then we went to Toshiba who had a world-class CMOS process but no presence in the merchant ASIC market. Kawanishi, the number-two man in the semiconductor division, showed us Toshiba's three- and two-micron CMOS technology. The performance and density were impressive.

Toshiba was not your typical Japanese corporation; their management style resembled an American operation in that all the Toshiba guys had an opinion and felt free to argue with Kawanishi.

After the first day of discussion with Toshiba, my intuition told me to go with them. When I got back to the hotel, I called the LSI team in the United States. "Hey guys," I said, "change

of plan. I've got potential deals with Oki and Fujitsu, but I'm going to make a deal with Toshiba. What do you think?"

Stunned silence. Fujitsu had been the preferred choice from day one.

The Toshiba contract was remarkably simple. Only six lines long, it says that LSI and Toshiba would develop a family of two- and three-micron gate arrays. That was it. It worked remarkably well.

TSUYOSHI KAWANISHI

I was impressed by Mr. Corrigan's presentation. LSI Logic had very ambitious plans for the ASIC market. At Toshiba we had an excellent CMOS process and had done some preliminary gate array work, but we had no experience with the merchant market ASIC business. The agreement with LSI Logic allowed us to learn the ASIC business with very little investment.

WILF CORRIGAN

I think Kawanishi decided that LSI could be an important steppingstone in turning his process into products. While Hitachi, NEC, and Fujitsu were well established in the world semiconductor market, Toshiba was late on the scene. Toshiba had built factories but didn't have much to sell. What they had to bring to the party was their CMOS technology. They needed partnership with a wide variety of international companies that could offer new designs that could go into production. I have tremendous respect for Kawanishi, a real statesman and a long-term strategist. Now, Toshiba is a strong second to NEC in semiconductors and my guess is that, sometime soon, they will surpass them.

CONRAD DELL'OCA

Wilf hired me from Hewlett Packard to do the process R&D. As a start-up, we didn't have the resources to develop advanced CMOS technology on our own. When Wilf and I visited

Fujitsu, we didn't get what you would call a warm reception. They stuck us in an empty conference room with just a few hard chairs around a table where they made us wait for two hours. When they finally showed up, we put all our cards on the table, but they told us nothing; we didn't know what they thought–whether they were impressed or were just being polite. They probably felt that we didn't have much to offer, since they already had a strong gate array position and we could only give them better software and an entree to the American market.

Toshiba, on the other hand, was another story. In many ways they acted like an American company and they seemed to take us seriously. After we made our presentation to an interested audience of about twenty Toshiba people, Kawanishi went up to the board and wrote down the three main elements of our relationship: LSI would provide design assistance, Toshiba would fabricate the wafers, and we would second-source each other.

I've got to say that working with Toshiba was really great–easier, in fact, than working within departments at Hewlett Packard. Our negotiations with them went smoothly and they always delivered on time. After our agreement in February 1981, things moved quickly. We had our first design-review meetings in July; by October Ven Lee had the design done; and by the end of December, just before Christmas, we saw the first 5000 Series 3-micron wafers. The negotiations on unmetalized wafer prices, which came down to a price delivered FOB LSI for about $270 each, wasn't finished until they had been shipping wafers to us for about three months.

The 3-micron 5000 Series and 2-micron 7000 Series of arrays were more than successful–they became industry standards. In 1983, we started to plan the next family. I was pushing for a new architecture, the so-called "Sea of Gates," which I figured would give us an extra 15 to 20 percent gates per unit

area. I proposed the architecture to Toshiba. After evaluating the concept for nearly a year, they sat down with us to do a deal giving us CMOS manufacturing technology over the next five years in return for providing them with our new CAD and engineering technology.

The 1.5-micron effort started in early 1985. In June, we finished up the agreement, started the design process, and set the schedule for the 1.5-micron process transfer. At the end of the year, Cy Hannon, Vice President of Manufacturing at LSI Logic, decided to take his manufacturing managers, including me, to Japan to prepare for the transfer process. The trip really opened our eyes. What we saw changed our whole concept of manufacturing standards in the semiconductor industry.

Toshiba didn't accept U.S. standards of wafer yield: while we had been happy with 50 percent, they expected to lose, at most, only one or two percent. They also didn't buy our practice of "rework," and would only tolerate a few percent. In the seventies we taught Japan how to manufacture integrated circuits. In the eighties the Japanese taught us how to do it well.

A major reason for Toshiba's excellence in manufacturing is that its workers are highly trained. While American workers received minimal training–for most tasks, a few hours–at Toshiba, apprenticeship programs for operators and technicians on the line lasted anywhere from six months to several years. By superior training, and also by giving line people responsibility for producing quality products, they were able to achieve standards of excellence that we could only hope for in the United States.

We came back from that first trip convinced that we had better learn everything about their manufacturing process, so, for the next visit to Toshiba, we sent fifteen people from every discipline. During our four-week stay we developed a routine: during the day, Toshiba people would give us lectures; then during the evening, the LSI team would spend three or four

hours going over the material and generating questions for the next day.

Execution was the secret to their success: execution in keeping equipment clean, keeping the particle count down, and doing the process right. What we learned proved invaluable to our LSI manufacturing in the United States.

The advanced Toshiba process, our new channelless architecture, and a 225 percent area increase in maximum die size to 1.5 cm. on a side resulted in our 10,000 Series gate arrays. It was this product that simply blew the competition away. Not until 1990 did our competitors come up with comparable products.

VEN LEE

We didn't have a real product direction until Wilf did the Toshiba deal. Then I was heavily involved with them doing the 5000 and 7000 Series of gate arrays. I asked Isamu (everyone calls him Sam) Kuru of Toshiba, why they had done a deal with an unknown U.S. start-up. He replied, "I just had a good feeling about you guys"–hardly a typical Japanese approach.

Toshiba was atypical for a Japanese company–their approach was "ready, fire, aim" when they saw an opportunity, and they were far more open than most Japanese companies.

I remember the afternoon I hosted a barbeque at my home for Egawa, Kuru, and a number of Toshiba engineers. I presented Egawa with an apron emblazoned with the words, "For this I went to college?" He put it over his black business suit and went out on the deck to cook the meat. Later, during one of my trips to Japan, he had me and my wife, Jenny, to his lovely house in Tokyo for dinner.

The Toshiba people were great to work with. For one thing, they had minimal "NIH" (Not Invented Here) attitude. One of their biggest contributions was to convince us to take our largest die size from 1 cm. to 1.5 cm. on a side, thereby immediately doubling our maximum gate count. Literally no one was

building logic chips that size in 1985, and many people thought it was impractical. It subsequently has become routine for LSI and most other major semiconductor suppliers.

WILF CORRIGAN

Our business relationship with Toshiba gradually started to deteriorate. Until 1985, we were primarily an engineering company–50 percent of our revenues were engineering based, and that's how Toshiba wanted us to stay. I suspect they had a pigeonhole for us that looked something like, "You're an engineering company that just does the low volume, and we're the high-volume company. You do the engineering," they'd say, "and we will just do the high-volume stuff." No matter how much I told them that we wanted to be a high-volume semiconductor manufacturer, they'd say, "Well, we're just executing the deal that we've had since day one," namely that LSI would stick primarily to engineering.

I don't think they really quite understood why we were annoyed at their attitudes. As LSI started manufacturing ASICs in volume, Toshiba started bombing the prices, automatically chopping our price by 20 percent across the board. Not only was our business being attacked, we were competing with our own technology. We were on a short road to hell. It was time to break the second-sourcing deal.

We are still on good terms with Toshiba, and hope to do other ventures with them. International joint ventures are the wave of the future, and our Toshiba experience has taught us that we need to figure out how to make them beneficial to both sides. There should always be some provision for parties to gracefully back out if it isn't working.

TSUYOSHI KAWANISHI

On the whole, the agreement with LSI Logic was a plus for Toshiba. In 1981, Toshiba's ASIC sales were negligible, but ten

years later, Dataquest listed us as the world's second-largest ASIC supplier. We used the LSI agreement as a model for later cooperation with non-Japanese corporations such as Motorola, IBM and Siemens. Our relationship with LSI Logic also helped me understand American thinking and culture, and I've made a number of American friends like Wilf Corrigan and Bill O'Meara.

On the other hand, the agreement helped to create Toshiba's largest ASIC competitor, LSI Logic, and naturally there have been conflict and disagreements. On balance, I'd do it again.

11 In and Out of ECL

Emitter-Coupled Logic (ECL) was the highest-performing technology available in 1981. Although its high power dissipation and other costly attributes made ECL impractical for most systems, it was a favorite of the mainframe computer manufacturers and promised LSI Logic a high-margin, difficult-to-copy product line.

ROB WALKER

In our 1980 business plan, we were to have both CMOS and ECL gate arrays. The ECL decision was reinforced by the many mainframe computer companies who felt their future depended on another source for the Motorola ECL Macrocell array. Since Motorola didn't want to do a second-source deal with us, Dan Wong, our ECL Design Manager, "reverse-engineered" the Motorola circuit. Signetics signed on to diffuse the wafers and, by late 1981, we had working parts. But in the year it took us to develop and prove our ECL array, the market had changed–many ECL mainframe programs had been canceled or severely cut back. Motorola had solved most of their problems and surviving Macrocell customers didn't need a second source.

On to Plan B. We cut a deal with semiconductor manufacturer AMD similar to what we had done with Toshiba in CMOS. They (AMD) agreed to diffuse our base wafers and license our LDS CAD software and first-generation Macrocell array. In turn, Dan Wong would design a leadership ECL array that we both would market. They were delighted with the LDS software, the Motorola look-alike Macrocell array, and

eventually, the advanced, second-generation ECL array. They used them successfully for several standard products and a few custom programs. Unfortunately, AMD was our only ECL customer.

As the CMOS market was exploding, the ECL market was going to hell, so after much debate, we decided to quit the ECL business. We transferred all ECL rights to AMD where they had moderate success in standard products, and Dan Wong became our principal CMOS array engineering manager.

In retrospect, our design ECL group, Dan Wong, Tony Wong, Yen Chang, and others turned out to have the ideal skills for advanced CMOS. As performance and power dissipation of CMOS reached those of ECL, their expertise in transmission lines, power distribution, and 100 MHz-plus clock rates proved invaluable. Although our ECL effort stalled because we lacked customers, our work laid the foundation for LSI's advanced CMOS arrays with ECL performance.

12 Second-Round Financing

In LSI's first round of financing in January 1981, 60 percent of LSI Logic stock was sold to outside investors at 90 cents a share. After a year, LSI had a 50,000-square foot building in Milpitas that included a metalization fab, offices, and a large computer facility. They had also shipped their first CMOS ASIC prototypes. It was time to bring more money into the company with a second round of financing.

WILF CORRIGAN

We decided we'd need to raise more money. We started talking with our first-round venture capital investors and they said, "You're right, it's time to raise money and we'll put some more in at $3 a share."

"No, we want $10 a share," I countered.

"You're crazy! No way are you going to get it; we won't pay it and nobody else will either," they said.

"Listen, let me try some outside investors," I said.

"This is ridiculous, but go ahead and waste your time," they replied.

At an AEA Meeting in Monterey, a young guy I hadn't met before took me aside. "Hey, I could help raise some money for you," he said. "How much do you want?"

"We want to raise about $10 million at $10 a share," I said.

"Yeah, I think I could do that."

"Well, who are you?" I asked.

"I'm Arthur Trueger and I have a consulting company. I've done work with Intel and consulted with a number of venture

people, but now I'm going into the venture business myself. I've got good connections with the major British institutions and they want to invest in Silicon Valley."

"Okay, how many trips to England do you think this is going to take?" I said.

"Only one. If you get into London on Monday, we'll have our meetings on Tuesday and Wednesday, and we'll probably have it all wrapped up by lunch on Thursday."

I thought, this sounds crazy but what the hell! Let's give it a try.

Arthur took me around to a number of British institutions. As in our first round of financing, I think it helped that I was a Brit; they knew me somewhat from the Fairchild days, so at least I wasn't some wild American. By Thursday, I had a commitment for 75 percent of the second round on their one condition that past investors would come in for 25 percent.

I flew back to Milpitas and had our Board meeting; I hadn't had a chance to tell the Board about my meetings with Trueger. We got into a discussion of second-round financing. "Well, I've come to realize that you guys are right," I said. "The $10 price is too high–we should really do it at $8."

"That's nuts, there is no way you can get a valuation that high," they said. "If I can get the other 75 percent of the second round from other people at $8, would you come in for 25 percent?" I asked.

There was a lot of discussion. Tom Perkins finally said, "Okay, if it can be done, I'll go along." Don Valentine reluctantly agreed: "If you can raise the other 75 percent, we'll come in for 25 percent and if you can raise the money at that price," he added, "I'll erect a statue of you."

"And I'll gold plate it," Tom said.

"Well, that's fine, I've got the other 75 percent. It's done." They damn near fell off their chairs in shock. Later, they presented me with a gold-painted plaster Buddha.

Just in case the venture capital didn't come through, I'd been negotiating with an old friend of mine, Fred Breneel, the

Chairman of Johnson Controls. I asked Fred if he would be interested in investing in a semiconductor company. Johnson's major competitor, Honeywell, had invested in Synertek, which had done well for a while. I suggested that, should this become an important strategic advantage, why not buy a modest insurance policy by an association with LSI Logic. Fred said he was watching what Honeywell was doing, but his gut feel was not to make a major commitment in unfamiliar waters. "We are not really an electronics company," he said. "We're a controls company."

"Well look," I said, "why not hedge your bets here? If you would guarantee our lease line, we'd give you warrants; that could be your way of having your toe in the water; if you need strategic advice, you could always use us. If the Honeywell strategy is correct and suddenly it becomes important for you to have a major semiconductor position, you can come in more heavily later. It would cost Johnson Controls half a million to a million dollars of equity and guarantee a $10 million lease line; your only risk is if we go belly-up and then all our equipment would have to be sold for whatever its market value. You could potentially lose $5 million on the deal. Personally, I think that Honeywell could be getting ready to take a bath for maybe $100 million and I think it's really high risk going heavily into the semiconductor business. So buy some insurance."

"Okay, I'll do it," Fred said, and sent out Jim Keyes–at that time the Financial VP, but now CEO of Johnson Controls–to arrange the details.

Either deal would have carried us for the next year, but as it turned out, we got both: we raised the $10 million second round and we got the Johnson lease-line guarantee. That got us set up for the rest of 1982 and positioned us to go public offering in 1983. It is always advisable to have a Plan B, and sometimes you get lucky and end up with both A and B. This was one of those times.

13 Digital Equipment– TI's Stumble Opens a Market

Digital Equipment Company was to become LSI's largest customer in the mid-eighties. Initially, they were wary of the little West Coast company with its unfashionable CMOS technology. Wilf Corrigan, Bill O'Meara and Rob Walker visited Digital in January 1981; the meeting did not go well.

WILF CORRIGAN

I knew several guys in the purchasing establishment at Digital and that got us in the door in January 1981 to tell our story.

"Your pitch is all very interesting," they said, "and we're impressed with what you guys are doing, but it's not for us. CMOS isn't appropriate for minicomputers, but good luck anyway."

Months later, we got a call from Digital and were told that Gordon Bell, Senior Vice President of Engineering, would be in California and wanted to visit LSI. He was only supposed to meet with us for an hour, from 8:00 to 9:00 in the morning, but the discussion ended up going into the evening. "Guys, you've convinced me that there's a major sea change in the industry," Gordon said as he was leaving. "I'm going to take action."

Shortly after the meeting, he sent out an internal Digital memo that effectively said, "Okay, on the assumption CMOS is radically changing the way we design computers, I want all 15,000 Digital engineers to re-evaluate their programs."

After that, Digital sent a small army of engineering and purchasing guys, some hostile and some friendly, to evaluate us.

Skeptical, but technically thorough, they were on survey missions. Shortly after that, we got a call from Digital requesting us to quote on the "Falcon" chip. We knew we were competing with four or five other ASIC companies. Digital had a worldwide engineering meeting scheduled for December 1982, and they wanted to hold up a simplified single-board computer using the Falcon ASIC and contrast it to the TTL board it would replace. I think Digital felt they were falling behind in their level of integration and needed to reduce costs.

This was a tremendous opportunity for us to prove ourselves. Rob redesigned the Falcon TTL functions into our CMOS library, Julie Chen worked all night doing the layout, and we sent the quote back with the full chip layout. Digital was impressed and we got the contract.

ROB WALKER

We shipped the Falcon ASIC and it worked the first time, proving to Digital that we could come through quickly and accurately. Nevertheless, Digital selected Texas Instruments for their new generation VAX computer. We pointed out TI's mixed record on ASIC and the technical risk of their bipolar STL technology, but as TI had been a long-term supplier to Digital and had actually delivered a few STL prototypes, Digital remained loyal to them.

One afternoon at 6:00, 9:00 their time, we got a call from Digital. TI had just told them they were decommitting their bipolar STL arrays and canceling the program, and Digital wanted a team from LSI on a plane immediately to explain how we could bail them out with a CMOS solution.

TI's debacle gave us a huge boost and made us Digital's primary gate-array supplier. In addition, bipolar ASICs were recognized as inferior to advanced CMOS, and we became a preferred supplier to the computer industry. TI's stumble allowed us to become a major force in ASIC.

We were also able to bail out the government-sponsored VISIC program which had attempted to get advanced ASIC into military systems. VISIC technology was in trouble and delaying many critical weapons systems. Our 2-micron, 7000 series family of CMOS gate arrays quickly saved many military projects. CMOS gate arrays were replacing both bipolar and full custom-handcrafted MOS technology. Just as TI's problem catapulted us into the computer industry, the failure of VISIC made LSI Logic the pre-eminent ASIC supplier to the military and aerospace industries.

14 LSI Marketing– The Bulldog Approach

When you are an unknown start-up, marketing and sales are particularly important. Fortunately, LSI had the best: Bill O'Meara, Bob Blair, Keith Lobo, and Perry Constantine, among others. Every LSI design engineer understood he was key to the company's success. Nearly everyone came to work wearing ties, which was not the usual Silicon Valley dress code. Tiny LSI wanted to look like IBM.

BILL O'MEARA

When three or four Hughes people visited us, they came hat in hand. They had five designs they wanted us to prototype, but they couldn't guarantee production unless they won the government contract. We were astonished to see a major customer apologizing; evidently our competitors wouldn't even talk to them.

I thought, wait a minute, we have a chance to do something here. And so I told Hughes that we would charge them a healthy fee for engineering, but would not require a production commitment. You could almost see the tears well up as though we had hit an exposed nerve. A plan began to take shape. If this arrangement could work with Hughes, the leading electronic defense contractor in the United States with its own semiconductor capability, it could work for every military customer. Our experience with Hughes validated Rob's strategy of separating design from production, and differentiated us from AMI, CDI, and other ASIC suppliers.

PERRY CONSTANTINE

In the early days, getting a customer to sign off for a $25,000 design felt to us like $25 million. We had convinced the engineering guys at Two-Pi, a local computer company, that doing a CMOS array design instead of a bipolar array was the right approach, but when our sales rep and I met with the purchasing manager he said, "You're too late, we've already placed the business with somebody else."

"Who do we see to change your minds?" we asked.

"The Vice President of Engineering and the Director of Purchasing," he told us.

I called their Director of Purchasing, promising that we would have our LSI management team at their facility the next day. He was astonished. "But tomorrow is Christmas," he said.

"That doesn't matter," I said. "We'll be there."

"Well," he said, "if you're so eager, I don't mind coming down."

Christmas day I called Bill O'Meara and Jack Higbee, pulling Jack out of the shower. "Jack," I said, "you've got to be at Two-Pi in two hours to give a presentation."

"Just give me a chance to dry myself off and put on my suit," he said.

So we gave our presentation and got the order. I left the meeting thinking that LSI was the only company I had ever worked for that could have gotten senior management out of the shower, dressed, and at a customer's facility on a few hours notice on Christmas day for a $25,000 design.

This incident typified the high energy and commitment we were pouring into the business. We had to convince the customer that LSI Logic was the wave of the future, then explain this new, not-very-well-understood technology called gate arrays. Our sales force was like Mormons on their bicycles, knocking on your door to try to sell you a Bible.

At our first WESCON show in Anaheim we were going to demonstrate our LSI design tools. Since we couldn't afford a booth, we booked a hospitality suite. "How are we going to get the workstation down to Anaheim?" Myke Connell asked me.

"I haven't thought about it," I said.

"Well," he said, "we've gotta be there by tomorrow."

"I have this big Chevy Suburban; why don't we drive?" I suggested.

We took the Suburban to LSI and loaded it up. Phil Pfeifer, Myke Connell, and I drove nonstop to Anaheim and set up the hospitality suite ourselves. During the show, the suite was packed with customers excited about the LSI ASIC message. We were a hit.

LSI GOES INTERNATIONAL

15 Entering Europe

Since LSI Logic had done so well in the U.S., attention naturally turned to the European ASIC market. Wilf Corrigan and Bob Blair were both Brits, so the focus fell first on the United Kingdom.

WILF CORRIGAN

We saw the worldwide ASIC market as a triad made up of the United States, Europe, and Japan. If LSI had waited until everything gelled in the United States and then decided to do something serious in Europe, we never would have gotten off the ground. Inevitably, one of the European semiconductor companies would have seen what we were doing in the United States and replicated it. Even if they weren't as good, they would have been seen as the innovator and our little American company as an also-ran. We had to move immediately or lose the market.

We wanted to participate in foreign markets, but we didn't want to spend a lot of our own capital. Our experience at Fairchild taught us how expensive it was to operate marketing, sales, and manufacturing in Europe. This was a unique opportunity to take the American start-up model overseas.

We came up with a plan to clone ourselves and use a venture capital approach to finance LSI Logic Limited. Eventually, we got Europeans to invest, and by the summer of 1984, we raised a total of $10 million in return for 18 percent of the European company. As the operation grew we got a lot of long-term, low-interest loans to cushion the P&L effect of starting up our European operations.

BOB BLAIR

I was born in England and grew up there. In 1966, I graduated from college with a degree in applied physics. I started as a process development engineer at Marconi, but after a few years I decided the white coat and laboratory were not for me.

Fairchild was expanding its European operations and advertising for product marketing engineers at their headquarters near Frankfurt. Even though I knew nothing about marketing or electrical engineering, I thought I had a shot at a job since I was a physicist already working in the semiconductor industry.

I interviewed with Ralph Bennett and Doug Usher at Fairchild and they offered to make me the transistor product marketing engineer in Wiesbaden, West Germany. My new salary was twice what I was paid at Marconi. I packed a suitcase, got in my MGB, and drove off to work in Germany. I'd never been there before.

I arrived the day America landed on the moon. Unlike the astronauts who were trained for their mission, I got the classic introduction to American high tech: "This is your job, this is your desk, that's a salesman, here's some prices, and off you go."

In six years, I became Fairchild's product marketing manager for Europe, where I remained until 1976 when I returned to the United Kingdom as Fairchild's General Manager of Marketing for Northern Europe. I was promised a job in the United States, and after living two years at the Holiday Inn in London, in 1978 I moved to California as Fairchild's European Marketing Manager.

Fairchild was doomed as soon as Schlumberger acquired it in 1979. Schlumberger was a hugely successful oil field services company with an almost perfect P&L and balance sheet. Their business philosophy for Fairchild totally changed the flavor and attitude of the company. Schlumberger mistakenly believed it could transfer its oil-patch culture and business strategy to Silicon Valley to turn around our "ailing, sorry semiconductor

company" and at the same time capitalize on the semiconductor technology to enhance their petrochemical business. It was clear to all of us that Schlumberger's plan was a disaster. Wilf Corrigan resigned very soon after the acquisition, and I stayed around for another 18 months deciding what to do with myself.

That problem was solved when I was invited to a party at Bill O'Meara's house. Bill told me something was cooking and I might be interested, so "watch this space." A month later, LSI Logic hung up their shingle, and I paid a call on the four founders.

This was a good opportunity. I joined LSI after arranging to be fired from Fairchild–they called it "reducing overhead"–meaning getting rid of anyone who was still left at headquarters. When I arrived at LSI, the company was only a little beyond the founding stage. I didn't know the first thing about ASICs, but I was impressed by LSI's two brilliant CAD guys, Koford and Jones. A small but select group, we quickly got to know each other well.

LSI was a new era for me. I had come from the classical standard-product world of the seventies and this was my first experience working in a start-up where there were no systems and plans in place. Everything was done on the fly as needed. Rob, Bill, and I defined the product line, identified potential customers, and developed a sales strategy. By the middle of 1981 we recruited Keith Lobo for marketing, and Dave LaRock as our first salesman–both from Fairchild. We were a close-knit group where everyone was willing to pitch ideas and concepts, but in the end left the execution to the individual with the experience to carry it through.

Besides the basics like data sheets, reps, pricing, backlog, and order-entry, we had to tackle broader issues like manufacturing. Do we need a factory? Yes, we do. Where are we going to put it? In the high-rent district or the red-light district?

We chose the red-light district of the time, Milpitas. Wilf and Jack Higbee were driving around what used to be farmer McCarthy's ranch and came across this 50,000-square foot building in the midst of the onion fields. This building was so ugly and located in such an out-of-the-way spot, they figured that it had to be cheap. It was.

Eventually we got used to the unfashionable Milpitas address. Our building became the basis for developing the company's "larger than life" image. It had more square footage than we needed, but it made us look real to customers. If the ASIC didn't work properly a user didn't have a product, so in those days, no customer would give you an order for an ASIC without first visiting the factory. We could show them a large clean-room manufacturing area, even though we weren't doing much manufacturing then. We had some fab equipment in place and we had people around wearing bunny suits, who talked the silicon manufacturing language. Suddenly, we appeared to be a serious semiconductor company rather than a start-up with pencil and paper.

As we went into 1982, we started to book orders with real customers. Most were unknowns, but we did land some contracts with majors like IBM and Digital. The track record of the LSI founders made them feel that they had little to lose and everything to gain by giving us some small orders for noncritical circuits. For some of the smaller companies, on the other hand, we were essential for their success. In effect, we had these smaller companies held hostage. We were glad and lucky that we could deliver on most of our promises.

As it became apparent that the half-life of the ECL market exceeded how long our money would last, we realized that CMOS technology was our future. Ven Lee and Conrad Dell'Oca believed that CMOS could rival the performance of ECL; everyone agreed so we bet the company on that premise.

To make ourselves big, we pursued major customers. At the time a group of computer companies–Control Data Corporation (CDC), Nixdorf, Olivetti and others–got together as a defense against IBM. They called themselves Standard Computer Komponenten GmBh or STACK for short. In 1981, Ed Jones and I managed to get invited to a STACK review meeting held in a chateau in the Italian hills. We told them we were going to have a wondrously integrated CAD environment: Schottky-speed CMOS, two-layer metal, 6,000 gates now, 10,000 gates soon. They were skeptical. They recognized that we had a lot of water to push uphill.

One of the senior CDC guys politely told Jones that they had spent millions of dollars and ten years trying to develop what we were saying we were going to do on a shoestring in six months. Jones just smiled. The STACK attitude was, don't call us; we'll call you. What they didn't realize was that a few smart people could outperform their enormous bureaucracies and outdated technologies.

LSI became the guy to beat in CMOS gate arrays. Our 3-micron two-layer metal 5000 Series product was rapidly followed by our 2-micron two-layer metal 7000 Series product which we announced concurrently, but manufactured consecutively. Our 7000 Series 2-micron product turned out to be an industry standard and we continued to gain momentum.

Many pundits were promoting cell-based and silicon compiler products as being smaller, faster, and more customizable than gate arrays for ASICs, and therefore would obsolete our products. But they were wrong. They didn't consider that gate arrays are easier to design, manufacture, and get to market on time.

We had a hell of a growth rate. Sales were negligible in 1981, but we sold about $5 million in 1982, $35 million in 1983, and, in May of 1983, we went public. We achieved a valuation on the company of $600 million based on $5 million

in the first quarter of 1983. After the IPO, cash was plentiful, but we still had to watch the P&L. In 1984, revenue more than doubled to $84 million.

Now that we were successful with small and large customers, we were confident about our strategy in the U.S. We were now *the* U.S. leader in ASICs. Customers were even coming from Europe to visit us.

Since 1981, I'd been acting as the International Sales Manager, booking a few orders here and there from high-quality European companies such as Telettra, GTE, Nixdorf Computer, ICL, and IBM in South France.

It became apparent that we ought to expand our operations in Europe, but even though cash was available in the United States, we really didn't want to spend it in Europe. So we decided to clone our American operation. We would take the LSI product line and set up design centers close to our customers' operations. The design centers would have hands-on design capability that could directly emulate what went on in Silicon Valley so that the customer did not have to take a day-long flight just for the privilege of doing business with us. At this point, Europe was still very much a virgin market with no clear leaders in the ASIC business.

The Thatcher government had reduced corporate taxes in the United Kingdom so we established our holding company there. I went to Europe in April 1984 and four months later, LSI Logic Limited was founded.

Our European company was structured differently than previous American semiconductor companies. National and Fairchild had gone to Europe with wholly-owned subsidiaries, primarily sales and marketing operations. What manufacturing they did reported back to the states. We had a different strategy. We intended to be a real European company with European investors owning 20 to 30 percent. That way we could fund

it with European money, while keeping the U.S. company in control.

We went to the London market to raise most of the money. Our business plan specified that LSI Limited had an evergreen technology license with its parent in the United States, and offered growth, reasonable profitability, and a long-range objective to take the company public on the London exchange. Sulzer AG in Switzerland saw this opportunity to bring electronics into their company and became an investor. Our plan and the lack of serious ASIC competition in Europe at the time allowed us to sell the deal in London and in other markets.

We raised about $10 million for 18 percent of the European company, enough to establish our design center structure. Where to locate them wasn't a problem. We established our new centers where the customers were, and we quickly set up a hub design center and European company headquarters in the United Kingdom, and a base in Germany. Horst Sanfort, whom I hired to head the German office, agreed that Munich was the right place to establish a design center in Germany. After Munich, we opened centers in Paris, Stockholm, and Milan.

We felt that Israel was important because it has a large military market and, since in the United States LSI had led the field in military ASICs, it was a logical move to set up a design center in Israel.

Staffing our international design centers with locals made communication with customers easy. Since we had already established relationships with major European companies, we quickly dominated the European ASIC market.

16 Expanding to Japan

After successes in the United States and Europe, Wilf Corrigan next turned his attention to Japan. Would it be possible to clone another LSI Logic in a market notoriously adverse to outside investment?

WILF CORRIGAN

Early on, we had a sales representative in Japan, but after three years he hadn't booked any business. We felt we had to do something really serious to have an ASIC position in Japan. Our successful U.S. and European start-ups had proven that a small team of bright, motivated people with a piece of the action could out-gun much larger competitors. Prevailing opinion was that you couldn't do a Japanese-based start-up, but we thought, if it worked in the United States, why the hell wouldn't it work in Japan?

When we researched it, we found that Japan is an entrepreneur's paradise in that they have minimal business tax and very close to zero capital gains tax. A Japanese businessman can't earn enough salary to get rich, but if he can somehow get a piece of a start-up company, he won't pay any tax on the capital gains. You'd think that in that kind of environment there would be thousands of entrepreneurs, but there aren't. A fledgling venture capital industry had just begun in Japan but was starved for entrepreneurs.

After our U.S. public offering, I went to Japan to meet with the president of Nomura, the number-one investment banker in Japan. "Would you like to come and speak to some of our

people about your LSI Logic stock?" he asked. I grabbed my slides expecting a fireside chat. I was amazed when he led me into an enormous lecture theater complete with a large screen and a translator. There must have been 200 Nomura people in the theater sitting there with pencils poised over their notepads. "We brought in all of our regional sales directors from across Japan because we are very interested in American high-technology companies," he said. "A significant portion of your IPO went to Japan and these guys are ready to start selling LSI stock tomorrow." It struck me that there was a huge untapped demand here.

After I gave my lecture, I asked the Nomura guys, "What do you do in venture capital? Is there a market for raising money?"

"Well," they said, "there could be, but we're having trouble finding the right companies."

"Supposing we set up an LSI Logic Japan and sold around 30 percent of it to Japanese investors, and then take it public here sometime in the future?" They liked the idea and introduced me to the key people in venture capital, insurance, and banking.

Every time I went to Japan I made it a point to see Mr. Inamori, a major supplier of our ceramic packages and an original investor in LSI Logic, to brief him on LSI. "We are planning a Japanese company," I said, "and we've got about 20 investors lined up."

"What about me?" he said.

"You know," I said, "you really helped us a lot in 1981 when you invested in the first round, and I didn't think that it would be appropriate for me to ask you for more."

"No," he said, "here's my million dollars," and plunked another million into the pot.

We raised about $25 million in cash (4.5 billion yen) in return for 30 percent of the company based on a business plan

and LSI's previous four years' performance in America and Europe. This was probably the first time that a company was financed in Japan on just a prospectus.

I was in a quandary. I'd spent a year talking with Keiske K. Yawata (everyone calls him K.K.), President of NEC America, trying to persuade him to come with us, but I knew we had to have something concrete to recruit him. To raise Japanese funding, I was telling everybody that we were going to have a well-known Japanese CEO as president, but I couldn't say who it was. I was pretty sure that eventually K. K. would make the decision to come–I just didn't know when. I had a backup candidate, but K. K. was my number one choice. He was very smart, knew the Japanese industry well and, from his experience in the United States, could relate to an entrepreneurial company.

Once we had the money, I really put the hard sell on K. K. I had to visit his boss and his boss' boss several times. It was just like asking for a woman's hand in marriage–you go and talk to her Dad and announce your intentions.

The Chairman of NEC, Dr. Kobayashi, is a very distinguished man who had been in the industry many years. I'd known him a long time because Fairchild had a history with NEC. I asked him if he would let me hire K. K. Yawata, but he refused.

K. K. YAWATA

My father was quite unusual. He was one of the first Japanese businessmen with a background of Western business practice and culture. He had spent his twenties overseas, including six years in London where he acquired proficiency in English, which he passed on to me. In addition, we were raised Episcopalians, and so our family culture is Christian.

I majored in communication engineering, but I was more interested in the components that made electronic communication feasible. Toward the end of my studies, the transistor was

introduced and I thought it was going to be the hero for the next few decades, so I decided to concentrate on semiconductors. My professor advised me that NEC would be the best place to go. After a few years at NEC, I decided to come to the United States to study quantum electronics and solid-state technology. I went to Syracuse University on a Fulbright scholarship, got my M.S. in 1962, and went back to Japan and NEC.

I've spent most of my career around transistors and integrated circuits. I had quite a few "firsts" in semiconductor manufacturing: I managed NEC's first clean room and I supervised the design of their first automatic wire-bonding equipment.

In 1973, I was invited by a senior NEC executive to head an international marketing group for semiconductors. Finally, in 1981, NEC appointed me Executive Officer of NEC Electronics where I was responsible for developing products, manufacturing, and marketing ICs for the U.S. market.

I met Wilf Corrigan for the first time in 1975 when he came to Japan as a CEO of Fairchild. After that, I would see him at least once or twice a year. When I came to the United States to head NEC Electronics, Wilf and I decided to meet quarterly to discuss semiconductors. We often met for dinner at Chantilly in Palo Alto or Barbarossa in Redwood City.

In early 1982, Wilf confided that he was starting an ASIC company in Japan. He explained how he was going to finance it with Japanese money, but he didn't tell me right away that he was trying to recruit me. I asked him a lot of naive questions about the Japanese financial market and I was impressed by the research he had done and how much he knew.

He also convinced me that if I continued to work for NEC, I would spend all of my personal "capital" accumulated over my career with not much to show for it when I reached mandatory retirement. But if I invested my experience and leadership in a start-up in Japan, my "capital" might grow ten or even a hundred times. Then he invited me to join LSI.

Besides the potential of a Japanese IPO, the most attractive aspect of LSI Logic was its CAD development tools–exactly what I had been looking for since the seventies. I had asked NEC engineering to come up with similar design tools. They tried, but their software was hard to use and wasn't offered to the customer. LSI Logic's practice of training customers and making the software easy to use was appealing. In April 1984, I decided to join LSI.

Wilf visited with Dr. Kobayashi, the Chairman of NEC, and asked him to approve my moving to LSI, but he wouldn't hear of it. So I spoke to my boss, Dr. Ouchi, in June 1984. "You can't be serious," he said. I told my bosses at NEC that I was determined, but they just didn't accept the idea.

WILF CORRIGAN

When Kobayashi refused to give K. K. approval to leave NEC, I went to Inamori for advice. Inamori is a self-made man. In Japan he's a maverick. He's the "raised nail" they couldn't hammer down. He started small and he went his own way against the establishment, and he is now a multi-billionaire. His chain of jewelry stores illustrates my point. He had developed a process to manufacture artificial gemstones such as rubies, emeralds, and garnets. When the established jewelry infrastructure resisted his products, he simply set up his own chain of retail jewelry stores. In addition, he has now set up the Inamori Prize, the Japanese equivalent of the Nobel Prize.

"I think Mr. K.K. Yawata should head LSI's Japanese venture," Inamori said. "Arrange for me to talk with him, and I'll see what I can do."

I called K.K. "Let's get together with Inamori and have dinner," I suggested. "He's going to try to persuade you to take the LSI Logic job because he feels it's the right thing for you personally."

He didn't think it would do much good, but since he had always wanted to meet Inamori, K.K. reluctantly agreed to the meeting. I had them both to dinner at my house in Atherton, and afterwards we sat down to talk. Like many Japanese businessmen, Inamori doesn't speak much English but he understands it very well. He pointed to his interpreter. "He will translate for you," he said. Then he turned to K.K. and talked continuously for an hour in Japanese with the interpreter whispering in my ear. I was just a spectator.

At the end of the evening, just as he was getting into his limousine, Inamori turned to me and said, "He'll come."

K. K. YAWATA

Inamori convinced me I ought to take the chance on a start-up, but he warned me that it wouldn't be easy to leave an established company like NEC. "You must accept the fact that you may not be able to walk in the dark." It's a Japanese expression meaning that if you go against the norm, you risk becoming a social outcast. I sent a registered letter to Dr. Ouchi which said, "I have made my decision and I'm leaving; I'm not reversing that decision." Dr. Ouchi finally took me seriously and accepted my resignation.

I joined LSI Logic in December 1984. In 1985, we set up offices, bought computers and hired sales, marketing, and engineering people in Japan. We were large enough to generate $50 million a year in NRE alone.

We were disappointed that our CAD tools were not initially accepted by major potential Japanese customers. Many had their own ASIC and CAD capabilities and were unmotivated to try something new. Quite a few smaller companies, however, were able to understand our value and committed to us. Aside from NEC, which early on recognized the value of our CAD tools, it took us about four years to gain acceptance from major

Japanese firms. They had seen so many American companies come and go that they didn't want to commit to a start-up with no history in Japan.

The Japanese don't like to buy high tech products not manufactured in Japan since they feel that foreign manufactured products are of lower quality. In 1987, in a joint venture with Kawasaki, we built a Japanese wafer fab and proved we were committed to the Japanese market.

It was no coincidence that LSI Logic K.K. became profitable in 1987. Besides the new fab which showed that LSI was more than a design and marketing operation, the Japanese-American trade agreement gave us a tailwind.

Our Japanese customers are rightfully confused as to whether LSI Logic K.K. is Japanese or American. We're really both. We're a Japanese company because we're funded by Japanese investors and all managers and employees are Japanese. We do our business including all data sheets, catalogs, and documentation entirely in Japanese and, most importantly, we do our manufacturing in Japan.

On the other hand, since 1986 when the Japanese-American Trade Agreement was signed, it has been an advantage to be an American company. Since LSI Logic Corporation in the United States is LSI Logic K.K.'s majority stockholder, we started flying the stars and stripes next to the Japanese flag. Manufacturing in Japan gives us Japanese costs and quality, yet for purposes of the trade agreement, our products are counted as American. It's a perfect combination–if a customer buys from LSI Logic, they are buying from an American supplier, and yet the ICs are designed and manufactured in Japan. So we switch our hat back and forth–Japanese or American–depending on the circumstances. This is one of the few times that an American company has been able to do in Japan what the Japanese have done so successfully in America.

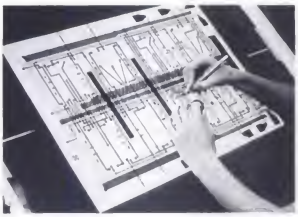
The Japanese have always been a tough market for us since our biggest customers are also our largest competitors worldwide. Most of our customers in Japan have in-house ASIC capability that we compete with. But we do have a number of advantages: our "right-first-time" delivery, our libraries–probably the most extensive in the world–and our level of integration on a single chip. In 1985, when LSI Logic K.K. started, no one else in Japan had 10,000 gates on a chip, and we have continued to lead in chip complexity.

Our state-of-the-art design environment and design tools also put us ahead. Integration of levels of 100,000 to 300,000 gates means that an ASIC now is made up of CPU, memory, peripherals, and whatever else the system requires. We have cells in our library covering all of these existing chunks of logic, including RISC microprocessors, graphic processors, DSP, and a lot of peripheral and I/O controls. The system designers can design their ASIC using familiar functions.

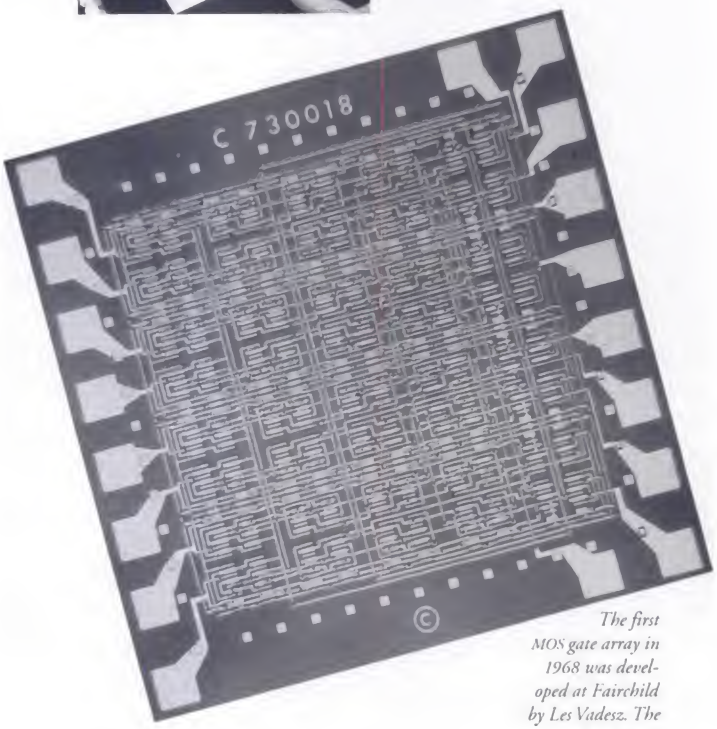
To continue to get the business, we need to expand our intellectual property by enriching our library with special-purpose functions. We must understand the usage so that we can intelligently group circuits for unique applications. To supply circuits for image compaction or video applications, we must understand video systems such as camcorders, TVs, VCRs and video terminals. Traditionally, ASIC manufacturers don't have that expertise. I think it's important that LSI Logic continue its acquisition of systems expertise by hiring systems engineers and by forming alliances with systems companies. That has motivated me to get very close to a customer like Matsushita (known as Panasonic in the United States) which has strong video capability. Once we understood the systems aspect of the application, we have expanded our capability to other video applications and are now working with Sanyo on an HDTV chip set.

The Japanese don't do business on a short-term basis. In Japan, you don't just sell products or technology. You must

create a long-term relationship which Japan has a tradition of honoring. If you cultivate a deep relationship with your Japanese customers and cherish them, they will tell you their plans, so that you can intelligently plan your products. And if you invest in equipment and facilities, many Japanese customers will assume responsibility to use them. At LSI Logic K.K., we are beginning to enter these kinds of relationships with major customers like Matsushita, Oki and NEC.

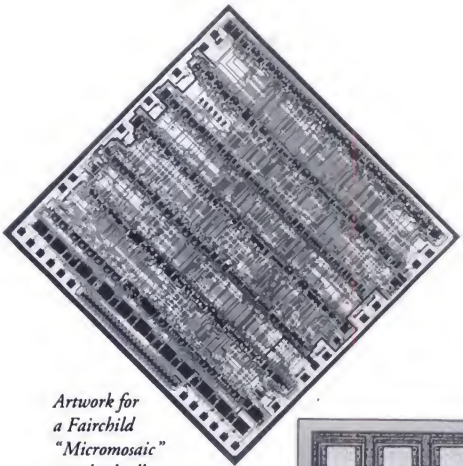


Taping gate array interconnection artwork by hand in 1967 at Fairchild. This task was automated by Ed Jones the following year.



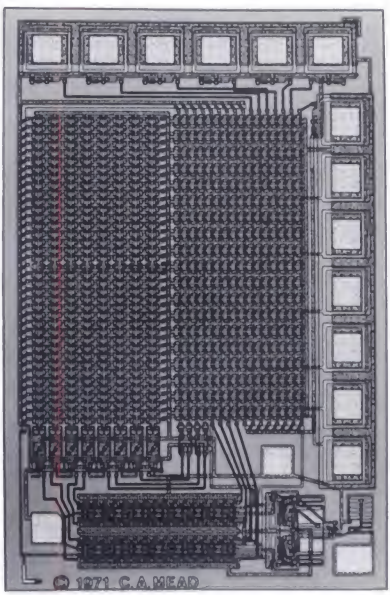
The first MOS gate array in 1968 was developed at Fairchild by Les Vadesz. The ***two-level metal interconnection process was not compatible with MOS and we never got working parts.***

The 1970 Fairchild CAD group that largely set the ASIC paradigm for the eighties. Top row, left to right: Ron Barry, Jim Koford, Henry Sun, Jack Crawford, Ed Jones, Ed Porter, Pete Jacobson, Ralph Bestock. Bottom row: Bill Jensen, Julie Mikalian, Daniellie Hollander, Judy Borssicut. Hugh Mays, the Department Manager, is in front.



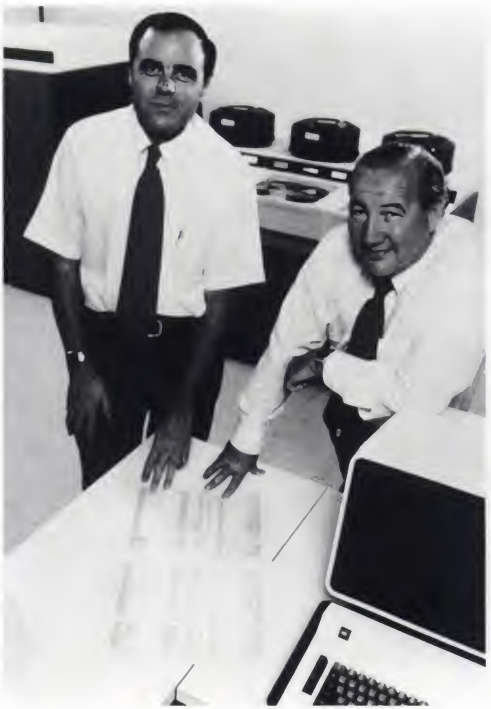
Artwork for a Fairchild "Micromosaic" standard cell design circa 1971 as generated on an IBM 360/67.

The first "silicon compiled" IC. Designed in 1971 by Carver Mead, the compiler took as inputs the number of inputs, outputs, min-terms and other parameters plus a state transition table and automatically produced the design.



An early Intel ad extolling the virtues of their microcomputer to replace standard logic and ASICs.

Bob Blair (standing) tries out the first LSI Logic presento, circa 1981. Counter clockwise from Bob: Ven Lee, Mick Bohn, Dan Wong, Skip Fehr, Wilf Corrigan, Conrad Dell'Oca.



Wilf Corrigan (right) checks out LSI Logic's first mainframe in 1981. Jim Koford on the left.

The first LSI Logic ad as it appeared in Doug Fairbairn's "VLSI Design," 4th Quarter, 1981. The headline says, "Get Involved, Start Now" because we didn't actually have working silicon at the time.

A modern LSI Logic gate array from 1991. The two large blocks are embedded RAMs.

The LSI Logic founders accept the 1986 Entrepreneurial Company of the Year Award from Standford Business School Alumni. Left to right: Mick Bohn, Wilf Corrigan, Rob Walker, Bill O'Meara.

17 Heading North to Canada

Founding the U.S. company, then going public, LSI was on a roll. Then LSI cloned the U.S. company in Europe and Japan. International employees had founders stock in their company and investors had the hope of a public offering, in London and Tokyo as they had done in the U.S. LSI was becoming the McDonald's of semiconductors.

MICK BOHN

After putting together the Japanese deal, I came back to the United States. Some people from Canada expressed an interest in attracting a semiconductor company to Canada, so Jay Shin and I went to Canada with a business plan. We negotiated a $26 million government grant, paid over three years, to establish LSI Canada. Then we set up six design centers and grew the business. After our third year we had revenues of $30 million and took the Canadian company public on the Toronto exchange. The objective of all of the LSI foreign affiliates was to go public when the time was right.

WILF CORRIGAN

Here's another case where the local government said they wanted high tech jobs and a jump-start to their educational system, and were willing to spend government money. It worked. They got the jobs, they got the expert education, and they got an indigenous ASIC capability. So often, governments dump their money into crazy operations like INMOS, and it's lost.

PERRY CONSTANTINE

Mick thought there was an opportunity for us to do an affiliate company in Canada along the same lines as our other affiliates in Europe and Japan. At the time, representatives of the Alberta government were in California looking for companies to transplant to Canada to expand their economy beyond oil and lumber.

After we did the deal, LSI Logic set up a small metal fab at the University of Alberta in Edmonton. The license fees we received from the University were then used as the seed money to start the Canadian company. After Mick had been there a couple of months, he said, "Perry, why don't you come up and run marketing and sales for us and help me get it established?" So I went. We quickly decided that, since LSI Canada would be the smallest market, we had to destroy the competition to succeed. In such a small ASIC market, you've got to own it.

Our major Canadian customers were BNR and Northern Telecom, our market base for starting the company. To make it difficult for our competitors to participate in the market, we had to bring our design capability to the customer. Our competitors would have to spend more than they could afford in the limited Canadian market.

We put design centers in Ottawa, near BNR, and then in Montreal, Toronto, Vancouver, and Calgary, and started calling customers. At the time, we would have considered ourselves lucky to get even ten Canadian customers, but within a year, we were talking with more than 150 Canadian firms.

Our take-no-prisoners strategy gave LSI Canada a higher market share–probably 75 percent or more of the non-captive ASIC market–than we have anywhere else in the world.

We took the Canadian company public in April 1987. Like the U.S. IPO, we hit the window just perfectly; a week later, there would have been less of an opportunity. We raised $37 million which, by Canadian standards, was a successful public

offering and meant we could maintain a strong balance sheet. From day one we've been self-financed, fulfilling a major goal to make the Canadian company able to stand on its own.

18 Manufacturing in Europe

Sales in Europe for LSI were climbing nicely, but European customers were pressuring LSI to manufacture there. The challenge was to set up an indigenous manufacturing capability without depleting most of the U.S. company's capital.

BOB BLAIR

By 1986 we had our European design centers ticking, revenues were doing well, and the European company was profitable. We were feeling pretty good about ourselves, and we thought now was the time to think about manufacturing in Europe. We wanted to build a major manufacturing plant somewhere in Europe capable of diffusion, assembly, and test. The question was: where? The easy decision was to do it in the United Kingdom because of language and proximity to our European headquarters. LSI management and the Board favored the United Kingdom, but I wanted to pursue other alternatives, particularly Germany. Since interest rates at that time were half what they were in the United Kingdom, Germany was a bargain for borrowing money, and my European experience told me that Germany is considered "more European" than the United Kingdom.

Our due diligence in government grants showed that Italy and France were not attractive because the incentives were just not there. Finally the choice came down to the United Kingdom and Germany. The U.K. government made a mess of the grant with us; they wanted us to build a plant in Wales, but the politics of the grant were unacceptable. It was a Catch-22 proposal. They could give us grants if we were failing, but not if we were a success.

In contrast, we got good reception in what was then West Germany. The State of Lower Saxony encouraged us to build our factory in Braunschweig. It was a watertight deal with no loopholes and included capital, R&D, and employee grants. Being so close to the East German border made us a little nervous, but Germany is Germany and had many advantages. Braunschweig was only half an hour away from the Hanover Airport and had excellent telecommunications with the rest of Europe. So the European Board approved the venture, and we began construction of the building. Our plant in Braunschweig produces high pin-count plastic packages and is the center of excellence for plastic packaging for LSI worldwide.

As we were building the Braunschweig facility, another opportunity presented itself. A wafer-manufacturing plant in the United Kingdom that was built but not yet put into production, was offered to LSI Europe at low cost, and we agreed to do a deal with its owner, STC. It gave us a fully facilitized wafer fab that only required manufacturing equipment. We revised our European manufacturing plan to do chip manufacturing in the U.K. and assembly and test in Germany, and we put future wafer fab expansion in Germany on hold.

Besides the low cost, there were other advantages in doing the U.K. deal. STC is a major player in the U.K. telecommunications market, and we wanted to have a relationship with them. They also offered to encourage other major companies to invest in the operation but, ultimately, we couldn't enlist other U.K. companies in the venture. While we successfully produced ICs in the United Kingdom for six years, in 1990 we concluded that the U.K. diffusion manufacturing facility was a "boutique" that may have been appropriate for the mid-eighties but was not competitive in the nineties against the Japanese. So in early 1991, we decided to phase out volume manufacturing operations in the U.K. facility. In retrospect, manufacturing

semiconductors in Europe in the nineties didn't make sense because the volumes were too low and the economics just didn't pan out.

In spite of closing our wafer fab, our European company is, overall, very successful. In 1990, LSI Logic Europe was the fastest-growing semiconductor company in Europe, the leader in CMOS gate arrays. Our competitors are primarily the same Japanese companies that we face worldwide. Our only real American competitor in Europe is VLSI and only two European companies continue to be competitors on their home turf.

In my opinion, only two European semiconductor companies are worth a damn–SGS Thompson and Siemens AG. Both companies are extremely competent technically, but even these giants are feeling the pressure from the Japanese manufacturing machine. They've had to cut back massively because they had too many plants. Siemens semiconductor operations reportedly is losing about $300 million a year. SGS apparently is also losing money. SGS and Thompson merged less than two years ago; after the merger, they had 16 plants in Europe–clearly too many.

In the seventies and early eighties, "Made in Europe" was such a cachet that the customer was willing to pay a premium for semiconductors manufactured there. Now, in the nineties, computer revenue has gone to hell. SUN Microsystems redefined the model of a successful computer company by regularly doubling price performance every year. While "Made in Europe" is prestigious, keeps jobs, and is good for the social environment, the reality is that if a chip costs 20 to 30 percent more than if made somewhere else, it can't compete.

WILF CORRIGAN

We always believed we had to have European manufacturing, and certainly from our projections of the European ASIC

market, it made sense at the time. We had the opportunity to move into Germany with very attractive financial incentives from the West German government, but then STC offered us a wafer fab plant in England. We looked at our European sales forecasts and decided to build both plants.

What we did was typical of the times, but in retrospect, the early eighties was a disastrous period for the United States. Because of the strong dollar and the disparity of interest rates between Europe and the United States, America began moving manufacturing overseas to Japan and Europe. European labor seemed reasonable when measured at those 1986 exchange rates. Conditions are totally different today, and we closed down the plant in the U.K. in 1991.

The cost of a critically sized wafer fab has increased dramatically. To maintain competitive prices, we would have had to extensively expand and modernize the European plant. Unfortunately, the computer market in Europe is shrinking, and today the European market isn't big enough to support a semiconductor plant of critical mass. That means either you have a non-cost competitive sub-critical size plant or you build a plant of critical mass and export. Japan has cultural reasons for wanting their ICs made in Japan, so the European fab would have to export to the U.S.

Unfortunately, Europe is a very high-cost manufacturing region because of the number of working days per year, the number of legislated vacations, the welfare state–all these issues raise costs quite dramatically. And the secondary infrastructure needed to support semiconductor manufacturing equipment is inferior to that of Japan and the United States.

As it turned out, our long-range plan to go public there influenced us to over-invest in Europe. We wanted to do in Europe what we did in the U.S., namely, commit to factories, build the business, go public, and use the equity to finance more factories.

LSI Europe has been a mixed bag. It's been very successful in marketing, but not financially. That's changed now that we have consolidated our chip manufacturing in Japan and the United States and closed down the U.K. plant. Our Braunschweig plant in central Germany has been very effective as an assembly and test center. We're by far the largest European ASIC supplier; I think LSI Logic Europe would rank about number six in the world as an ASIC supplier.

By most standards, we've done well in Europe: more than $100 million in 1991. The problem is, we haven't done it as well as we'd hoped; we thought we would do more than three times that by now.

19 LSI-Kawasaki Joint Venture

LSI had hired K.K. Yawata, set up its Japanese company, got local capital, established design centers, and booked some business. LSI needed some Japanese manufacturing, but didn't want to dilute the local marketing thrust by spending all the money on manufacturing. LSI decided to find a Japanese partner with deep pockets.

WILF CORRIGAN

We began discussion with Kawasaki Steel. They wanted to move into the electronics business and felt that semiconductors were crucial to their future. Silicon is a metal. Kawasaki knew how to make steel foundries, so they probably figured that a "silicon foundry" must be similar.

After a lot of negotiation, we had Kawasaki as a partner. They felt comfortable with the big investment required, but the only way we could justify such a large fab and operate it economically would be to use it as a source for LSI Logic worldwide. The economics looked pretty good because the cost of Japanese capital was very low, the interest rate was low, and a lot of this would be straight equity capital with the costs measured in yen. Kawasaki felt optimistic that they could build their own semiconductor business and would have strong demand for the facility as well.

MICK BOHN

The negotiations with the Kawasaki people were prolonged and difficult. I remember explaining the outline of the negotiations

to Wilf, and he doubted that such a deal could be done. In the end, Kawasaki agreed to invest 90 percent of the capital, and LSI would put in 10 percent and our technology. We would own 55 percent and Kawasaki 45 percent of the joint venture known as Nihon Semiconductor, Inc. Subsequently, I had the Kawasaki people out to my North Dakota ranch and took them pheasant hunting, for them a first. In Japan, it's illegal to own a gun, much less hunt. They shot pheasants (which we had for dinner), rode horses, and really enjoyed the cowboy experience they had seen only in the movies.

K. K. YAWATA

It was a novel idea for LSI to form an alliance with Kawasaki Steel, which at the time was not an electronics company. They wanted to broaden their capability into the high tech area; I think all five major Japanese steel companies were trying to diversify, but no one found a way for them to get started. Our idea for forming a joint venture manufacturing ASICs was interesting, and they agreed to accept us as a strategic partner. Kawasaki would invest $100 million and LSI Logic would provide the manufacturing and process technology in addition to $10 million in long-term investment.

In June 1987 the factory was completed, equipment was installed, and we were ready to start manufacturing. The differences between Japanese and American culture created communication problems among the process engineers, but that was soon remedied. By the end of 1987, we were producing a higher yield on larger wafers than the LSI fab in the United States. Because manufacturing was brought up so smoothly and LSI Logic was able to use 100 percent of the factory's capacity, I believe it gave Kawasaki confidence. Much to our surprise, they decided to build their own semiconductor factory in Utsunomiya.

WILF CORRIGAN

Neither LSI Logic K.K. or Nihon Semiconductor has a single American employee. They are both run as Japanese companies and are gaining market share in the Japanese market. The trade agreement has helped, but the biggest factors in our success are that we manufacture there and provide Japanese-style service. Our major competitors are the Japanese, and we're one of the few American-based companies competing with them on their own turf.

I think the competitive position of America and Japan in our industry is misunderstood. American technology is good, but America has lost, and must win back, its ability to manufacture well. That's very much a strength of the Japanese. Take the example of the GM-Toyota joint venture known as NUMMI, located in Fremont, California, one of the least automated and most efficient of the GM plants. The Japanese improved the operation by good management, superior training, and motivating workers instead of simply adding more robots.

Culture homogeneity and group allegiance give the Japanese big advantages in manufacturing. The Japanese have the highest literacy rate in the world, and everyone working in one of their factories goes through the same educational system.

Having a single language is another advantage for the Japanese. In a U.S. wafer fab, you might find seven or eight languages spoken, and 20 or 30 different dialects representing a dozen different cultures. We pay a price for cultural diversity. It enriches us and sparks new ideas, but at the cost of communication.

In contrast to America, which emphasizes individual achievement, the Japanese are used to working as a group and are extraordinarily dedicated to their company as a kind of super group. Japan is a hierarchical society where, starting with the Emperor, there's a kind of national pecking order and everybody seems to know where they fit.

COMPUTER-AIDED ENGINEERING

20 LSI Design Tools

In 1981, when LSI Logic started, there were only a few commercially available computer-aided design tools. What was available was not very good or well integrated. It was clear that LSI would have to develop most of its own CAD tools.

JIM KOFORD

When Rob Walker came to Ed Jones and me in 1980 and invited us to join what was to become LSI Logic, I was immediately concerned about the difficulties such a fledgling company would face. I had been through one unsuccessful start-up, and I was well aware that we had to move quickly before our money ran out. We needed an industrial-grade design environment, and Ed and I both knew of the enormous sums of money that others had put into developing such capability– often with limited success. It was certain we were going to be criticized as unrealistic unless we could prove our critics wrong by performing.

Ed and I had one great advantage over other would-be CAD developers–this was our second time around. Rob and Wilf had enough confidence in us (although we came to test such confidence) to let us map our own computer-aided design (CAD) plan. We were allowed to specify the strategy, the computing resources, and the implementation. All we had to do was meet the goal we had all set for ourselves: a viable CAD environment for the design of gate arrays within a year.

In March 1981, Ed and I set out to develop the start-up CAD plan. This we did keeping in mind that the heart and soul

of any good integrated circuit (IC) CAD environment was and still is properly integrating logical design services (simulation, analysis, and test) with physical design services (layout, checking, and packaging). To be successful, you must always incorporate a firm understanding of sound circuit engineering principles. Failure to do this is often the fatal flaw of commercial CAD tools.

Since there was no way that the two of us could write, debug, and document all the needed software in 12 months, we had to go "third party" for core tools for circuit simulation, logic simulation, and layout. Ed and I would then concentrate on writing the all-important interfacing and delay-prediction software to turn the selected collection of core tools into an ASIC design system. Meanwhile, Rob Walker's engineering group would develop the models and data structures describing our ASIC products.

Besides selecting core tools, we needed to select hardware and software environments for our CAD system. Our years at Fairchild had convinced us that the industrial-grade IC CAD system we were planning, with its heavy emphasis on simulation and automated layout, needed lots of MIPS of computing power, memory, and disc storage. After evaluating many different hardware options, we concluded in 1981 that the only hardware environment with the power, reliability, and price/performance we required was an IBM mainframe. We could get six or more MIPS of computing power, the system disc and tape I/O were unmatched, and we could lease an "IBM-mainframe clone" such as Amdahl at a competitive price.

Of course, we had worked with non-IBM systems (Digital, in particular), and in some ways preferred those machines, but they didn't have the computing power we needed. Furthermore, the lack of clones of other vendors' hardware placed Digital and others at a price/performance disadvantage, much as today's

IBM PC clones. Conventional wisdom said we shouldn't be using IBM hardware for CAD because of its older operating systems, available languages, and lack of modern graphic interfaces. But we were certain that we could obtain modern graphics terminals and interface them to the IBM hardware. Although we did this very successfully for our internal graphics requirements, it was not practical to do so for most of our customers. With our alphanumeric interfaces, we appeared somewhat backward in the early eighties because we focused on more fundamental needs. Even though we didn't show as well as our competitors, our circuits worked–something the competition couldn't necessarily guarantee.

After selecting the computing environment, we set out to find graphics hardware. We chose the products of Megatek, then a leading graphics terminal vendor. We selected the TEGAS logic simulator and the Silvar-Lisco layout package. By the fall of 1981, Ed and I were busy integrating all of this into an ASIC design automation system that Rob called LDS-I, for LSI Design System I. The TEGAS Logic simulator turned out to be a fortunate choice. Primitive by today's standards, it was reasonably reliable and effective for the designs of the period. The people at TEGAS were competent and we worked well together. I started building interface programs incorporating TEGAS into LDS-I. A documented, working simulator let us start the all-important activity of modeling for our macrocells in the summer of 1981.

We were not so lucky with the Silvar-Lisco package. Their software did not match our array approach, and it soon became clear that we would have to develop our own layout software. On his own, Ed Jones managed to develop a workable graphics layout environment by early 1982. It was a remarkable achievement when you consider how many engineers it normally takes to develop an industrial-grade IC layout capability.

In the fall of 1982, Comsat introduced a new version of the TEGAS simulator called TEXSIM which had back annotation, an important feature now standard on any competent IC design simulator. The performance of an IC depends on its layout. Back-annotation allows actual interconnection delays to be used in simulation. This allowed us to use our own proprietary programs to calculate delays of circuit elements and feed them to the simulator for very accurate simulation. Bishop Brock of TEGAS and I worked around the clock to produce a new version of LDS that supported back-annotation. Other significant enhancements that Ed Jones and I developed led to our second-generation CAD system which Rob Walker called LDS-II–LDS that works!

As we moved through late 1982, Ed and I began to plan for a *real* LSI CAD system. By mid-year, it had become clear that graphics and software portability would become major issues. While we were very proud of our accomplishments to date, we knew they had been somewhat expedient. The company was now launched and it looked as if it would be successful. We needed to turn our attention to our CAD strategy for the rest of the decade.

Although we ran well on IBM compatible mainframes, we did not offer solutions to the VAX, Apollo, or Prime user. Furthermore, all modern computing environments were increasing the support of graphics, and a burgeoning CAE workstation industry was providing our users with graphic schematic interfaces. The alphanumeric IBM interfaces we were using looked even more primitive when compared to the newer graphics interfaces, and the old mainframe FORTRAN language was woefully obsolete.

In formulating our follow-on software strategy, we needed to write our own CAD system, tailored to the needs of LSI Logic. It had to be portable because we knew that low-cost,

high-performance computing hardware was coming from many vendors. Since the development time on a major CAD system was two years or more, we had to "intersect with reality" in 1984 or 1985. Finally, we wanted to utilize the latest developments in graphics for ASIC CAD.

In the fall of 1982, two extremely fortunate events occurred. Several of our former colleagues contacted us; they had been following LSI Logic and wanted to join. Soon Bill Jensen, Dennis Yamamoto, and Ron Ryan were on board. We were also able to hire Doug Boyle, a brilliant young Ph.D. from Stanford, who was well-versed in the latest software tools.

After studying available languages such as PASCAL, MAINSAIL, and C, we chose C, the language associated with UNIX. We felt that this language was ideally suited to the efficient implementation of complex CAD algorithms, the most portable language, and the most likely to emerge as the next major standard. I think that on all three of these points we were right on. The choice of C as LSI Logic's standard CAD implementation language has been a happy success.

Thus, we started on our all new LSI CAD system. Bill Jensen and Doug Boyle did the front-end logic system including a major new logic simulator, LSIM. Ed Jones, Dennis Yamamoto, and an outstanding new graduate from the University of Texas, Ching Yen-Ho, did the layout system. Patricia Rohrs was building a professional documentation group. Doug had also hired a brilliant core-logic development group: Paul Filseth, Will Naylor, and Tom Wilworth. This team produced our mid-eighties CAD system, LDS-III. The new system was entirely written in C, and ran under IBM VM/CMS, VAX/VMS, and UNIX. Ultimately, it included many landmark innovations for us, such as LSI's behavioral simulation, logical expression synthesis, multi-chip simulation, R-C tree analysis, automatic routing and object alignment in

schematic entry, automatic schematic generation from netlists, test synthesis, floor planning, compact-array layout, regional chip layout, and regular-structure compilation.

The story of LDS-III cannot be told without mention of Silicon Graphics and SUN Microsystems. By 1983, we were beginning to reach the limits of the Megatek graphics hardware that we were using for chip layout. Ed Jones was asked by one of the Valley venture capitalists to have a look at a start-up that was planning a revolutionary graphics terminal based on a special "Geometry Engine" graphics processing chip. Ed visited the new company and returned convinced that "if they execute what they plan, our current graphics terminals will be history."

That type of enthusiasm is uncharacteristic from conservative Ed Jones, so Wilf Corrigan and I arranged to have lunch with Jim Clark, the Stanford professor behind the Silicon Graphics design. Afterwards, Wilf's comment to me was, "You must have really liked what you heard, Jim; I couldn't get a word in edgewise."

Ed and I really did like what we heard. LSI took delivery on the Silicon Graphics IRIS System, Serial Number 002, and Silicon Graphics became the graphics terminal of choice at LSI Logic for the next several years. With the new Silicon Graphics terminals attached to the mainframe, we had a very powerful layout environment. We were able to use the IBM mainframes through the use of a proprietary C compiler developed by a consultant named Mark Brown. However, we knew that the future of ASIC CAD lay not in mainframes, but in high-performance graphic workstations.

Doug Boyle had become the primary advocate of UNIX at LSI Logic. In 1983, Doug convinced us that we should look at the plans and products of a new UNIX workstation company, SUN Microsystems. Doug and I went over to SUN and I came away very impressed. SUN had a great design team from

Stanford that had designed the Stanford University Network Workstation, and they also had Bill Joy, the father of Berkeley UNIX.

They were committed to the then revolutionary concept of Open Systems, and that dovetailed perfectly with our need to have portable software that could be used with the products of many hardware vendors. We bought SUN workstation No. 450 (it still works!) and Doug Boyle and Bill Jensen began to use it as a UNIX development platform. The SUN workstations quickly became an industry standard CAD platform, and SUN and LSI Logic still enjoy a close technical relationship.

By the end of 1988, we realized that even LDS-III would need to be replaced. While LDS-III was probably regarded as *the* premier gate array design system in the world, it too was showing signs of obsolescence. A thriving third-party tool industry was developing even better human interfaces, and an increasingly sophisticated customer base was clamoring for better control of the design process.

For the past three years, Ed, Dennis Yamamoto, and Ching Yen-Ho had been developing LSI Logic's third-generation CAD system, the Concurrent Modular Design Environment, or C-MDE. This system takes the integration of logic design with layout design to new heights. It makes rich use of concurrent multi-tasking, shared memory and data structures, and an advanced graphics interface. It runs under UNIX, using accepted graphics standards, and will be available on a number of hardware platforms. It will handle standard cells as well as gate arrays, and it should have a capacity of a million transistors or more. We have finally shaken the legacy of the older mainframe-influenced user interfaces, and C-MDE will reward us for the hundreds of man-years that have gone into it.

The future for Electronic Design Automation is very bright. Within the lifetime of LSI Logic, we have seen hardware technology move from $1 million mainframes with alphanumeric

interfaces to $1000 workstations with modern graphics interfaces and 10 to 20 times the memory capacity and processing power of a 1981 mainframe. Ever more sophisticated software techniques allow us to produce and maintain software that allows relatively small teams of engineers to design, debug, and bring to production multimillion gate systems in months, not years. Large design spaces can be explored effectively so that the resulting designs implement products of high quality and capability at low cost.

Much of the drudgery of older design methodologies has been eliminated, as engineers design at higher and higher levels of abstraction, using such tools as the VHDL language and logic synthesis. Better high-end methodologies minimize the use of traditional CAD techniques such as gate-level simulation and test vector preparation. An aggressive EDA software tools industry is constantly developing new products to simplify and render more efficient the design process.

Two U.S. commercial companies have been primarily responsible for bringing the ASIC semiconductor business to its current status: LSI Logic and VLSI Technology, Inc. While we started with completely different approaches, we have arrived at similar end-points. We at LSI have always acknowledged the achievements of VLSI people like Doug Fairbairn and Jim Rowson, and we have respected them as worthy competitors. As they explore advanced new approaches to the problems of automated electronic design in their start-up, Redwood Design Automation, we wish them luck, and we hope we can use their products in the future.

The United States possesses a very strong engineering community. Rob Walker, Ed Jones, and I are very proud to be members of that community and we hope we can do our part to preserve it and strengthen it.

21 CAE WARS

Through the seventies, the primary computer-aided engineering (CAE) tools were no more than electronic drafting boards. The principal suppliers were Calma, Applicon and Computervision. While better than cutting rubylith with Exacto knives, they did not support schematic capture, logic simulation, automatic layout or test generation–the tools required to automate IC designs. The vision of a set of integrated tools for IC design installed on a powerful graphic workstation was compelling.

A number of start-ups were funded in the early eighties to provide process-independent CAE systems. The three most prominent were Daisy Systems, Mentor Graphics, and Valid Logic, known in the trade as "the DMV." Debuting at the 1982 Design Automation Conference in Albuquerque, New Mexico with a dramatic show worthy of Hollywood, they took the engineering community by storm. Their merchandising was terrific, the demos compelling, and they sold the promise of reducing system design from years to months. Virtually every major electronics supplier evaluated "the DMV" with the goal of standardizing on one CAE vendor's suite of tools for their corporation.

ROB WALKER

At LSI Logic, we watched the CAE wars with great interest. At the time, we had no schematic entry and our logic simulator was accurate and powerful but required a big IBM or Amdahl mainframe. We evaluated the DMV and selected Mentor Graphics for several reasons. As opposed to Daisy and Valid's custom hardware, Mentor used a standard workstation from Apollo, which promised us rapid price performance improvements.

Second, their logic simulator, the holy grail of the LSI Logic design philosophy, was the most accurate of the three. Finally, while Daisy was the CAE market leader, their president, Aria Finegold, saw LSI Logic as a competitor and wouldn't negotiate a reasonable deal with us.

LSI did an OEM deal with Mentor, developed the logic symbols and models, and started calling on customers. In our naivete, we figured the ASIC customers would make their decision on rational grounds. Wrong! We didn't realize that the bloody internal battles that system companies had gone through to select their corporate CAE system had left the staff extremely polarized.

About 70 percent had chosen Daisy or Valid or someone else, and the thought of buying or leasing a Mentor system from LSI Logic to design their ASICs was totally unacceptable. Very quickly, it became apparent that we had to support all three major CAE vendors and, in fact, even some smaller suppliers such as Viewlogic and IKOS. This turned into a huge drain on R&D resources, and we never were able to do a really first-class job.

It was during this period that Myke Connell, then in charge of our Mentor Graphics support, made a killing on the stock market. He was impressed with the Mentor Graphics system, and the company had just gone public. He phoned his broker and instructed him to buy Mentor stock. The stock quickly doubled in value and he sold out, reaping a tidy profit. It was

only then that he discovered his broker had bought stock in Mentor, the condom company, not Mentor Graphics, the CAE company.

By the mid-eighties, our customers were discovering that the DMV had a number of problems. To make them user-friendly, their logic simulators were so simplified that an ASIC design would work in simulation and fail in silicon. Obviously, you want it the other way around, where any design that operates correctly in simulation is sure to work in silicon. Second, the CAE suppliers, particularly Daisy, over-promised. Their software was full of bugs, was late, and changed quickly. Third, the early workstations were little more than personal computers and lacked the computing power for the large simulations necessary to ensure working silicon. In practice, mainframes had to be used for the full chip simulations.

Finally, the DMV had a real conceptual problem regarding ASIC libraries. They honestly believed that their customers should buy a workstation and the application software from them and receive, from the ASIC vendor, logic models and performance libraries at no cost. We at LSI Logic had invested tens of millions in these libraries and considered them our "family jewels," worth more in our eyes than the DMV hardware and software combined. In fact, we were the first to encode our complex functions so they couldn't be reverse-engineered into another ASIC vendor's library.

This fundamental difference of perspective was always a source of friction between LSI Logic, CAE vendors, and customers, although in recent years the value of the intellectual property of silicon "foundries" has become more accepted. In 1992, after going bankrupt, Daisy, now called Dasix, is a division of Intergraph. Valid Logic has merged into Cadence with the Valid name fading into history. Mentor Graphics, the DMV survivor, now shares with Cadence the lion's share of the CAE market.

22 Silicon Compilers

In the early eighties, the academic world led by Carver Mead at Caltech was espousing a new approach to integrated circuit design known as silicon compilation. The idea was to automate as much of the design as possible, so that system engineers could design ASICs without involving themselves in a lot of circuit and layout issues. Then the ASIC would be manufactured by a silicon foundry, a semiconductor manufacturing facility which would sell silicon by the pound, much like a steel foundry. Certainly compilers were a laudable goal and quite successful at VLSI and LSI Logic, particularly for regular structures such as memories, multipliers, state machines and data paths. George Gilder in his book, Microcosm, *published in 1989, saw a bright future for process-independent compilers:*

> ***The masters of the silicon compilers were young geeks scarcely out of school. The experts on the old system resented these newcomers ... They tried to twist the new technology to match the old expertise ... Impelled by the logic of the microcosm, the silicon compiler represents a further shift of the sphere ... It is a weapon of creative destruction that will ultimately force these established firms to change the way they run their business. From***

the establishment point of view the compiler would lead to 'bad designs'–But Mead ... [was] saying that in the usual sense, for most chips, quality didn't matter ... The compiler paradigm would ultimately prevail regardless of the views of the established firms. It would move the power to design chips–and to determine which chips get designed–away from the semiconductor firms and toward the systems companies. Most portentously, the silicon compiler would move industrial power away from commodity chip designers and toward systems architects.

Gilder foresaw a $500 million market for process independent compiler tools in the early nineties.

Based on the rosy projections for compilers, three process-independent silicon compiler start-ups were founded: Silicon Compilers, Inc., Silicon Design Labs, and Seattle Silicon Technology. Despite Gilder's "quality doesn't matter", "shift of the sphere" and other most portentous predictions, and hundreds of millions invested by venture capitalists, all of the start-ups failed. What went wrong? Defects in the process-independent silicon compiler companies eventually proved fatal.

CARVER MEAD

Gordon Moore introduced me to Silicon Valley. I was a young assistant professor still wet behind the ears, when one day Gordon Moore walked into my office at Caltech and said, "Would you like some transistors?" At that time, silicon transistors

were very expensive, something like $25 each. He pulled out a manila envelope that must have had several pounds of transistors inside. I had never seen so many. Gordon plopped them down on my desk. "Here," he said, "we like having students using our stuff." And then he invited me to come up and consult with him at Fairchild. In 1961, I started coming up to Silicon Valley approximately once a week, which I've been doing ever since.

So I was around when the integrated circuit was just starting to find its way into real products. I would snoop around in all the neat work that was going on at Fairchild, find research topics, and take them back to Caltech. I saw the Micromosaic project, and although at the time I was in device physics, I was fascinated by the potential of design automation.

In 1968, I was invited to give a talk at the Device Research Council at the Lake of the Ozarks. They wanted me to discuss what happened as transistors got smaller and we put more components on a chip. Preparing for the paper, I started working on some simple scaling calculations. I then realized that if you scaled things right, everything got better. I stood up and gave a paper about how, with scaling, the power went down, the speed increased, and the number of devices went up.

By 1969, it was very clear to me that someday we were going to be able to put millions of transistors on a chip. That meant that I was working on the wrong end of the problem. If we really could make a million transistor devices, the key issue wasn't about wafer fab or semiconductor device physics, it was about, "How the hell do you design something with a million working parts?"

At that time, nobody had a clue about how to design chips of that complexity. I needed to figure out (a) What kind of thing do you do with million-transistor ICs? and (b) How would you ever get the design right? So I taught myself logic design since I had never done any. To understand how computers

work I started teaching a freshman course in computers because that's a good way to learn. Then I thought, even if I had a program that would wire together a bunch of logic gates, there are two problems. First, just getting a logic diagram with a million working parts is a big deal, and I'm not sure I could ever get it right. Second, that approach would preclude me from using a lot of the things that made MOS technology so attractive such as precharge, pull downs, and everything one could do if they know the environment in which the circuit lives. I needed to find a way of using primitives larger than just gates. My first priorities were data logic and control logic because everything can be divided into something that handles the data and something that does the control.

Coming up with the array-logic concept was really exciting because I could do any function in what I call "finite sequential logic." I didn't realize that this principle had been well known for years and it was called finite-state machines. The books I read talked about automata, but I didn't know what the hell automata was, and it wasn't described in physical terms.

I took my ideas to Noyce and Moore who had just started Intel in a little plant in Mountain View. I became an Intel consultant with badge No. 5. I showed them, with my approach, how you could do both commonatorial logic and sequential circuits, but at the time Intel was a tiny company focused on memories. All they could commit to was running some test parts.

At Caltech, I built an artwork language that allowed you to enter input feedback terms, minterms, and outputs and would automatically generate the layout. Then you could give it a truth-table for the microcode, and it would produce the tooling for an IC. This was the first silicon compiler; it was great fun.

ROB WALKER

The most fundamental lack of understanding of the academicians was the concept of an arms-length vendor-independent

silicon foundry. The idea was that you could implement your design using generic design rules, get bids from the silicon foundries, then simply optimize or re-compile the design for a specific technology process and foundry. Unfortunately, it just doesn't work that way. The topological design rules do not embody all the knowledge needed to produce production quality integrated circuits. For example, reliability issues such as latch-up, electromigration, ground-bounce, and electrostatic discharge protection were not sufficiently addressed by the simplistic design rules of merchant process-independent silicon compilers.

In the real world, compiler tools must be qualified by generating test structures which are then fabbed, tested, characterized and put on life test. Based on this feedback, the compiler eventually is qualified for a specific process and fab. Naturally, this is an expensive proposition; to do it with five or ten silicon suppliers is prohibitive.

A second flaw lies in the business model. Suppose you run a silicon foundry and a customer wants you to fab 5000 ASICs a year, with a complexity of 10,000 gates. You have no idea of the functionality or reliability of the design. If you're lucky, you might be able to get $20 for each of these parts, or a total of $100K for the deal. Are you willing to risk your reputation as a quality silicon supplier or face a major lawsuit for $100,000 worth of business?

Fatal flaw number three is that the merchant market process-independent compilers don't work on gate arrays, the principal ASIC design vehicle. Naturally, LSI Logic compilers work on both array and cell-based ASICs.

Flaw number four is production test. You don't have a usable ASIC unless there is a tester program created to extensively test the production parts to ensure that no manufacturing problems have rendered that chip flawed. These tests require tens of thousands, sometimes hundreds of thousands of individual patterns. What productivity is gained in generating a design

in a few weeks if it requires several months to write the test program? In contrast to process independent compilers, those from LSI Logic and other silicon suppliers compile the production test, and often special test structures for each function.

Finally, there are many circuits you don't want to compile. Suppose you need a 32-bit SPARC microprocessor with an ethernet controller. Since both are available as a megacells, you just select and interconnect them; design time takes just a few days.

CARVER MEAD

I think the reason that the commercial silicon compiler firms failed was a conflict of cultures. The system people didn't want to give up their gate level logic because that's what they knew, and the semiconductor people didn't want to give up their process-optimized design. That left us with a small group of customers willing to go out on a limb.

I was a member of the board of Silicon Compilers, Inc., whose compiler tool was called Genesil. I had enormous battles with Phil Kaufman, then President of Silicon Compilers Inc., over unbundling Genesil. Phil was from Intel and he had Andy Grove's "gotcha" mentality–what I call the negative value-added approach: If you can make an Intel chip that does not work with a Motorola chip, then you've won.

That philosophy had rubbed off on Kaufman–he didn't want anyone to be able to take a part of Genesil and mate it to other people's tools. I think Silicon Compilers would have been a roaring commercial success if we could've sold pieces individually.

Another problem was our arms-length relationship with semiconductor manufacturers. I remember a discussion I had with Phil when we first moved into the Hamilton office in San Jose. "Phil," I said, "we've got to start fabbing our stuff so we

can build a relationship with the semiconductor vendors. This will develop confidence that our designs will work in production as promised." To Phil, once you had a simulation, that was all you needed. He believed you just pushed a button and got silicon.

JIM ROWSEN

Silicon Compilers Inc. oversold and underdelivered. They always pissed me off by taking business away from VLSI, then failing. Behind the scenes, they had a "tape out" group that took one or two months to hand-massage a Genesil design so it might have a chance of working. After VLSI developed a data path compiler, we beat the shit out of them.

ROB WALKER

A personal story will illustrate the dichotomy between the silicon compiler's promise and delivery. In the mid-eighties, Seattle Silicon, a process-independent silicon compiler start-up, was going through one of their periodic financing rounds. They contacted us at LSI Logic, and Wilf and I went to Seattle for the day to hear their pitch. They had more than 70 employees and were burning more than $1 million a month. Their top management was on hand for their demo to us. The first menu of their compiler software that they showed on the screen listed a variety of silicon foundries and processes. You were to pick one for compilation into that technology. No Japanese, no mainline semiconductor suppliers, not even VLSI were listed. All the choices were small, failing and inept semiconductor manufacturers–not a good sign.

As the Seattle Silicon demo continued, a large static RAM was compiled. You would just type in the organization and required performance and out popped an embedded RAM. Later, after lunch, they asked me if they could show me more. I asked to meet their circuit designers. They only had three or

four out of their 70-plus employees–another bad sign. They rounded up two young men and we went into a conference room. I asked about their backgrounds. One guy was right out of college; the second had spent two years at Boeing. "Where did you get the design for the RAM bits, decoders and sense-amps?" I asked.

"We got them from a textbook," they answered.

"Well, have you ever had any built, characterized, and life-tested any?" I asked. The answer was no.

Now a RAM design is difficult. Even with experienced designers and a good fab, you must build some typical organizations and test the hell out of them to ensure they will work when embedded in an ASIC. I told Wilf on the flight back, "I can't believe these people will ever be successful with their approach."

In 1991, Seattle Silicon's compiler-tools group were sold to Oki for cents on the dollar.

Another sad silicon compiler story is that of Evans and Sutherland Computer Division. Dave Evans was a true convert of the Carver Mead silicon-compiler philosophy, and had been instrumental in VLSI's funding. Evans and Sutherland chose Silicon Compiler Inc.'s Genesil software tools for their ES1 supercomputer project with Minneapolis-based VTC Corporation as the silicon foundry. Their computer required only six ASIC types, and we at LSI pleaded with them to buy some insurance and let us back up their Genesil-designed ASICs. They wouldn't hear of it–only the Genesil/VTC scheme made sense to them.

Subsequently, VTC was unable to fabricate the ASICs and the designs were eventually redone in the Hewlett-Packard 1-micron process, entailing more time-to-market delay. Finally, they had the supercomputer almost working but they needed to redesign two of the six ASICs. After a three-year development and a $30 million investment without a fully working product, their top management pulled the plug. Stunned employees

learned of the shutdown of the Supercomputer Division on the floor of the Supercomputing 1990 Conference in Reno.

At LSI Logic and other major ASIC suppliers, compilers are alive and well. When used with extensive libraries of megacells and logic synthesis tools, they materially reduce design time. The merchant-market silicon compiler companies failed because they lacked the concept of a close coupling to a few, high-quality semiconductor foundries, and they had an overly simplistic view of semiconductor manufacturing.

ASIC WINNERS

23 Cadence Gets it Right

Cadence Design Systems is a very successful supplier of design automation for electronic systems and ASICs. They have been a thorn in the side of LSI Logic for years, primarily because they have provided competitors, in particular the Japanese, with workable design automation technology. For some reason, the Japanese have always been weak in computer software, especially design automation. This weakness gave the American-based LSI Logic and VLSI a tremendous advantage over the Japanese in the early eighties.

Throughout that period, there were a variety of design automation companies: Daisy, Mentor, Valid, Calma, Silicon Compilers Inc., and Seattle Silicon, to name a few. Fortunately for LSI Logic and VLSI, they never appreciated the very close relationship between silicon manufacturing and design tools required for producing high-performance, reliable, high-yield circuits. Their arms-length, almost adversarial "silicon foundry" attitude never worked well.

Then came Cadence. With experienced IC designers and a strong Japanese presence, they became the ASIC design tool supplier to Japan Inc. Through acquisitions and mergers, Cadence has acquired ECAD, Gateway, Calma, and Valid Logic in addition to a number of smaller ECAD companies.

JOE COSTELLO

While I was at Cal working on a Ph.D. in physics, I did some part-time work for National Semiconductor. One day I got an intriguing call from National. They were doing something in speech synthesis and recognition, which had always been a pet interest of mine. I was still working as a physicist but I thought the semiconductor business would be fun to be around, so I ended up going to National and took over a speech-synthesis project.

That's where I got to know Jim Solomon, who was facing big productivity problems in IC design and looking for improvements. He kept trying to cram all kinds of design automation down our throats. He'd bring in university software from Berkeley but it was always a disaster–we found it easier to design by hand.

He proposed that National should form a group to develop some heavy-duty design automation. Charlie Spork had the presence of mind to say, "You know, it won't work here at National–wrong culture. It may sound good right now. We'll get excited about it, but the first time there is any kind of glitch or downturn, the program will get cut. You ought to set up an independent company and get other semiconductor companies interested."

Jim ended up getting National, Harris, and GE as industrial sponsors to invest in the company and then got some venture guys to back him up. Jim left National in mid-1982 to found SDA.

We all thought he was crazy. We gave him a going-away party, and after a few beers, someone asked, "What's with Jim? He's a bright guy. National loved him. He could have had any job in the company." We at National thought that design automation guys were the ultimate pits, so we laughed and joked when he took off, and we never understood his vision.

My group got cut and I left National a year later. Jim called me and asked "How's it going, Joe?" he said.

"Well not so good," I said, "I'm leaving National."

"Well great," he said, "why don't you come interview at SDA?"

I went on the interview only because he's a good friend, but I didn't want to work in design automation (DA). I thought anyone involved in DA was a flake by definition.

The people at SDA surprised me. They described their vision with a lot of energy and excitement. Later I met some of the Board, but I still didn't know what my job would be. When I asked Jim, he said, "We've got a lot of work to do here; I'll call you tomorrow with an offer."

He called me the next day. "How about handling customer service, documentation, and training?" he said.

Jim came from the perspective that IC designers need a complete, integrated solution. From the Berkeley guys, he had gotten this notion of frameworks to build an underlying foundation into which you could plug all the different tools. He thought we should focus on software and forget the hardware because the Digitals, Apollos, and IBMs of the world would automatically take care of it. Based on those fundamentals, he started SDA.

I was amused at one conversation I had with Jim early on. "What kind of funding did you get?" I asked.

"Wow, it's unbelievable, Joe," he said. I was thinking $2 to 3 million bucks; I figured even that was more than we'd ever need. They have given us over $10 million dollars. I don't know what we're ever going to do with so much money. There's no way we could ever use it."

$22 million later, we finally had a profitable company; we had underscoped the problem slightly.

Initially, our story didn't play well to customers. Most didn't

appreciate our framework concept. They were looking for a hot logic simulator or a better circuit simulator or verifier. "Just give me a tool," they would say. Then there were the 'silicon compiler' people who promised to revolutionize the world. Next to them, our story was pretty boring. We finally decided to take a stand and to get very clear and crisp about what we felt was fundamentally right about our approach. We promised to supply a complete, integrated yet open approach to IC design automation, and we started to get a few believers. We still had the original industrial investors GE, Harris, National, and L.M. Erickson who led us to some other key accounts–a big piece of business at Hughes which in turn led to Toshiba and SUN Microsystems.

We had an IC layout editor written by some ex-Berkeley and AT&T people who believed they had built a better mousetrap. I honestly don't know if it was better or not, but it was different, and no one was buying it. We kept getting feedback from our customers. "You've got to have Calma commands if you want to sell into this business. You're on a workstation that's neat, you have better architecture, you have some wizzy features like automatic place and route, and an interactive design-rule checker. That's great, but your layout editor doesn't look like anything anybody understands. You need some Calma commands." Our engineers said, "We're not going to do Calma, it's old, stupid, and the wrong way to do it."

We finally got a new guy in and in just a couple of months he wrote a Calma knockoff. It may have been coincidence, but we went from selling six or ten copies to ninety in three months, which really got that portion of the business cooking.

But we still didn't have all parts of the puzzle; we had a little of this and a little of that but not a complete product set. Nevertheless, we were moving up with revenue at a $15-$20 million yearly run-rate.

Then we tried to go public. We were actually scheduled to go out in October 1987. Then the stock market crashed and our IPO got squelched. Fortunately, we had enough cash in the bank to carry us.

It was a crazy time in the CAE industry; people were going under and there was lots of talk about mergers and acquisitions. A couple of guys came to us and suggested we would be smart to merge with ECAD. That would really change the ASIC marketplace. Len LeBlanc, our CFO, gave me a call in the middle of the night when I was in Japan and said, "Maybe it makes sense to merge ECAD and SDA." At that time, ECAD and SDA were vicious competitors. ECAD was increasingly moving into layout, which we considered our turf, and we were already bumping into each other in verification.

Each of us went at the problem differently. In physical design verification, they were batch, we were interactive. In automatic place and route, they were doing block place and route, but we were doing standard cells. In layout, they were taking a very high and symbolic approach; we were using a Calma-like polygon editor.

Although we were complementary, we were out there crunching on each other, and so I thought, why merge with them? We hate each other. Len advised me to think about it.

I came back from Japan just before Christmas 1987. We figured a merger with ECAD had merit, but concluded that they would never go for it. They were just too vicious, and they would see it as a sign of weakness on our part, so I felt we shouldn't even talk to them about a merger. Lo and behold, the week after Christmas, Alex Brown calls and says, "You know, our client ECAD thinks the best thing they could do would be to do a merger with you."

After talking to them, we realized that a merger would give the combined companies critical mass in R&D, sales, and

marketing along with a size that was much more credible to our larger customers who were asking for more technology than either of us could provide in a short period time. Fortunately, we had the framework architecture to fold together our technologies and put them into an integrated package. That's what led us to decide to merge the companies. Although everybody was very skeptical about it at the beginning, it worked great, and our sales really took off.

Naming the new company was a challenge. If we retained the name SDA or ECAD for the merged company, the other group would feel like losers. Instead, we came up with a new name, Cadence, for the merged company.

We saw that being a dominant supplier to ASIC foundries was critical, but in the long term, we needed to serve the systems marketplace since, increasingly, ASICs were a fundamental portion of systems design. We had already determined that staying solely in the ASIC arena could be a dead end where we would get niched into being just a chip player.

We talked to our systems customers and they kept saying, "This piece that you're doing for us in ASIC is neat, but our job is the system. We need tools for everything." Then we evaluated the market. Did we have a chance? Could we take on big companies like Daisy, Mentor, and Valid in the systems business?

Two things convinced us that we could: we saw that our decisions about the framework base and supplying software versus hardware were basically correct, and that the other guys were on the wrong track. Knowing how hard it was for us to get our framework off the ground, we figured it would take them two or three years to replicate the capability. It's always good when the other guys have to go through a major revolution to compete.

Second, we saw a glimmering of "top-down" design. We thought a fundamental change in design methodology could be

really helpful. Systems were using more ASICs. Multi-chip modules were coming, and for sure, board level design would change radically. Surface-mount devices, finer line widths, and lots of analysis would be needed, which meant that board design methodology would become far more complex. We gambled that it was the time to enter the system tools market. We had to take our shot right away because if we waited, the opportunity surely would be lost.

In the beginning, some of our guys lobbied for us to develop most of the new tools ourselves, and I said, "Wait a second–even if you developed the world's greatest logic simulator right now, you're not going to compete with Verilog from Gateway." So we started merger talks with Gateway and Synopsis. We really wanted Synopsis synthesis, but we just couldn't make that happen, so we ended up developing our own synthesis product. I had predicted that Gateway probably wouldn't want to merge but that Synopsis probably would. Luckily I was wrong, and we merged Gateway into Cadence.

PRABHU GOEL

After stints at IBM and Wang, I decided to start my own CAE company, which eventually became Gateway. At Wang, I had spent a month evaluating the HiLo logic simulator.

In June 1983, Phil Moorby, the developer of HiLo, called me from England. "Prabhu," he said. "Why don't you hire me and I'll come to the States and write a new logic simulator for Gateway? After my experience developing HiLo, I think I can really improve on it." I hired Phil in March 1984 and in a year he developed Verilog, the standard by which other logic simulators are now measured.

When we started selling Verilog, it had the capability to span the complexity range from the highest level of abstraction then available all the way down to gates and even transistors. Since we had no ASIC libraries initially, we sold to sophisticated

integrated circuit and systems companies like Motorola and SUN Microsystems. Our selling point was the notion of the advantages of a more abstract design methodology. We wrote models for complex elements such as an Intel 8085 microprocessor and allied microperipherals. We could demonstrate an entire computer system simulated at a high level, actually accepting C code, compiling it, dumping it into RAM, and executing instructions.

The people at Motorola, particularly Dr. Vassillios Gerousis, really helped us get into the ASIC simulation business. Motorola Austin was using Verilog in the design of microprocessors like the 68030. The Motorola ASIC group heard of their success and came to Gateway with a proposition. They would tell us what features we had to enhance to make Verilog suitable for ASICs and, if it worked out, they would become our customer. No formal commitments were made, but we worked together and they introduced us to ASIC requirements such as pin-to-pin delays, back annotation of interconnection delays, and glitch detection. Motorola did a massive technology transfer, and we did everything they asked us. As a result, they adopted Verilog as their "golden" simulator–they would commit to implement ASICs that worked the way Verilog said they would work.

We decided that ASIC was the future of Gateway. We formed a business group to approach all the ASIC suppliers and do what was necessary to make Verilog their standard. Aside from LSI Logic and VLSI, who had their own simulators, most ASIC suppliers were using Daisy, Mentor, or Valid CAE tools known as "the DMV," and they were realizing that these generic simulators were being force fed into their ASIC needs as opposed to our approach of implementing the real needs of ASIC technology directly.

We were able to get ASIC suppliers such as VTMC, National Semiconductor, and Motorola to make Verilog their

golden ASIC simulator. Then we marketed the hell out of the concept that ASIC customers should use Verilog, not "the DMV," in order to minimize correlation problems with their ASIC suppliers.

A second factor in our success was that Verilog could do top-down design with abstract modeling. Customers like SUN Microsystems and Silicon Graphics reported reducing the time-to-market of their workstations by as much as six months.

Another big boost came from Synopsis who came to us in 1987 wanting to license the Verilog language for their logic synthesis product. We were very receptive to the deal as Trimeter, the other major logic synthesis toolmaker, had selected our competitor, the VHDL language.

Very quickly, Synopsis began going to the system companies championing the Verilog cause and demonstrating its productivity advances along with their synthesis. High-level Design Language (HDL) and logic synthesis was the one-two punch that blew away the other simulators; none of our competitors created a complete design environment around their simulator.

In 1989, I was planning on taking Gateway public. We were close to $20 million yearly revenue with a nice 20-percent-plus profit margin. Joe Costello and I had discussions about combining Cadence and Gateway; from their standpoint, we had exactly what they didn't have. From my standpoint, I was coming to see that Gateway lacked a sufficiently large sales and marketing organization. When I looked into the costs of upgrading marketing and sales to do the job adequately, it was clear we would have to acquire companies or merge with someone to obtain a critical mass.

As we were preparing to go public, Joe Costello called and since we had developed a good rapport, I shared our plans with him. "You know," he said, "getting two public companies

together is a lot more painful than getting a private and a public company together. Let me see if I can put together a merger proposal."

When Joe came back with a serious proposal, I talked to my Board and gave them my perspective. "Look," I said, "we can continue to make money in this business for awhile, but as you look beyond the horizon, we will just be a niche player." So we concluded that we could do a lot better for the sales and marketing of Verilog, for the people in the company, and ultimately for the shareholders if we put the companies together.

JOE COSTELLO

Before the Gateway merger, we had done a deal with Tangent for gate array and standard cell layout tools. After Gateway, we added a printed circuit board capability from ASI. Most recently, we merged with Valid Logic Systems to create a CAE juggernaut with 2200 employees and worldwide revenue of $392 million in 1991.

Harvard Business Review summaries say about 70 percent of all mergers fail, so we came up with a set of criteria for both companies considering a merger that I think has withstood the test of time. The first criterion is whether the merger is strategic from a market, distribution, and technology point of view and will work long-term. A merger acquisition only makes sense if it fills a strategic hole in your plan. Too many companies do acquisitions because they look cheap, or the timing seems right, or it's only a defense move instead of serving their true priorities.

Our second criterion is having minimum overlap between the companies. Zero overlap is almost impossible–our rule is no more than 20 percent. In a merger, you spend 90 percent of your management time dealing with overlap. Overlap is where you find all the friction and all the grinding of the R&D guys takes place. You're dealing with egos, customers, sales force, marketing guys who are jockeying for whose product will win. If

you have too much overlap, you're screwed. People will get angry and frustrated and bail out, and you'll end up with nothing.

Our third criterion is having a good cultural match between the merging companies. That may sound overly trendy, but it's really important. Just like people, companies have personalities. If the management team is pretty closely aligned, it usually filters down into the company in style and approach. In one of our Cadence mergers where the cultures were very different, it has been very difficult to get people to work as a team.

Finally, both companies must agree that the merger is good for the shareholders. It's got to add to earnings per share, and except for ASI, our other mergers have done that. Because ASI wasn't a healthy company, it gave us a hit to earnings per share for awhile.

Looking at failed mergers, I haven't found one that didn't break one or more of those rules. The Daisy/Cadnetics merger, for example, violated all of them, and they went bankrupt.

How to keep key people whose stock is now worth quite a bit relates to the first criterion that both parties must believe the merger is strategic. Let me take Gateway as a prime example. Prabhu Goel was well compensated for his 50 percent ownership of Gateway in the merger, yet I never worried about whether he was committed to Cadence because he had a vision. He wanted to see it through and he stayed on three years to do just that. He's like Rob Walker and Jim Koford in that he wanted to make his vision come true, and Cadence gave him a vehicle to make it happen.

I remember when we sat in his house and talked about what was possible, where we were going, and how we could do it better together. I knew we had a bond right there. When you have a mission, it doesn't matter how much money you have. If you connect on that wave length, you're in good shape because people are committed to something more important than dollars.

Paul Huang and his ECAD team had the same commitment. Paul and some of his guys eventually left to start another company, but only after they helped us make the transition successful. Paul is not the guy to stick around in a large company, but he spent two and a half years making the merger effective. That's the key, I think, sharing that strategic vision where you concern yourself with what can be accomplished together.

Cadence needed to penetrate the Japanese market, which we realized when we looked at the data on IC design and saw that most of it is done in Japan. Naively, we thought, "Let's get over there and start selling our products," and started asking around about how to do it.

We signed an agreement with a Japanese distributor called TEL, seemingly a good idea since they were a big distributor and had done other design automation deals. But after a year and a half, we had sold only $400,000 in Japan, about half in hardware. Now Japan is the number one market for IC design automation in the world. Needless to say, our sales weren't going well.

In the period from 1984 to 1985, the president of TEL was Larry Yoshida. When the semiconductor capital equipment business went to hell, Larry got fired because he was aggressively expanding their business, causing the company to lose money for the first time. But, after a few months, some of his customers asked him to start another distribution company. "We love you," they said. "Do it."

We were introduced to Larry through one of our customers. "Wait a second," we told him, "this is Japan with its traditions. You just got fired from a respected company and you want to start up a distributorship, and we're supposed to dump TEL and go with you? That's crazy."

So we gave him a test. "Larry," we said, "get us in to see six of the top ten semiconductor general managers two weeks from now." And he did. We thought, "This guy is for real, we'll do it.

We'll go with him. It certainly couldn't be worse than the existing situation."

Larry Yoshida and our partnership with Toshiba got things cooking for us in Japan. Larry did a fabulous job recruiting a team of people, and putting in a lot of focus. Cadence also spent a lot of energy in Japan. Even when we were small, we had full-time teams there servicing customers and talking to them, trying to understand them. That dedication got us off the ground in Japan. In fact, before we merged with ECAD, over 60 percent of our sales were in Japan; now it's about a third of Cadence sales overall.

We kept worrying that the Japanese were going to develop their own software. When are we going to get nailed like everybody else in the other U.S. industries? After a little while, when we understood the dynamics, we were less concerned. Japanese companies have in-house design automation teams. It can be argued that the design automation people are not as strong as those in the United States, but some of them are pretty good. The in-house groups have some decent tools and they were doing some successful designs so why didn't they ever invent a Japanese version of Cadence?

I believe there are two reasons. One is that the Japanese CAE people are in big companies and there is no way they were going to sell to their competitors and there is no way their competitors were going to buy them anyway, so they could never make a market. There would have to be an independent design automation company and there's not much push to do a Japanese start-up. Unless the Japanese get more entrepreneurial, the odds of them starting something that would be effective in design automation are fairly low.

I've always said that LSI and VLSI have the best tool sets for ASIC because they are totally integrated into their technologies. In my experience, most productive design automation teams must work hand and glove with the IC designers. It's one of

those instances where the sum of the parts is greater because the energy starts flowing back and forth, the design automation guys get excited when they actually see something work, and because they get more productive and course-corrected more quickly. We made an edict recently that we would start no projects without a semiconductor or systems partner. Synergy is key to good IC design automation.

24 Altera Takes the Programmable Approach

Up to this point, the discussion on Application Specific Integrated Circuits has been on "mask programmable" types, i.e., those manufactured specifically for one customer. Another type, "programmable logic" circuits are manufactured identically in volume, then personalized in the field by the customer for a specific application.

Programmable devices are marketed using a variety of acronyms, PLD (Programmable Logic Device) and FPGA (Field Programmable Gate Array) being the most common.

Altera Corporation of San Jose is a leader in the field, and Bob Hartman is a founder. Bob had worked with Rob Walker at Fairchild in the seventies, and in 1980, they co-authored an article on gate arrays. In the same year, Bob Hartman started a small gate array consulting company called Source III, and his experiences there led him to innovate a unique approach to ASICs.

BOB HARTMAN

At Source III, we consulted for people who were trying to design gate arrays. At the time, most layouts were manually routed and checked, so a lot of silicon expertise was required–more than most customers had. Between 1980 and 1983, we did about 50 designs employing a variety of technologies:

CMOS, ECL, ISL and TTL. We also consulted for both gate array suppliers and their customers on other issues such as choice of technology, vendor selection, and production testing. We decided sometime in 1982 that we could capitalize on our knowledge of the business by writing and selling a comprehensive survey of the emerging gate array business. That book, *Gate Arrays: Implementing LSI Technology*, contained an extensive list of suppliers, how they did designs, the emerging technologies, and lots of product detail.

One reason we wrote the book was to protect ourselves because, as consultants, we got called upon to do a lot of free consulting. We believed that rather than answering the same questions over and over and getting nothing for our hard-earned knowledge, we could sell a book that contained the answers. To an extent, we achieved our aims, but the financial payoff was not very great. One of the best results of our effort was that it forced us to document what we knew and fill in many gaps in our knowledge.

When we finished the book, we reflected on what we had learned. There were about 65 companies in the gate array business in 1982. The number of suppliers was growing daily because the barriers to entry seemed low. We believed that there were far too many ASIC suppliers, and that some consolidation was inevitable. At the same time, we were looking for a way to get out of consulting and into a product business. We concluded that what the world really needed was not another mask-programmable ASIC but rather a programmable solution for customers with small production requirements and no silicon expertise. Such a product could be manufactured in high volume and supported by electronic distributors.

Ours was a market-driven response. We knew in general what the product should be before we had any specific idea of the exact architecture or technology. Then we had to choose the silicon technology, programming and device architecture. We

picked CMOS technology for its low power and high density. For a programmable approach, we looked at EPROM, EEPROM, SRAM and fuse link. EPROM was the densest, most accessible, most reliable technology with the most manufacturing history. We also created some architectural concepts. These decisions were the genesis of Altera.

We then wrote a business plan and started making presentations with the usual Silicon Valley approach of raising money and starting a business. We got Jim Hazle involved as a consultant, and he helped put us in contact with legal counsel and investors. We got the initial seed funding of $1.3 million from Alpha Partners. Alpha's business was to take potentially good ideas at a very early stage and get them to the point where they could be turned into real companies. Finally, we had to begin assembling a team.

We believed we saw a way to do programmable ASICs that was a fundamentally good idea with no inherent technology risks. We thought our business plan was sound, but the potential investors came back with, "Well, if this is such hot stuff, how come nobody's done it? The technology's there, the architecture is fairly straightforward, so why haven't other people jumped on it?" We thought the answer was that the people who knew about the capability of the technology didn't know the market and vice-versa, but we honestly didn't know for sure. The initial funding was to prove that the technology worked and that there was a market for programmable ASICs. Between June 1983 and March 1984, we hired people, lined up a semiconductor foundry, defined the architecture, did the design and the layouts, and produced our first circuits.

One of our several charters during that time was to produce a device that would show feasibility. Rather than do a test chip, we produced the EP300, a superset of the 20-pin PAL family which we thought would be a salable product.

Second, we had to find a CEO, but we didn't feel we had one among the original group of founders. We talked to more than 20 people before we finally decided that Rodney Smith was the right guy. He turned out to be a great choice. Recruiting your own boss is not all that unusual in Silicon Valley, Mike Markkula of Apple being a noteworthy example. We also had to find someone to head marketing since we didn't have substantial marketing knowledge ourselves, so we did an extensive search. We also had to build the engineering infrastructure and raise more money. In our first nine months, we raised our next round of financing, roughly $6 million.

The charter for Altera had two elements. First, we needed to develop large-scale programmable devices. The 20-pin EP300 we originally designed was intended more to show feasibility than to be a final product. Since our long-range goal was to develop much larger devices, the big task early on was to architect higher density parts, which incidentally, is still our biggest challenge. We've made some rather dramatic strides. Our latest products are 30 times more complex than our first products.

Second, we needed to develop software tools that would enable customers to use our devices. Since the kind of business we were entering could be likened to either microprocessors or gate arrays, our two business models were microprocessors from Intel and ASIC from LSI Logic. It was pretty clear that the winners in the ASIC marketplace were the ones with the best support tools and Intel's development tools accounted for much of their success in microprocessors. You can't sell high-density programmable logic ICs without software tools any more than you can sell gate arrays or microprocessors without them. We were convinced from the outset that software was key to our business–at least as important as silicon for Altera's success.

Our computer platform decision was also tough. In mid-1983, the IBM PC was only two years old, and the clone

manufacturers were just starting. At the same time, there was a choice of workstations such as Mentor on Apollo, Daisy, and Valid. Our dilemma was that a workstation would cost our customers probably $80,000 to $90,000, but a personal computer platform, although a lot less powerful, was much cheaper. We decided to target the PC first and then, if we had to, port tools to the workstations. Fortunately, since PC computing power has grown as fast as our needs, our choice was a good one. The low cost of PCs ($2,500 to $3,000) has allowed our customers to do their programming right on their desktop.

Today we have more than 5,000 customers or customer locations, and more than 12,000 development system sites worldwide. Altera ICs are in almost everything that uses digital logic. Our biggest markets are communications, industrial controls, military, office equipment, printers, and PC peripherals. Historically, we don't do well in the high-speed data path, workstation, and mainframe markets. We currently offer parts with densities to 10,000 gates, and we have upcoming designs that will take us to 20,000 gates.

We've also done a lot in package development. EPROM technology needs ultraviolet light for erasure–once one pattern is erased, another can be programmed. This requirement forced us to develop some unique windowed packages, particularly high-lead count quad flat packs. We anticipate going as high as 288 pins when we reach 20,000 gates. While we offer all of our ICs in windowed packages, most of what we sell is low-cost plastic "one-time programmable" devices which don't require windows. These parts are blank (i.e., erased) when the customer gets them, and then they're programmed one time to fit a particular application. We typically offer a ceramic windowed part for development when there are many changes, and a low-cost, non-erasable plastic counterpart for higher-volume production. Over time, most of the volume goes to plastic.

Contrasting our business with that of LSI Logic, our complexity tends to be from 500 to 10,000 gates moving toward 20,000 gates. I believe LSI Logic's complexity is an order of magnitude higher. We also differ in how we sell to the marketplace. While LSI sells primarily through a direct sales force, Altera stocks and sells through distribution, just like any other IC standard product; people can buy a few or tens of thousands. We're ideal for the developmental environment and low-to-moderate production volumes. But if an ASIC customer is going to require 10,000 or more identical units a year, mask programmable ASIC such as those from LSI, are probably a better choice economically. Luckily for Altera, and something that we realized early on, many systems never reach that volume.

Programmable logic offers two big advantages: time-to-market and low risk. Our customers have told us of many designs that were completed in a few days, while design errors can be corrected and functional changes done in a few hours. Here we have a distinct edge over gate arrays. The development tool environment also is different in that we're still using low-cost PC computers, while gate array tools almost entirely run on much more expensive workstations.

Naturally, we've had our setbacks. We originally planned to go public in 1987. In fact, Rodney Smith, our CEO, was supposed to go to New York to talk to analysts and kick off the road show. Then came the great market crash of October 1987. The Dow dropped 500 points and our IPO was put on the shelf. We were fortunate that we didn't have a pressing need for cash, and six months later, in March 1988, we were able to go out. The IPO provided an opportunity to stop (if just for a moment) and enjoy the success that we had all worked for. We took the entire company out to the Red Lion Inn for a celebration. We were extremely fortunate to get to that point, and we knew it.

While our IPO marks the end of this narrative, by no means is it the end of the Altera story. Since 1988, we have increased sales by a factor of three, added many employees and developed a lot of new products. Early in 1992, we introduced our first EEPROM device. I expect Altera to be around for a long time.

25 VLSI– Virtually LSI

VLSI got its funding in December 1980 just a month before LSI Logic. At that time, the only thing the two companies had in common was that they were both in the ASIC business. In all other respects, they were poles apart. The engineering people at VLSI were young and disciples of Carver Mead, the Caltech VLSI guru, while those at LSI Logic were middle-aged and had all been at Fairchild.

LSI was committed to gate arrays and believed that the Mead-Conway full-custom methodology was flawed. VLSI used Digital Equipment VAX minicomputers to run the Mainsail language; LSI used the cheapest available IBM compatible mainframes and Fortran (later C). LSI's computer tools were alphanumeric and ugly, but accurate. VLSI used beautiful graphics and pop-up menus, but their logic simulator and test methodology were weak. The two were bitter enemies not only in business, but in ASIC methodology as well.

In 1992, LSI and VLSI are still competitors. In fact, VLSI is now LSI Logic's only major U.S. ASIC competitor, but their design methodologies are now quite similar. Both companies' tools run on powerful workstations with superior graphics. Both offer gate arrays and cell-based ASICs. Both have diversified

into Application Specific Standard Products (also known as chip-sets). In fact, the joke is that VLSI stands for "Virtually LSI."

ROB WALKER

Over the years of competition, mutual respect has grown between the technical teams of LSI Logic and VLSI. Doug Fairbairn and Jim Rowson, the principle architects of VLSI's technical direction, have left VLSI and founded Redwood Design Automation. Thanks, Doug and Jim, for your friendship over the years and particularly for leaving VLSI, our biggest U.S. competitor.

Jack Balletto, one of VLSI's founders, has also left the company and is now a venture capitalist. I've known Jack since the early seventies when we were both being battered at Fairchild MOS.

JACK BALLETTO

In June of 1973, I joined Bob Schreiner as a founder of Synertek. His investor strategy was to find a group of systems companies that wanted a semiconductor position without spending a lot of money. It took about six months before convincing Victor, General Automation, and ATC to fund the company at $250,000 each for a total of $750,000. About a year later, we got Bulova; they paid twice the price and put in another $500,000. Over the first twelve months, we received a grand total of $1.25 million and didn't get another nickel from an investor for two years.

One of the first things we brought to market was the last-mask ROM for quick-turn manufacturing. We went from zero market share to something over 50 percent in the ROM market in six months when Atari, our biggest customer, took off in the game business. We dominated Atari's ROM business, and Synertek grew quickly. This was the first time that customers actually paid extra for quick turnaround (QTAT).

We wanted to build a second fab, but couldn't afford the $5 million price tag. Schreiner told us that we couldn't take the company public; we were then doing about $20 million per year in sales, with 15 percent pre-tax profit. Atari and Apple were our two biggest customers and we also had Olivetti and Digital. If you looked at the balance sheet and the customers, you would say that for a $1.25 million investment, we had done an unbelievably good job.

But even with this success, we couldn't raise a nickel from the venture capitalists and we couldn't go public at that time. We had to sell or eventually die. So we sold the whole company to Honeywell for $22 million. Looking back, it doesn't seem like much money for all the work that went into it, because in fact, the company did some pretty good things. The 6500 microprocessor, which we received on a cross-license deal with MOS Technology, was in huge volume for Atari and Apple and was the principal engine for both the video game and personal computing industries.

So I went from badge number three and a founder of a company which was taking on all the big guys like Intel and Fairchild, to Honeywell employee number 649,312. Honeywell management was incredibly screwed up. We had meetings with the top five people at Honeywell who assured us they understood how small companies grow and would leave us on our own. That was fine until we had the first budget meeting. Our Synertek engineering guys had designed all their chips on Tymeshare since we never could afford in-house design automation. With the Honeywell money, we said, great, now we can get our own computer. Our engineering guys picked Prime as the most cost effective in-house computer solution and submitted a purchase order.

Honeywell management then made it clear that Prime Computer was run by a bunch of Honeywell turncoats so we couldn't buy a Prime machine. Digital and IBM were also

politically incorrect. In fact, the only choice given us was to buy a Honeywell machine. The appropriate Honeywell computer would not be available for another year, so our engineers had to design a 16-bit microprocessor on Tymeshare. I knew then that this merger was a mistake, and six months later I left to form VLSI.

Dan Floyd, Gunnar Wetlesen, and I got together in July 1979 to write the business plan for VLSI Technology. Initially, we thought: "Let's make a semiconductor company that is only a silicon foundry to manufacture designs done by customers; maybe there's enough business so that all we would need is a perfect, quick turnaround silicon manufacturing plant." We started talking to some corporate investors and figured that we'd finance it the same way we did Synertek.

At the Dataquest Conference in fall 1979, Digital Equipment presented a paper that said that 25 percent or more of their semiconductor requirements in the eighties would be custom or semi-custom. It looked like the guy stole his forecast from our business plan. This legitimatized our business concept so I figured it wouldn't take too long to get our $10 million. Wrong! Turns out $10 million was a lot of money back in those days–and still is. But we had seen Synertek miss the chance to be one of the major players because of hand-to-mouth funding, and we didn't want that to happen again.

Almost all our potential customers agreed that down the road they would like to do their own chips. The question was, who was going to teach them? They had huge staffs of systems people but nobody who knew chip design. We met with Carver Mead, who was teaching classes on VLSI design at Caltech.

"Carver," I said, "I have a little problem with this foundry concept. Nobody's around to teach these hundreds of thousands of systems people who want to design their own chips. Where's

the software and the teachers? This fab is going to start costing half a million to a million dollars a month just sitting there." So around December 1979 we defined a second operation in the company, a group who would teach customers how to do their own design.

From talking with Carver and others, we heard of Doug Fairbairn, a bright young guy who was right on top of the VLSI movement. Doug worked for Lynn Conway at Xerox Palo Alto Research Center (PARC), and in January 1980, we convinced him to join us as the fourth founder. It took us from July 1979 to December 1980–18 months–to get our funding.

DOUG FAIRBAIRN

In 1976, Ivan Sutherland was working with Carver Mead as Chairman of the Computer Sciences Department at Caltech. Bert Sutherland, Ivan's brother, was the head of the Systems Science Lab in Xerox PARC where I worked. Through the Sutherland brothers, we got Carver Mead to come to Xerox in the spring of 1976 and give a three-day course on how to design VLSI.

Lynn Conway and I attended the course and were very impressed with Carver's ideas. The most exciting aspect of what he had to say was the power and efficiency to be gained by melding the worlds of integrated circuits and systems. We and the other attendees were all from a systems design background and immediately realized the benefits of integrating our ideas in silicon rather than on printed circuit boards using traditional TTL logic.

A real strength of Xerox PARC was that it wasn't a pure research organization. Rather, it was filled with bright people wanting to implement their new innovative ideas, not write papers about them. In line with this philosophy, we felt that in order to really understand this new design medium of integrated

circuits, we actually had to design them. But, in order to do that, we needed appropriate design tools. Again, Carver Mead had the solution.

Jim Rowson was a senior at Caltech doing work in system design and IC design tools and was the ideal person to solve our design tool problems. Jim came to PARC for the summer of 1976, and in that short period he developed an interactive layout editor called ICARUS to run on the Alto personal workstation. This was the first such CAD tool, and it ran on the first personal computer. It offered very fast response, exceptional ease of use, and was widely used at PARC, and eventually the rest of Xerox as well. It featured multiple windows, pop-up menus, and mouse-driven drawing ease.

We used ICARUS to design a number of chips, and we built our confidence and understanding of the process with each step. We became enthusiastic about spreading our message that there were tremendous benefits to be gained by bringing the system designers close to the silicon, allowing them to implement what they had only dreamed about.

The Mead-Conway technology was one technique for bridging the gap. As our understanding of the technology and the sophistication of the tools evolved, it became clear that there were other ways to approach the problems. Unfortunately, Carver Mead's essential vision and contribution was sometimes lost because of the problems with its implementation.

To spread their message and methodology further, Carver Mead and Lynn Conway collaborated on a book, *Introduction to VLSI Design*, a college-level text that taught the "Mead-Conway" design methodology. First published in 1979, this text was quickly adopted by hundreds of universities around the world.

Jim Rowson and I decided to create and publish a magazine that brought together system architecture, design tools, circuit

design, and IC fabrication, the multiple disciplines which affected the IC design process. We called the magazine *Lambda* after the essential unit of measure in the Mead-Conway methodology. I wanted to publish this magazine while still working for Xerox, so I decided I'd better first get permission. I approached Bert Sutherland and the people at Xerox PARC to see if they were interested and would help us. "Bert," I said, "we want to publish a magazine on chip design on a quarterly basis."

"What are you going to do after the first year?" he asked.

"Well," I said, "if it's a raging success or a dismal failure, I'll know what to do. And if it's somewhere in between, I'll have to figure that out."

"Okay," he said, "but you better clear it with the lawyers." And I did. They were surprisingly accommodating.

Then someone recommended that we talk to the Xerox people in Pasadena. Xerox was trying to adapt the Alto computer to electronic publishing. Alto was the original desktop-publishing computer, and the Pasadena operation actually had an Alto connected to a typesetting machine. You could enter your text on the Alto with all its nice type fonts and then ship it off to the typeset machine and get back publication quality print.

We went down to Xerox Pasadena and asked, "How would you like to help us do this magazine as an experiment in electronic publishing?" They agreed. Jim Rowson and I were working on the project together and when it came to writing the articles, we started calling our friends.

The first issue had four articles: one on semiconductor fabrication, one on circuit design, one on system architecture suitable for IC implementation, and a fourth article that featured a new semiconductor start-up company whose business plan called for them to focus on IC fabrication for independent design teams. I thought this was a perfect fit for the magazine

because this new company was just what all these new designers needed–a place to get their chips made. Most of the existing semiconductor companies only fabricated chips of their own design, and were not set up for dealing with outsiders. The new company was VLSI Technology, Inc.

I interviewed the three VLSI founders in their Los Gatos office in November, 1979. They had just gotten together as a team in July and had published their business plan in September. They were beginning to show it around, but were getting a lot of questions about where the new designs were going to come from and who was going to train their customers. They began shopping around for someone to join the founding team who could do the training and develop the software tools. They selected me.

I wrote an article on VLSI and it appeared in the first issue, which hit the streets January 15, 1980. But by this time, I had already left Xerox to join VLSI Technology. Since VLSI was still in a fundraising mode, I had quite a bit of time to work on the magazine. I was always careful to keep my job and the magazine editorially and financially separate. I didn't want to seem to favor VLSI in any of the writing or ad placements for fear of losing potential writers, readers, or advertisers.

Lambda was the first magazine devoted solely to ASICs, and Xerox's contribution in helping to design and print it created quite a controversy. The first issue was put together in December 1979 while I was still with Xerox. A woman at Xerox Pasadena Division was experienced in printing and book design and worked over Christmas laying out the magazine. She also helped us choose the printer and paper stock. Jim Rowson's brother-in-law, a graphic designer, did the design. We decided to get the best quality paper to give it the "heft" and feel of a first-rate publication since the magazine was only 32 pages long and had no advertising. We printed 2,000 copies. Printing was

expensive but as part of their experiment to prove the desktop-publishing concept, Xerox Pasadena picked up the tab.

Since I had gotten permission from my boss and my boss' boss and the Xerox legal department to publish *Lambda* magazine, I figured I was in the clear. When the time came to leave, I went around handing out copies of the magazine, showing people what we had done and how Xerox Electro-Optical Systems in Pasadena had helped us.

On my exit interview, Frank Squires, the personnel guy who had been a good friend the eight years I was there, was outraged. He thought I was a devious, evil character who had screwed Xerox and misled them. I was really upset by Frank's attitude; I thought we were friends. Then I went to see Bob Spimrad, the head of Xerox PARC to tell him what I had done. He was relatively new, and I didn't know him well. He said he wasn't happy with the situation, but he couldn't do much since I had cleared it with the lawyers. So finally I went to his boss, George Pake, who had been the head of the operation for most of the time I was there. He looked at the magazine and said, "Hey, this is great. You just went off and did this? I think it's wonderful." I felt relieved.

I was amazed that even though I left, the people in Xerox Pasadena were willing to perform the same tasks for the second issue, including paying for the printing, and we were able to print another issue in May. When that was done, again with no advertising, they said they couldn't help anymore.

Meanwhile, I was working for VLSI primarily to help raise money. The plan was done and VLSI needed only 25 percent of my time, so I continued to work on the magazine. I hired my secretary from Xerox and moved her into the den of my house, which became the magazine's first publishing office.

It was time to make some decisions. Xerox was no longer going to pay for printing and I couldn't keep spending my own money–I needed to get some advertising.

One day, I got a call from a guy at Harris who wanted to place an ad in the next issue. I really didn't know if there was going to be a next issue, so I promised to call him back. I started calculating and figured that if I could sell 15 pages of ads for $1,000 a page, I could pay for the next issue. I called the Harris guy back and confidently told him the next issue was going to come out in November. He signed on and I spent the next six weeks on the phone calling all my friends to get ads for the next issue. When all was said and done, I reached my ad target of 15 pages.

Jim Rowson and I continued to work together and we were also teaching a VLSI design course at Hewlett-Packard. HP had approached us to put together a course on IC design for their engineers. I was assisted by Bob Mathews and John Newkirk, professors who were teaching the Mead-Conway methodology to SRO classes at Stanford. HP paid us for the 10-week course, videotaped it for in-house use at HP, and gave us the sales rights to the course and videos. Meanwhile, the magazine took on a life of its own and I hired Jerry Werner as editor.

VLSI finally broke its funding bottleneck in December 1980. We hooked up with Dave Evans of Evans & Sutherland Computer Corporation. Dave had been looking for a company like ours for quite some time. He felt that getting VLSI design technology into his company was critical to their future success. So he embraced the concept and agreed to invest $3 million in VLSI. Bill Hambrecht of Hambrecht and Quist was on his Board of Directors and had high respect for Dave's technical expertise; he went in for $1 million. Since H&Q was the leading high-tech venture capital company of the day, we were immediately oversubscribed. We had gone from a year or two of famine to feast, and had more money pledged than we could use. In the end, Evans and Sutherland invested $3 million and five different ventures came in for another $7 million. On

December 12, 1980, we put $10 million in the bank and launched the company.

JIM ROWSON

I got my Ph.D. from Caltech in June 1980 and hung around as a postdoc waiting for a job opportunity; I didn't want to go to an established company. And then Doug Fairbairn recruited me to VLSI to lead the software team. At that point, we were very much students of Carver Mead's hands-on layout and that's what we taught our customers.

DOUG FAIRBAIRN

Since you couldn't be an engineering company without a VAX, the first thing we had to do was buy a Digital VAX computer which was then at the peak of its popularity. You could have $500,000 worth of computer sitting on your doorstep and Digital had the audacity to make you wait 13 weeks to install it! Obviously we had to get our VAX up quickly, and as part of our purchase arrangement, Digital flew in an installation team. Pam, the Digital salesperson, bought them beer to keep them happy during the late night installation. A few years later, we arranged another deal and she became my wife.

Next we had to pick a programming language. I didn't ever want to be in the position of Calma, running on Data General hardware and not being able to move. We needed portability. We looked at PASCAL, Mainsail, C, and Lisp. At the time, C was a university curiosity and Mainsail had a lot of features that made us believe we could build large software systems very reliably. PASCAL was so different from one machine to another that it wasn't portable. Fortran was never an option. We selected Mainsail and it turned out to be an outstanding decision.

We started teaching month-long courses on VLSI design October 1, 1981. During the four weeks, the students actually

designed a chip that we later fabbed. Although we were exhausted after the first course, the results were worth it. We ran our second course in February 1982 with our next-generation software tools.

Other interesting things were going on in parallel. In the VLSI business plan, we said we would design and manufacture state-of-the-art Read-Only Memories (ROMs) that would drive our manufacturing process. While we were working on silicon compilers, some other guys who had worked at Synertek and knew the ROM formula, were off in the corner designing ROMs. They completed their first product around the end of 1981, and then in 1982 came the video game boom which was very ROM-intensive.

In 1982, we did $22 million in revenue, all in ROM. In 1981, it was half a million in videotapes, courses, and consulting. VLSI was first perceived as a training company. Then when the 1982 video game boom happened, we had $22 million worth of ROMs and people said we were a ROM company. While the training and the ROM efforts were planned, they were never intended to be the dominant thrust of the company.

This entire time, we didn't have a wafer fab. In fact, we were the first fab-less semiconductor company. Since we were selling lots of ROMs, our customers were video game people. Our first custom chip was for a video game company called Williams in Chicago. As I recall, the class of February 1982 had about eight engineers.

Meanwhile, LSI Logic was pushing gate arrays and developing proponents. I had a meeting with Carver Mead in February 1981, right after we got our funding, and he recommended that we develop a gate-array capability. "You don't want to be in a position where you have to argue against LSI Logic," he said. "Have gate arrays in your portfolio. Tell people we'll do gate arrays and then switch them to our custom solution later."

Since we didn't believe that gate arrays were a good thing, we didn't take his advice. Anyway, there was no way we had the energy to do both.

JACK BALLETTO

According to our business plan, we needed $10 million in working capital, and later we would need $30 million for a wafer fab. When we managed to get venture capitalists interested in our concept they dug into the plan, and said, "Well, wait a minute, you said it was a $10 million deal, where are you going to get the $30 million for a fab?" We said we would figure that out later, but that it would probably involve some corporate investors. The VCs turned us down so many times, I felt like a Hollywood starlet going to an audition and hearing "You're too tall and you've got no boobs. Get out of town."

A couple of times we almost got lucky. Olivetti remembered us from the Synertek days and was willing to do the entire deal. We had a letter of intent in the summer of 1980, and it would take about six weeks to get their final approval. Two weeks later, we read that Saint Gobin, a French company, had just bought 25 percent of Olivetti stock. It turned out that this was the same company that had a joint venture with National Semiconductor in France. They had a huge empty semiconductor fab so our deal with Olivetti went on hold.

About then, some of the venture capitalists started to take us more seriously. Carver Mead's boss at Caltech, Ivan Sutherland, signed on as a special partner with an East Coast venture firm, Advanced Technology Ventures. Ivan understood what Carver Mead was saying and he started prodding his people, "Listen to these guys, what they're talking about is going to happen,"

Ivan was also a cofounder of Evans and Sutherland Computer Corporation, and he pitched their president, Dave Evans.

When we talked to Dave, we found that he was on the Board of Hambrecht & Quist. Dave Evans called Bill Hambrecht. "I think the VLSI business plan is plausible," he said. "You ought to listen to them."

After Hambrecht checked with some of his people, he told Dave, "It turns out some of my guys already talked to VLSI and they tell me it's all over in semiconductors. The future belongs to Intel, TI, and the Japanese–and that's it."

"Maybe there's something new happening," Dave said. "I think there's a new product and service opportunity in semiconductors and VLSI has a chance to be the leader.

From there our funding went quickly, and we rounded up $10 million. At the same time, the corporate guys started to come alive. Bendix had surveyed all their department managers to determine their strategic needs. Two of the top requirements were right out of our business plan: they wanted to do their own chip designs, and they wanted some control over a wafer fab.

Bendix was upset that they hadn't gotten in on our initial $10 million funding. We closed out our first round in December 1980 and they couldn't get the money authorized until the 1981 calendar year. So I went back to Bendix in January and said, "Look, there's another way you can get involved and that's to help us with our fab." So Bendix agreed to guarantee loans for the entire fab and we took down about $20 million in capital equipment that Bendix guaranteed at seven percent interest. Had we gone out on our own, we wouldn't have gotten the loans, but if we had got them through some miracle, it would have been at 18 percent or so–remember 1981?

Six months later, Olivetti came back in the picture and said they wanted to do business with us. They came in for another 10 percent funding, and agreed to buy about a million dollars in product the first year, and to put a design center in Italy.

VLSI was financed on a piecemeal basis. We took the working capital off the three-year plan and sold it to the venture capitalists. Then Bendix guaranteed a $30 million loan and Olivetti agreed to buy enough product to guarantee our first two years sales. *Voila,* we were in business.

One day Doug came in with a copy of *EE Times.* It had a photo of Steve Jobs and on his desk was the Mead-Conway textbook! So I called Steve and let him know that VLSI was the leading practitioner of Mead-Conway in the entire universe (Steve likes that kind of talk). The conversation led to VLSI's very early involvement in the Macintosh computer.

The early people at VLSI came from the same group at Xerox PARC that Apple courted for the Mac team. One time Apple and VLSI were trying to hire the same engineer and I got a call from Jobs. He reminded me how many ROMS and custom ICs Apple might buy from VLSI, and let on that he was personally interested in this particular engineer. The bidding stopped that day. We got no future draft choices, but Apple is still a very big customer of VLSI.

DOUG FAIRBAIRN

Our next milestone was the Bagpipe Project. It was the "lost summer of 1982." In one of our early classes, Burl Smith from Apple got excited about ASIC. He was the lead hardware designer for what was to become the Macintosh, and he convinced Apple management that they should pursue Mead-Conway technology to implement everything except the CPU and memory.

We had a handshake agreement, and we started the design with absolutely no formal arrangements. In fact, the day Burl Smith showed up, he said that since we were doing the ASIC as a side deal, we could throw out the existing spec and add more cool features. The day we started, we were two weeks behind!

We busted our pick for the next six months working on this chip–we were fighting power and size and everything. It had a very fast, dynamic memory control on chip and logic to control the video, the sound, the mouse, and the keyboard. We had nearly everybody at VLSI working on the project overtime.

As the project grew, we brought in more and more people because of the business potential. But just as we got the silicon almost working, Steve Jobs canceled the project. We learned an incredible amount from the experience, but it was a low point because we had just spent our hearts and souls on the project and it got cancelled. Apple could have introduced a fully integrated Mac based on this chip.

JIM ROWSON

While Bagpipe was a big disappointment, it did bring the Mead-Conway design philosophy out of the laboratory into the real world and pushed the tools and methodology to a much higher plane. We had to use and debug the software in parallel. Meanwhile, we were doing a lot of custom designs for other people. In December 1982, we came out with our first set of software tools to sell to customers. This was way before LSI Logic provided a competitive product. It was fundamental for us to get tools into the hands of the users that were sufficiently bulletproof so that the customer could, without talking to us, do their own design. That philosophy was the number-one goal for the software development team at VLSI since day one.

DOUG FAIRBAIRN

I moved the magazine activities into a real office and increased the staff during 1982, so I was not needed on a day-to-day basis. As time passed, the pressures of helping to grow VLSI and of keeping the magazine alive became too much for me; I had to choose. While I enjoyed the publishing business, it was always my "second" career. I didn't have the experience or

money to take the magazine to the next level, so I decided I had to sell.

Fortunately, the magazine was starting to establish a reputation in the industry for quality and innovation, and it was gaining the notice of other publishers as well as readers. In January 1983, I started getting calls from people interested in buying the magazine, by this time renamed *VLSI Design*. In May I sold it to CMP Publications in New York. CMP eagerly took over the publication and invested in it substantially. It did reasonably well for several years, but eventually the magazine fell victim to its relatively narrow focus, and was finally discontinued in 1990.

JACK BALLETTO

We were chugging along in 1982. Some of our memory guys were working on the next generation ROM and, on the side, working on a video game ROM. We had space in the Granger building, and one Thanksgiving I got a call from the security police at Granger. Some of our memory-design people were under arrest! Thanksgiving day they scaled the walls, jimmied the lock, got in, and were working on ROMs while everybody else was on holiday. I love those guys; they're nonstop workers.

I brought in Ron Kasper as the sales guy about a year before. I decided that what Fairbairn was talking about was so complex and tricky to sell that we had to get in a sales guy to fine-tune the pitch. Kasper had some spare time and heard from one of his cronies that Mattel was going to need a ton of game ROMs, so he went down to L.A. and walked into the Mattel lobby. It was a cold call–all he had was a prospect's name. After sitting in the lobby for six hours, the receptionist took pity on him and called the customer's secretary who agreed to let Ron go inside the closed area which was air conditioned. Ron's pretty smooth, so soon they're bringing him coffee and sandwiches. Finally the secretary says, "I'm going to put you in this chair

because your guy is inside the conference room having a meeting. When the meeting breaks, he'll have to walk right by this chair, and I'll flag you."

A half hour goes by, the meeting breaks, the guy walks by, she flags, and Kasper jumps up and introduces himself. The Mattel fellow had never heard of VLSI or Kasper, and as it turns out, he was the wrong guy anyway. The right guy was the VP of Purchasing who was in another Mattel facility halfway across the city. Ron's going crazy; he's been there all day, so the initial prospect says, "Let me call him for you."

Ron ended up having dinner that night with Mattel's VP of Purchasing and after two weeks, we received a $12 million order for ROMs! Al Stein had just arrived that day as our new president and he wouldn't take the order unless it came with an irrevocable letter of credit. Kasper and Mac Wilson, who had also just joined the company, went back and told Mattel that we couldn't take the order without an irrevocable letter of credit, and they got it! I don't know about those sales guys–it's incredible what they're able to do, because when they do their thing, it's scary. So we landed the Mattel order in April 1982. We were no longer just a training company, we were shipping silicon in volume. By the end of 1982 in eight months, we had shipped $20 million in ROMs.

In August 1982, we had a board meeting. All along, we'd been talking with GE. Now they wanted to get on the team and were willing to invest $20 million. "I don't think we ought to take the GE offer," Bill Hambrecht said. "I think we ought to go public." This was when Apple was at $12, the DOW was 780 and going down, and here Bill Hambrecht is telling us to reject the GE offer and go public. We took a vote and decided to do it; Bill Hambrecht must know what he's doing. He had foreseen the start of the bull market which started just six weeks after our board meeting. LSI Logic lucked out with a late IPO that hit the market peak.

I'm a founder of two companies, Synertek and VLSI. At $20 million in sales, Synertek was profitable, had a broad customer base, and was the leading supplier to two hot new industries: video games and home computers. Synertek was sold to Honeywell for about $25 million–or about our yearly sales.

On the other hand, VLSI went public with a market value of $400 million on just $22 million in sales even though it was losing money and had a very narrow customer base. Was it worth 15 times more than Synertek? The high tech IPO window lasted only five months and luckily our financial advisors saw it coming. Yes, it is important who you have as investors.

DOUG FAIRBAIRN

As VLSI continued to grow, I moved up steadily in the organization, finally taking over as General Manager of the ASIC Division in January 1987. In this role, I had responsibility for not only the design tools, but also the design centers and silicon products. Over the years the design tools evolved from the primitive text-driven tools we offered in our first class in 1981, to a set of integrated graphics-oriented tools dealing with the design process from logic synthesis through physical design and verification. The tools also expanded from dealing only with custom and cell-based designs to offering the user a choice between gate arrays and cell-based implementations. VLSI made the decision to move into gate arrays in 1984 and we had a competitive product by 1985.

Initially we were sure that cell-based ASICs would always beat gate arrays because they were cheaper and offered more flexibility. We felt it was only a matter of time before users would feel comfortable with cell-based products. Our analysis had two flaws. First, we didn't recognize that the large number of gate array suppliers would drive the prices artificially low. Part of the lower price was legitimate because the gate array's limited number of custom mask sets made their development

cheaper. Our second mistake was not realizing that arrays were flexible enough for most designers. Cell-based didn't have as many advantages for designers as we thought. Gate array's faster turn time and greater customer confidence will keep a major force in ASIC for the foreseeable future.

After nearly 11 years with the company and working so hard to see it successful, in November 1990, I regretfully decided to leave VLSI. It was time for me to move on and explore new opportunities.

In January 1991, I joined with Jim Rowson and Dan Yoder, both former colleagues from VLSI, to form a new company, Redwood Design Automation. From our experience at VLSI, we felt that systems designers had made tremendous progress in the 1980s in both productivity and design accuracy. However, the fact remained that over 50 percent of the chips we fabbed at VLSI had to be respun to get them completely correct. The ASICs almost always matched the function and timing specified by the designer, yet the design often wouldn't play in the system. Clearly the engineering community needed better tools to help get most designs correct on that first turn of silicon.

At Redwood Design Automation, we are starting down a new path, just as we did in 1980, when we put together VLSI Technology Inc. At that time, people had the feeling that custom chips would be beneficial to their system, but they didn't know exactly what tools to use, where to apply ASICs or how to design and test them. We solved all those issues. Now, in the nineties, people are asking the same questions about systems. Redwood hopes to solve these system problems just as we did for ASIC in the 1980s. That is our challenge for the 1990s.

ROB WALKER

In 1991, VLSI Technology posted revenues of $413.4 million, 59 percent of LSI Logic's revenues for that year. VLSI's profits were $9.9 million in 1991, 19 percent higher than those of LSI Logic.

ASIC SHORTFALLS

26 California Devices– An Early Leader is Overrun

California Devices Inc. (CDI) was one of the few merchant-market ASIC suppliers in the late seventies. They started three years before LSI Logic and by 1981, had garnered significant design wins. At that time, there was a several year delay between starting an ASIC design and achieving production volume. Bob Lipp, the CEO and founder of CDI, is a pioneer in the ASIC business. He designed the world's first CMOS gate array. He did a second-source licensing deal with LSI Logic in 1981 on his 5-micron gate arrays which jump started LSI's manufacturing with immediate production.

BOB LIPP

I went to California and joined National Semiconductor in 1972. I was there less than five months when National had a layoff. At that time National was on the NASDAQ, and they wanted to get on the New York Stock Exchange. Evidently, the NYSE required that a company on the exchange show a profit for five consecutive years. National was in danger of an unprofitable quarter so they had a big layoff to cut costs. Since I was in custom MOS, and we were doing great things, I thought I was safe. My buddy in the cubicle, on the other hand, was a RAM designer and he thought for sure he was going to get nailed. Of course, when the layoff came, I got hit and he didn't.

I went to a company called Micropower where I designed custom CMOS watch chips. I was with them for a couple of

years when I hooked up with Frank Deverse and Charlie Allen of International Microelectronics Inc. (IMI) which was making masks at the time. IMI was looking for something interesting, so they contacted me and we came up with the idea of making gate arrays using CMOS technology. I designed a 100-gate CMOS gate array. If it flew, I was supposed to get royalties and a piece of the company. We were pushing the state-of-the-art at the time. CMOS gate arrays were expensive and slow, but there were a few niche applications such as airplane strobe flashers.

CMOS arrays started hitting with the CB radio boom and all of a sudden there was a big demand for them. By then, we had expanded the line to a family of arrays from 50 to 400 gates complexity. As far as I know, mine was the first CMOS gate array ever made, and in my naivete, I never thought of patenting it. The row and column architecture was a completely new concept that probably would have been patentable, and had I gotten a patent I wouldn't be struggling today to make a buck. Just a few pennies royalty for each gate array made and I'd be a rich man today, sitting on the beach sipping a Mai Tai.

After about three years of nothing much happening, the gate array product started revving up during the CB boom. Frank Deverse had given me about $1,000 in royalties, and when we starting hitting it big, he realized he'd have to start paying me serious money, which he didn't want to do. He quit paying me royalties, explaining, "Well, if I had offered you $10,000 in 1974, you would have jumped at it." But that wasn't the deal. I took him to court in 1977, and after a three-week trial where he gave all sorts of excuses and reasons why he shouldn't pay me, I ended up getting a $120,000 award–real money in those days.

IMI really wasn't much more than a shell, subcontracting all manufacturing, assembly, and test. There weren't many assets I

could get my hands on. I finally settled for $60,000. Half of that went to my lawyers.

It appeared to me that CMOS gate arrays were a viable and growing technology, so with my $30,000 seed money, I founded California Devices, Inc. I hooked up first with Bernie Aronson, who was interested in being an investor. Bernie and I decided to bring in a third partner, Brian Tighe, whom we both knew pretty well, to referee any disputes. The three of us founded the company with a total investment of $50,000. I had predicted in my two-page business plan that I'd need about $60,000 and sure enough, after a few months I had to loan the company $10,000.

Since I still had some consulting contracts to complete, CDI had to be a part-time start-up. Bernie had an office complex in San Jose where I subleased an office and put a California Devices sign out in front above one of the doors. When one of my customers walked in they'd see all of the engineers from Bernie's company, and they'd think that my operation was much bigger than just me working part-time.

After the first year, I moved into my own offices and hired a few employees, four at first, and the next year twelve more. We did quite well. In just one year, revenue grew from $50,000 to a couple million.

Meanwhile, IBM had announced a mainframe computer which used gate array technology, and all of a sudden gate arrays were perceived as a growth business. I began to think that maybe I could make a big business out of CMOS gate arrays. I raised $700,000 in funding from three venture capitalists.

We decided to get into silicon gate CMOS, and in 1980 we joined forces with AMI in Santa Clara. AMI told us they had a 5-micron silicon gate process and we used it to design the product, a joint development we owned equally and which LSI Logic and Wang subsequently licensed. California Devices did the design; AMI did the tooling and production and was

confident that they could actually build it. AMI was running the 5-micron CMOS process in two manufacturing sites, Santa Clara, California and Pocatello, Idaho.

No sooner were we in production, than AMI lost the process at both the California and Idaho manufacturing sites. They couldn't give us enough silicon even for prototypes; we were left hanging by a thread. We got together with Universal Semiconductor to develop a substitute CMOS process that took six months to complete. AMI finally got their act together three months later.

The AMI fiasco used up our capital, and the venture capitalists who had invested in CDI–a small but well-run profitable niche business–believed I had misled them. It put my relationship with the venture people on a sour note from which it never really recovered. I guess that, from their point of view, no matter how much I tried to explain it, there was always that lingering doubt about me and the company.

About six months later, I managed to do another round of financing and got a fourth investor. By then we also started hitting periodic recessions in the semiconductor business in 1981 and 1984. It was a helluva time. We were slow to get into CAD. One reason was money–CDI was undercapitalized and we were still selling just the chips. Meanwhile, as the new paradigm of the ASIC business, LSI Logic was profiting from design services and computer time. It took us a while before we caught on.

LSI Logic was getting a lot of press, even initially, when the company was just the four founders–Wilf Corrigan, Rob Walker, Bill O'Meara, and Mick Bohn–with an idea. I was fascinated with how much money Wilf could raise and his projections for the size of the gate array market. At the time, I was skeptical that the market would ever be that large, but in retrospect, I guess their predictions were pretty accurate.

After we licensed our gate arrays to LSI Logic in 1981, we started receiving sizable royalty checks. By 1983, the money was

great but it raised the questions, "Why is LSI Logic selling four times what we are in our own product line?"

Conventional wisdom said that gate arrays were an interim technology that would be made obsolete by standard-cell and that eventually compiled circuits would take over ASIC. But the so-called experts didn't take into account that unit-volume-per-design was dropping. Typically each system had only one unique ASIC part, which meant that as time went on, gate arrays made even more sense, not less.

Every year, ASIC gurus like Dataquest would produce the same curve showing standard cell overtaking gate arrays in two years. It was crazy. They didn't seem to understand that development costs, time-to-market, and fear of failure are what drives the ASIC market.

In the classic handcrafted custom business, without CAD, the chip never worked the first time. Mostly, it worked the second time, but not 100 percent. And if you were really lucky, it finally worked on the third try. Each iteration took a three or four month turnaround, so typically you were a year late. Meanwhile, you were sweating it out the entire time asking yourself, "Is it going to work this time?" your stomach telling you that you may have missed something. Turnaround time and fear of failure kept gate arrays dominant over the standard cell.

After running CDI for five years, in 1983 I decided to step aside as president, hire a professional manager, and go back to managing technology. I thought a new CEO would regain the investor's confidence and I went on to design the first production "Channelless" or "Sea-of-Gates" array, a gate array populated by tens of thousands of transistors without specific wiring channels. CDI's channelless architecture was unique. We calculated that in its 3-micron configuration it was 40 percent smaller than LSI Logic's 5000 Series 3-micron gate array.

Unfortunately, CDI was never able to capitalize on the technology. In 1989, we went into bankruptcy, and our dream was shattered.

27 Wang Self-Destructs

In 1980, Wang was a high-flying computer company, and dominant in the word processing market. Wang had licensed from CDI's Bob Lipp the same gate array family that LSI was offering, and LSI targeted them as a major account early on. LSI was now in the perfect position to be Wang's second source or take the gate array business from CDI if they had problems.

SUSAN AYERS

The Wang semiconductor story started in 1978 when Dr. An Wang decided to invest tens of millions of dollars to build a captive wafer fab for Wang products. At the time, I was a young electrical engineer working for RCA at the Sarnoff Labs. I got a call from Dr. Spencer Hu, who had just signed on at Wang as Director of Semiconductor Design.

Dr. Wang was starting his new "technology adventure" called the Corporate Technology Center whose mission was to develop proprietary, high-performance custom ICs which would give Wang products a competitive edge and make them nonclonable by the Japanese.

The major semiconductor suppliers such as Intel, National, TI, RCA, and Motorola weren't interested in Wang's custom chip business because the volumes were too low to be handled efficiently by their fab lines. If a company was building a mainframe computer, it would sell maybe 100 to 500 systems a year. If it was building terminals, maybe it would produce 5,000 to 10,000 units a year. In the late seventies, merchant semiconductor suppliers were not set up to handle these low volumes. They

were interested in consumer-oriented semiconductors with volumes of 500,000 and up. When Dr. Wang approached the large semiconductor companies with his ASIC needs, they turned him down.

A more subtle influence was corporate pride. In those days, to be perceived as a leading Route 128 computer company, you had to have your own captive silicon design and fabrication in-house. Digital Equipment and Data General had their own fabs, and Prime Computer was planning one.

Wang wanted to be a major player and brought in experienced people from all over the world to staff the new organization. The vice president was Dr. Albert Belle Isle who came from a similar position with GE. He recruited people from GE, Digital, Prime, Motorola, and Silicon Valley companies. Wang started building a wafer fab in Lowell just down the street from the "Tower" of Wang headquarters. To build his dream, Dr. Wang was very generous with money; he wanted only the best. The wafer fab building, which now belongs to Macom, had state-of-the-art manufacturing clean-room technology and was on a par with the best that Silicon Valley offered.

I started work in January 1980 as the fifth person to be hired for the Wang semiconductor start-up, and was put in charge of building a design automation team. My charter was to procure commercially available software and hardware tools and integrate them with the manufacturing technologies; but the day I arrived, the Director of Software Development told me he was going to put me out of business in three years–his team was developing a proprietary design automation system tied tightly to Wang's technology and similar in functionality to the environment he left at IBM.

Two semiconductor technologies blossomed early in the Wang effort: the CMOS process which we licensed from National Semiconductor and the gate array we licensed from

CDI. National's fabs were in Salt Lake City, so Wang rented apartments there and many of us spent months in Salt Lake developing process expertise. At the same time, Wang approached Bob Lipp, President of California Devices and licensed his "323" gate array family.

One day in February 1981, I was sitting in my office at Wang. A light snow was coming down outside. I was listening to classical music, as I often do at lunch, and had my heels kicked off and my feet up on the desk and I was reading *EE Times*, when two people rudely interrupted the peaceful oasis in my office: a local semiconductor rep by the name of Don, and a well dressed man with a mustache named Bill. Don was one of those tenacious "in-your-face" reps–once he latched onto you, it was really hard to get away. "Oh, shit," I thought, "where do I hide?"

Don walked into my office. "Hey, Susan," he said, "want you to meet somebody. This is Bill O'Meara from LSI Logic."

"LSI who?" I asked. He told me that LSI was a new start-up in the Valley and that Bill O'Meara had a meeting with Prabhu Goel, but he was nowhere to be seen–he either forgot or blew them off for lunch.

I was irritated about getting caught off guard, so unladylike, in my office, so I quickly took my feet down, put on my shoes, took a look at my watch and said, "Bill, if you can't sell me in ten minutes, OUT you go! I've got things to do."

Bill smiled at the challenge, put his briefcase on the desk and took out a business plan. We started talking about the "vision" of LSI Logic. From what I could see, LSI had only been around for about a month and consisted of five guys and one desk, with a telephone receptionist shared by several other clients in turnkey offices somewhere in Silicon Valley. LSI Logic didn't have design automation tools and didn't have a fab. They had nothing, really, except a vision of the future. After 30 minutes or so, my secretary popped in and told me I had

meetings. I moved the meetings into my office to have Bill meet more people. He stayed for two hours.

BILL O'MEARA

After my lunch was canceled, our rep took me to the office of this gorgeous young woman. I figured she was a secretary or administrative assistant, but I was wrong. She turned out to be in charge of Wang's Design Automation. I started my off-the-cuff presentation, going through my transparencies using a white piece of paper as a backdrop. She got excited and kept stopping me to say, "Let me get someone to see this." After a half hour, there were five or six people jammed in her office. From this inauspicious beginning, Wang became our first large account.

SUSAN AYERS

The vision from LSI I saw back then was probably going to be the death of our Wang semiconductor organization. LSI Logic was everything that Wang's semiconductor group wanted and needed to be. LSI had financial backing and they were located in the heart of Silicon Valley. And they had top-notch people. Bill O'Meara's youthful entrepreneurial enthusiasm was something I hadn't seen at AMI or California Devices. I really believed Bill's story that LSI could deliver technology in a timely manner to Wang.

I had my secretary copy just about everything that Bill had in his briefcase. I ended up with the presentation and most of the business plan–every piece of information that would help me sell LSI Logic to my management. The rest is history. We got Bill and Wilf Corrigan together with Dr. Belle Isle and he formed an alliance with Wilf, Rob, and Bill at LSI Logic.

Wang was interested because LSI had licensed CDI's gate array, giving Wang a contingency just in case AMI couldn't fab our designs on schedule. If Lipp couldn't design it, we thought,

maybe these guys from LSI would come through. At the very least, LSI could provide a contingency to Wang's semiconductor fab.

A few months later, when I was out in California meeting with AMI and California Devices on some design tool issues, I was invited to visit LSI Logic. Silicon Valley companies grow fast! LSI was more than five guys and a desk: there were now about 25 people and they had just moved into a new industrial building in Milpitas. The building was so new that when you walked in, you were overwhelmed by the smell of glue from the carpet they had just put down that day.

LSI didn't have any cubicles up yet, so you could see from one end of the building to the other. Bill, Rob, Wilf, and Mick had their offices planned: they had masking tape on the floor and cardboard boxes piled up for a little bit of privacy.

Milpitas was the last area of the South Bay to be industrialized. All of a sudden, out in the middle of the onion fields, LSI Logic's building appeared. Milpitas? "Get real guys!" I said. "Silicon Valley is five miles away. No one will visit you in Milpitas." All the chip action was up around Moffett Field, and in 1981 Milpitas seemed like Outer Mongolia.

During the visit, I met Wilf Corrigan for the first time. Wilf has sparkling blue eyes like Paul Newman and a British accent. I also met Jim Koford and Ed "Too Tall" Jones, both of whom obviously knew their way around a computer and had insight into the needs of the end-user. Rob Walker knew design philosophy from a systems standpoint and was kind of cute. Rob and I talked about his plans for design automation, and LSI's plans to build quick turnaround gate arrays for the systems and computer industry that were not getting the attention of the traditional fabs such as Intel, Motorola, and Fairchild. LSI seemed just right for Wang.

Wilf, Rob, and I went to dinner at Ming's in Palo Alto where we sat around the table for most of the evening exchanging

gossip about the industry, trading West Coast and East Coast stories. We didn't realize that Don Hefler or one of his spies was lurking in the restaurant.

Soon after that, Hefler's *Micro-Electronic Newsletter* came out, a rag read by everyone in the industry and at Wang, especially by Dr. Belle Isle, an ultra-conservative East Coast type. He never had a hair out of place and wouldn't tolerate any of his employees getting "out of line." Hefler had written a little story about a dark-eyed "shady lady" from an "East Coast Chinese company" having dinner at Ming's and flirting with Wilf Corrigan and Rob Walker. The story implied that Rob was acting as cover for a romantic interlude between Wilf and me.

After the story ran, Dr. Belle Isle walked into my office with his jaw gritted. "Do you know anything about this?" he said. "Do you know who this woman is?"

"Well, I did have dinner with Wilf at Ming's," I admitted. "Yes, I guess that's me." His reaction was to clip my travel wings for about three months. Since I started my job at Wang I had been going out to Silicon Valley almost every week, but now I was allowed to travel only to Utah and Idaho. I got the "do nothing, go nowhere, and don't talk to anybody" schedule for the next several months; I guess Al felt I had caused a minor scandal. I thought, what the hell, women in the semiconductor business never did get much visibility.

Wang Microelectronics Center stayed active from its start in 1980 through mid-1983. Wang was in its highest period of growth, stock was soaring, and we added two more towers to our headquarters complex, making three. Wang became a tremendous presence in the word processing and computer market. Another recession in Silicon Valley in 1982-83 hit National Semiconductor, Intel, and Motorola. Suddenly these companies went vigorously knocking on the doors of Digital, Prime, Data General and Wang Laboratories.

In contrast with the mid-seventies to early eighties when they weren't interested in low volume ASIC business, now they were saying, "Hey, our fabs are open, come on in, we'll take anything you can give us. Want to do some gate arrays? No problem! We've got gate arrays. We've got all kinds of technology. You want to do custom chips? We've got that. We'll give you standard cells and help you build your own proprietary cells."

With the semiconductor majors' change in attitude, the future of Wang's internal start-up ASIC was in trouble. We had spent a small fortune on our facility and fab and we were still a year away from manufacturing a single device. Dr. Wang needed chips and the cost in the valley was right, so he shut us down and asked Al Belle Isle to resign.

Wang sold off the fab building and our group was transferred to the Vice President of Printers, Bob Chen. Bob, a hardware designer, knew very little about semiconductors. Unfortunately, he was having political problems within Wang. Bob had great enthusiasm for our survival, but Horace Tsang, a rival VP, wanted us disbanded. Horace was on his way up in the Wang organization and we were seeing first hand the power of the internal network of upper management at Wang known to the employees as the "Chinese mafia."

Eventually, Horace won power. Bob Chen's group was disbanded. Bob was sent to manufacturing and banished from the Tower, and Horace transferred or laid off all Bob's managers. Wang bought an equity position in VLSI, and Horace ended up on their board of directors. That's how the Wang internal semiconductor operation came to an end.

At the time, I was the only woman hardware manager at Wang, and because of the EEOC, I thought I was protected. Wrong! On the last day of the fourth quarter, I was called up to Fred Wang's office. I ran into Bob Chen and Spencer Hu on the way. "Susan," they said, "you were a good manager."

"What do you mean, was?" I asked. That day I received my transfer to manufacturing. I left shortly thereafter.

Slow reaction to a changing market, complacency, and the rise of personal computers left Wang in financial depression, losing millions of dollars each quarter. No longer a prime manufacturer of computers, Wang is more like a Super Var for IBM, their arch-rival of the eighties and the company An Wang vowed to beat.

Wang filed Chapter 11 bankruptcy August 18, 1992.

28 Intel ASIC– The Giant Blinks

While Intel had flirted with ASIC in 1971, their extraordinary growth and profitability had been built on the continuing flow of leadership products such as SRAMs, DRAMs, Microprocessors, EPROMs, Microprocessor Development Systems, and Single Board Computers. These innovations, now with yearly industry-wide sales in the tens of billions of dollars, were created by Intel.

In 1985, Intel was losing significant business to LSI Logic and other ASIC manufacturers. They assigned Jack Carsten, an executive vice president, to head up an Intel ASIC thrust.

ROB WALKER

Having worked for Jack Carsten at Intel from 1975 to 1980, I knew he was a talented leader and I was concerned that the combination of Intel, Carsten, and their license of IBM technology would be a daunting challenge to LSI Logic. In meetings with security analysts in 1985, they made it clear to us that since Intel had the microprocessor libraries and IBM technology, LSI Logic was in big trouble. Fortunately, they were mistaken.

JACK CARSTEN

I ran the TTL Department at Texas Instruments (TI) until about 1974. Business was exploding; when I left TI, we were doing $500 million a year. Then they asked me to rescue TI's MOS Department which was a real mess. I did that for about a year and then went out to Silicon Valley in 1975 to work for

Ed Gelbach at Intel. At that time, the microprocessor and the EPROM were the death knell of Fairchild's ASIC operation and I recruited Rob Walker from Fairchild to head up Intel's Marketing Communications.

ASICs had a bad name until the early eighties when Rob and Wilf got together. It was one of those things where the pendulum had swung too far in one direction. Intel had used a combination of EPROMS, RAM and microprocessors replacing what would have otherwise been the ASIC business.

That was the story until 1985. After ASICs started to become popular, Intel figured that they had made a horrible mistake letting LSI Logic and others run away with the ASIC market. In 1985, they asked me to do a study to determine the best ways for Intel to get into the ASIC business. I interviewed over 40 ASIC companies to learn the characteristics of a successful operation, the roles played by CAD, quick-turn silicon manufacturing, and cell libraries.

I concluded that the world's most successful producer of ASICs was IBM. They had continued to produce ASICs in high-pin count packages using advanced CAD throughout the seventies and eighties. I felt that since they still had a very powerful proprietary technology, they could give Intel a unique edge. At the time, Intel had a very close relationship with IBM; they owned 20 percent of Intel.

We struck a deal with IBM to license their gate-array line. We also got rights to their unique flip-chip packaging technology and CAD tools that they had developed over the years. The IBM cell libraries would be made available to Intel for our exclusive use in the merchant ASIC market. My theory was that although their CAD proved to be inadequate, we could use it as a core and a marketing vehicle, then we could enhance it. At a minimum, we were tapping into the IBM ASIC market where Intel would be the only other source. I was quite confident

that we could supply ASICs to IBM cheaper than they could build them given their incredible bureaucracy and cost structure, and by doing so, we would get a nice share of IBM's $2 billion yearly ASIC usage.

So much for theory. After we signed the deal, we evaluated the IBM software, and found some problems. It was mainframe based and had been optimized for bipolar technology. The IBM design automation tools and methodology were all based on a test protocol called LSSD. IBM had designed their tools so that you could not get the design manufactured unless you met all of their rules, including 90 percent test fault coverage. By doing this, the IBM manufacturing group forced much of the responsibility for quality back onto their users so that the divisions wouldn't get beat up for designs that didn't work or failed in the field.

The LSSD design philosophy arose out of a unique interdivisional warranty within IBM which stipulated that the semiconductor people had to pay the service and repair cost for every piece of IBM equipment that failed within five years because of a defective component. The LSSD requirement came out of a reasonable mainframe policy, but it is not the way to operate in the fast-moving PC and peripherals arenas and it is symptomatic of why IBM is lethargic and bureaucratic in their use of ASICs.

The IBM design methodology wasn't flexible. If you wanted to add a new cell to their library for example, it was a year's project, unacceptable for many applications. If you wanted to introduce a new process, you had to go through a characterization procedure, plugging all of the new parameters into the cell library. The time required to do that was just unbelievable. We thought the underlying problem was not IBM's CAD, but their rigid design style. IBM recognized their weakness and began in the mid-eighties to commit to fairly wide use of

merchant-market ASIC technology and methodologies, buying CAD tools from VLSI, Seiko and LSI Logic.

IBM had a lot of good automatic test program generation tools and automatic place and route capability. They certainly had well-characterized designs, and very good packaging. Unfortunately, this came at the expense of flexibility since the mainframe people could not afford to come out from under the IBM umbrella and lose the warranty coverage. If an IBM division bought components on the outside and the component failed, the division using the part had to pay the warranty costs, so there was tremendous incentive to stay inside and be protected from the subsequent costs of any problems that might develop.

The culture became so inbred that although IBM was the world's largest ASIC user and manufacturer, they were also slowest to develop new silicon or CAD technology. I think that explains a lot of the problems with IBM's ability to stay competitive.

Another challenge for us at Intel was interfacing the IBM tools to commercial CAE vendors such as Daisy, Mentor, and Valid. Back in those days, the CAE people supplied sort of a womb-to-tomb solution which, while not particularly cost-effective or efficient, was easy to use. When Intel entered the ASIC business, one of our challenges was to take the merchant market schematic entry and simulation packages from Daisy, Mentor, and Valid and plug them into the IBM cell library. IBM was interested in the effort because within the company they had maverick groups who wanted to use outside CAE.

Logic libraries were another problem. Certainly, when I was trying to get the Intel ASIC business going in the mid-eighties, libraries and proprietary cells were crucial. The tricky part was that many of the most desirable Intel proprietary functions, for example the peripheral circuits required for a PC, were not well

characterized. In addition, the vendors like Intel or Motorola who developed them didn't want to reveal to ASIC users the detailed innards such as the models, test programs, and other particulars needed to do a high-performance version–they didn't want anyone to rip them off.

We also encountered intense need for higher system performance, particularly in the PC arena. All the clone makers were in hot competition. They were under continual pressure to increase the clock speeds of the peripheral circuits well beyond what they had been designed for. Typically, the processor could outrun the peripherals so you were always running them with negative clock edges and other marginal schemes that were the result of starting with a poor design and then trying to double the clock rate. The designs had a lot of multiple clock edges inside and other scruffy stuff.

I'll admit to being guilty of helping create this monster because when I was in charge of the Intel Microprocessor Division, a lot of the peripheral circuits were not designed by Intel but by our second sources. The 8237 was designed by AMD, and the NEC 765 was the CRT controller. We didn't put any design methodology requirements on the second sources. Instead, we gave them a spec for a 4MHz part, they gave us back the silicon, and we in turn gave them rights to the 8086, or whatever the deal was at the time. We were very naive about what a fair trade was, so we helped create this monster.

Another negative factor was the IBM gate array packages–they used a custom two-layer metalization on ceramic substrates that was unique for every ASIC design. Even IBM used a wire box for prototyping because of the amount of tooling required. We had to layout the substrates, etch them, and run all the packages through the furnace. Once you got a design rolling in high volume, the cost was actually quite low and reliability was good. In fact, I think it's the best way to

make multi-chip modules. But, in terms of ASIC prototypes, it was awful because the tooling requirements were so horrendous.

For example, to do solder bumps on the chip you had to have an etched metal mask to evaporate a tin-lead metalization using a $2 million evaporator. Now, if you knew how to design the masks, where to procure them, went through the cost of making them, and had these huge evaporators, then you could do it. Packaging cost associated with any yield loss provided another stumbling block, particularly on a large die. When added to the costs of the silicon yield, the creation of new tooling was very expensive.

A windfall from Intel's ill-fated ASIC effort came from Intel's using the capability internally to develop peripherals–the PS-2 chip set being the first. We very successfully developed many peripherals in the late eighties using both gate array and standard cell ASIC technology.

After we solved most of the software, packaging, and silicon issues, an event occurred that ultimately killed Intel ASIC. IBM decided to close the PC architecture by developing the PS-2 which they changed somewhat arbitrarily from the existing PC architecture. For example, they changed the CRT interface from digital to analog, the keyboard, the BUS protocol, the structure of most of the peripherals, and the addressing mechanism. These were among the many arbitrary changes serving no practical purpose other than to try to get the clones off of IBM's back.

Clone makers reacted by pressuring Intel to reverse engineer the PS-2 chip set. It would have been a relatively straightforward job, since we had the IBM CAD tools and there was nothing in the contract that said that we couldn't supply the capability to the clone makers. IBM made it clear, however, that if we supported PC clones with the IBM tools and cell library, they would cancel all Intel ASIC business and the joint ASIC

agreement. They would also stop updating the computer tools and supplying us more packaging technology.

Intel had to make a decision. Their relationship with IBM was deteriorating. IBM was in the process of selling their interest in Intel, and the relationship was cooling considerably even though IBM remained Intel's largest customer. Intel decided to go ahead and support the PS-2 clones in spite of IBM's opposition. That decision put the kibosh on Intel's ASIC program because we lost IBM, our largest potential customer, we lost the tremendous effort we had put into packaging IBM's CAD, and we lost the image of having world-class ASIC capability.

We continued with a microcontroller core-plus cell program that had some modicum of success, sort of a custom microcontroller at the level of a 8051 or 8086. But in 1988 we decided, and rightfully so, to shut down the gate array effort since IBM was no longer a customer.

That's the summary of the rise and fall of Intel's gate array business. Now I'm in venture capital, and I often recommend to start-ups needing ASICs that they use gate arrays from someone like LSI Logic. ASIC consultant Andy Rappaport was running around in the mid-eighties insisting that 80 percent of ASICs was going to be standard cells and that the gate arrays would die because of limitations in cost and performance. In my view, gate arrays are relatively simple, easy to characterize, and easy to tune to a new process. In practice, arrays are always a year or two ahead of standard cells, and if you accept that as a given, then most of the advantages of standard cells go away.

ROB WALKER

In March 1992, Intel announced they were pursuing an alliance with VLSI Technology Inc. Intel would acquire a 20 percent stake in VLSI, and use their ASIC expertise in the PC arena.

ASIC IN THE NINETIES

29 Time to Market

A key factor for success in electronics and probably ***the*** *dominant factor in markets of the nineties, is time-to-market. In the workstation and personal computer business, products have a sales lifetime of about 18 months. A delay of only a few months in reaching production volume can turn success into failure.* Business Week *reported in their May 25, 1992, issue, "The [Apple] Mac Hardware Division must churn out more hit Macs–and do so faster while keeping costs down." The goal: In 1993, new products are due* ***every six months****.*

LSI Logic has always been strong in delivering ASICs that were right the first time, an obvious requirement for getting a product into production. But in 1985, production of prototypes took us six to eight weeks. In contrast, now LSI's prototype production time has been reduced to two or three weeks. This accomplishment is largely because of George Wells.

After positions of increasing responsibility at ITT, GTE Sylvania, and Fairchild, George ended up running all of General Electric's semiconductor operations. In 1985, Wilf recruited George to LSI Logic.

GEORGE WELLS

I can remember when I first came to LSI, sitting in staff meetings and Wilf asking me, "What do you think of our company?"

"I don't think you guys understand how far ahead you are in this business," I said. At GE, the engineering execution and aggressive marketing of LSI Logic were legend.

I was wondering how the hell I was going to contribute, and show all these bright guys at LSI that maybe Wilf wasn't crazy to recruit me. Already I was getting calls from customers asking me to accelerate prototypes. Suddenly, my engineering background kicked in and I thought to myself, what if I was one of our customers and had all standard logic and memory parts plugged into my system, and I was waiting for the ASIC to find out whether I had invented something really good, or whether I had a disaster on my hands. What a gut-wrenching ten weeks that would be.

I talked to Rob about prototype turn-time and he said, "We've been pushing to reduce turn-time, but we just don't seem to be able to get any improvement." So I decided to see what I could do.

It was classic problem solving: you break the problem into parts and assign responsibility to individuals to accelerate each step. For example, purchasing buys the masks, so buy them more quickly. In 1985, it took two weeks to procure masks. I set a week as the new goal. In our staff meetings, we would set goals for each guy and he'd say, "Well, I need help from so-and-so who's not in the room." So we'd get them in the room and say, "Your job of metalizing the wafers is taking five days, the new goal is two days. We're going to measure every segment from start to finish." After two years, I didn't even have to ask for data. It was always presented at business reviews.

In a speech I gave at SEMI in late 1986, I said that we needed suppliers to support our goal of reducing turnaround time. I told them that if the mask makers insisted on having a two-week turnaround time, there was no way I could make my goal and that if they wanted to continue to do business with us,

they had to turn out their masks in days, not weeks. I set them a goal of three days.

After my speech, Joe Ross, Chairman of Micromask, came over. "You know," he said, "I believe what you're telling me. The problem I'm having is that my people don't understand. I can't convince them that the fast turnaround you're asking for is possible at Micromask. Will you come to my company and tell them what you just told this group tonight?" I said, "Sure, if it will help me get my masks in sooner, I'll come." And that's what I did. Joe invited me over, they had the whole company there, and I talked to them about the need for fast turnaround on masks.

Six months later, Micromask was delivering masks in three days. "I want to thank you a lot," Joe said. "Not only are we able to meet your goals for LSI, but we're able to help all our customers get their masks out much faster. Our fast turnaround has given us an edge on our competitors. I'm doing a lot more business now, thanks to you. In fact, you saved my company."

Turnaround time with the right product became crucial for us to succeed with our ASIC customers. I can remember when we were doing our first 50,000 gate channel free array for a customer in Phoenix, and Steve Chan, one of our senior engineers, would appear in my office every morning. The conversation would start, "Okay, Steve, how many uncompleted nets in the layout are left?"

"Oh," he would say, "we've still got 235 nets," and the next day, we would meet again.

Meanwhile, every day our customer would be calling to ask, "How are you guys doing?"

"I can't tell you when we are going to deliver until I know that we have completed the layout," I would say. The day finally arrived when Steve said, "We're down to eight unconnected nets and we'll have them finished by hand tonight."

I called the customer and told him he would have his first prototypes within three weeks. He was overjoyed, and so were we. We had completed the industry's first 50,000 gate array.

Two days after receiving the prototypes, the customer called me back. He was all over me. "George," he said, "guess what? Your ASICs work. Even though you kept me waiting for a commitment, we are three months ahead of schedule. We thought we were going to have to rework the ASICs before we could begin our software development."

Zycad is another success story. When they were preparing to build a new product and ran afoul of Seattle Silicon, we turned their circuits around in just a couple of weeks and were able to produce enough parts for them to go to an important trade show. The President of Zycad came up to congratulate me. "You guys are the greatest," he said. "I love you. You saved my tail."

Another story illustrates the discipline we've been able to achieve. One Saturday, K.K. Yawata, the president of our Japanese affiliate, called me at home. "George," he said, "I need your help."

"Okay," I said, "but it's noon Saturday and I'm getting ready to go play golf."

"Your supervisor on the test floor has defied the president of your Japanese company!" said K.K. "She won't ship the prototypes that I need. I understand you have a rule that, if the prototypes don't pass the test, you don't ship them."

"What's wrong with that?" I said. "Why should we ship a prototype if the test says it won't work?"

"Because," K.K. said, "the prototypes work in the customer's boards and they need them for a demonstration they're giving next week at a big show they have to go to."

"You understand, K.K., I won't start another wafer until you sort out the test problems," I said. "If we ever get to volume manufacturing the test must be clean. Promise me you'll do that."

"Absolutely," he said.

So I called the supervisor and said, "Look, I'll come in Monday morning and sign a waiver to absolve you of any blame. Just ship the prototypes untested."

So we shipped the prototypes to K.K. and they went into a studio camera that was being built by Matsushita, beginning what was to become an important relationship. I was quite pleased but not surprised that an LSI line supervisor had stood up to an affiliate president. That's exactly the kind of discipline we expect from every employee.

Silicon Graphics was also one of our successes. They had rooms filled with boxes that were waiting for boards, and the boards were waiting for two ASICs. When their ASIC vendor called to say that they were going to miss delivery they were losing a million dollars in revenue a day.

So they called me. "Hey," they said, "we're stuck. We went with the wrong ASIC guys, we know that. Could you do a prototype of the chips and have them delivered in two weeks along with production parts?"

"You mean, you don't even want to check the prototypes to make sure they're okay?" I said.

"No, we don't have time for that and besides we know your prototypes always work. We know they're going to be okay."

I was a bit nervous, but fortunately, we were able to deliver production quantities in only eight days and they got their million dollars a day in revenue and made their quarter. Without us, that wouldn't have happened. It makes me proud to provide solutions like this to our customers.

30 The RISC Revolution

Microprocessors, which have been around since the early seventies, have radically changed electronics. In fact, they were one of the factors that derailed ASICs for a number of years. Traditionally, microprocessors have been stand-alone circuits, surrounded by a large number of memory and peripheral chips. As we move into the nineties, a number of trends have emerged that continue to revolutionize the use of microprocessors.

ROB WALKER

One or more microprocessors now make up the computing power of virtually all computers, whether mainframe, minis, workstations, or personal computers. In some applications, microprocessor cores have become megacells–not just stand-alone ICs, but imbedded in a larger integrated circuit, resulting in significant cost, performance, and size advantages.

Reduced Instruction Computer (RISC) architecture has revolutionized the microprocessor market in the nineties. Intel and Motorola emerged after the microprocessor wars of the eighties as the world's two monopolistic microprocessor suppliers and seemed unbeatable.

In 1990, we felt confident that the future of microprocessors belonged to RISC. Two leaders in the field, SUN microsystems and MIPS Computer had developed RISC microprocessors with much improved price performance over existing merchant-market or proprietary microprocessors. Because neither SUN nor MIPS had its own semiconductor manufacturing, LSI Logic licensed both designs for stand-alone and megacell use,

lured Brian Halla away from Intel, and got heavily into RISC microprocessors.

In 1992 the future is less clear. Intel has rebounded with increasingly powerful PC-compatible conventional microprocessors, in some cases more powerful than the MIPS and SPARC offerings. Digital and Hewlett-Packard have developed their own RISC architectures which have impressive performance, and they are now licensing them to other computer manufacturers. IBM has joined with Apple and Motorola to embed IBM's RISC architecture into Apple's future products.

Meanwhile, MIPS has been struggling with its R4000 machine, is losing money, and has been acquired by Silicon Graphics, a workstation company. Several of their customers have abandoned the MIPS architecture for those of Digital, HP, and primarily Intel. At SUN Microsystems, sales have flattened and SUN is in danger of losing its performance edge to others.

In April 1992, LSI consolidated its ASIC and standard products (including MIPS and the SPARC RISC microprocessors) under Brian Halla. This reorganization underscored the belief that customers demand the most cost-effective and highest performance solution and that nuances between standard ICs and ASICs were becoming irrelevant to them.

The future winners and losers in the microprocessor wars are not clear. But we can, with some confidence, make three observations.

Users will continue to enjoy more powerful computers and other electronics at increasingly lower cost. RISC technology has forced Intel, Digital, and HP to innovate at the fastest possible pace, meaning that like Moore's law, computers will exhibit a doubling of price performance every eighteen months or so throughout the nineties.

The United States has been supreme in microprocessors, and that shows no sign of changing. There appears to be no

Japanese or European threat on the horizon that can compete in microprocessors with the likes of Intel, Digital, HP, SUN, or Silicon Graphics/MIPS. This market exhibits American competitiveness at its best.

Finally, as the system becomes a single chip, the microprocessor will increasingly become a megacell within an ASIC. An end-product's unique features will require a custom solution and the ASIC market will continue to grow, but in a different format.

31 ASIC–The Future of America?

After eleven years, LSI Logic is now a Fortune 500 company and number one in gate arrays in the United States, Europe, and Canada. Even in Japan, LSI Logic is a major ASIC player. LSI's revenues in 1991 were $698 million, in spite of the recession. In-Stat, a Scottsdale, Arizona marketing research firm, estimates the worldwide ASIC market is still high growth and will double to $13.2 billion in 1995.

LSI's latest CMOS technology, known as the 300K process, uses 0.6 micron design rules to obtain 0.45 micron effective gate length. In contrast with their 1981 product which was limited to 1200-gate complexity, the 300K technology allows designs to go up to 600,000 gates! That means a designer can specify a one-chip system of 200,000 gates, 512K-bit SRAM, and one-megabit ROM.

The fast-turn ASIC technology has also allowed LSI Logic to enter the "Application Specific Standard Product" (ASSP) market. Sometimes called "chip-sets," the concept was popularized by Chips and Technology. Systems expertise and intellectual property, for example in personal computers, RISC computers, or HDTV, are supplied by the semiconductor manufacturer in the form of off-the-shelf products allowing customers to clone successful, high-volume systems with a minimum of

engineering investment. Margins of ASSP are superior to ASICs because they contain unique intellectual property.

ROB WALKER

Unfortunately, LSI Logic's revenue and market-share successes have come at the expense of profits. Going up against the best of the world in designing and manufacturing semiconductors is an expensive proposition, as investments in advanced R&D and new manufacturing facilities have left little margin for profits.

The *San Jose Mercury News*, April 6, 1992, said of LSI Logic:

In Japan, LSI Logic Corp. is viewed as a fierce competitor and a company others want to emulate. But in the United States, the Milpitas chip maker is more likely to be used as an example of how not to run a company–at least by Wall Street and industry analysts, some of whom view the company with indifference and don't recommend the stock. Years of battling to be No. 1 in the cutthroat and crowded customized chip market made LSI among the top three in the world [the other two are Japanese], but it also burdened the company with large, expensive and under-utilized manufacturing plants and too many people for its size."

Measured against our competitors, LSI has done well. Niche ASIC players ZYMOS, Universal Semiconductor, and California Devices have left the market. Major semiconductor suppliers such as Intel, Fairchild, National, GE, RCA, Hughes, Gould, and Harris have thrown in the towel on ASIC. Some U.S. ASIC suppliers are barely hanging in. Motorola, Texas Instruments, AT&T, and NCR are still in the business; however, their combined 1991 ASIC revenue was less than that of LSI Logic. Captive ASIC suppliers such as IBM, Digital, and HP soldier on, but other captive efforts from Unisys, CDC, Tektronix, ITT, Westinghouse, Wang, and Data General are now history.

Japanese giants NEC, Toshiba, Fujitsu, Oki and others continue to be major forces in ASIC.

Our Japanese affiliate, LSI Logic K.K., is a fast-growing operation. We still hope to take it public someday on the NIKKEI exchange.

We've done the things that we considered necessary to be a world-class competitor. We've spent heavily on R&D. Our worldwide operations are staffed almost totally by indigenous personnel. We've financed international expansion using local investors. Our executives receive modest salaries and fly coach or business class on their trips–there are no LSI Logic corporate jets or helicopters. We invest for the long term rather than the next quarter because our management has a long-term commitment to success.

Wilf Corrigan, in 1992, took a number of steps to improve profitability. Wafer fabs in Europe and Canada were closed. Packaging plants in Germany and California will be phased out. The U.S. wafer fab will become a fast-turn prototype facility. A second, very advanced wafer fab will come on line in Japan. Employee count has been reduced. In April of 1992, Wilf reorganized, combining all engineering and marketing for ASIC and standard products.

The Iacocca Institute at Lehigh University issued a report in November 1991 titled "21st Century Manufacturing Enterprise Strategy." The report concluded that:

Arguing that "Competitive advantage in the [21st Century] system will belong to agile manufacturing enterprises capable of responding rapidly to demand for high-quality, highly customized products ... ASICs ... [were] founded in this atmosphere of rapid innovation, technological and entrepreneurial dynamism, [and] high stakes uncertainty ... in short, in an atmosphere particularly well-suited to American strengths."

VEN LEE

I think the ASIC success formula has changed in the nineties. Large and mid-sized ASIC customers have been well trained by LSI Logic, VLSI and others. They know the basics of ASIC design and now are looking for lower costs and more flexibility.

I've founded a company called OASIC (for Open ASIC) to address the sophisticated customer's needs. They can use their corporate CAE tools such as those provided by Cadence or Mentor; we will supply the logic elements, models, and master-slices. They can then take their design and bid it out to a number of approved silicon suppliers. From our standpoint, we duck the costs of fab, CAE, and heavy application support which allows us to be a pure technology supplier.

We've capitalized on our LSI Logic experience by automating many design tasks. For example, we have developed a program that accepts the physical design, the logic model and SPICE parameters of a macrocell and generates 250 SPICE simulations over temperature, voltage, input transition time, and loading. From this database, we automatically generate logic models for Synopsis, Verilog, and Mentor.

This may sound like the old (and unworkable) Carver Mead silicon-compiler scheme, but it is fundamentally different. We work with only a few silicon manufacturers who pay us a licensing fee for being on our supplier list. We optimize the design for each manufacturer so the ASICs are identical in function and performance. But design relating to latch-up, static discharge protection, and electrogration are unique to each supplier. These details are transparent to the ASIC customer; we and the foundry take care of them. We also characterize and life-test devices from each supplier; this is not your father's old silicon foundry concept.

We're just getting rolling at OASIC. The next few years will prove if we are another LSI Logic or another Edsel.

TSUYOSHI KAWANISHI

At Toshiba, even commodity products are now being personalized. Customers want to implant their unique features into the chip, even in previously standard products such as memory and discrete devices. They need this customization to obtain the best value, cost, and performance, and to tailor their product to their market segment. To fully satisfy our customers' needs, the semiconductor manufacturer must cooperate closely with their customers in the technology.

Low-profit margins are a continuing problem in ASIC. If semiconductor manufacturers want to achieve adequate margins they must increase their intellectual property. The silicon foundry concept of dumb manufacturing just doesn't provide us an adequate return.

At the risk of strengthening my competition, I believe America must get its act together in manufacturing. These "fabless" chip companies may look good for a while, but ultimately their lack of manufacturing capability will prove fatal. I believe the triad of hardware, system, and software must be in balance for long-term success.

Americans don't seem to realize the problems we face in Japan; for example, too few people and a very expensive infrastructure compared to the U.S. You can be very competitive if you choose.

WILF CORRIGAN

It's clear that the ASIC formula is changing and expanding. Now that we can put the entire system on a chip, the question is how that will be accomplished.

I think that something I call "Object Level Design Methodology" may be the answer. In this process, designers would select a processor, RAM, ROM, and special logic with just a few commands. We at LSI Logic can quickly turn their ideas into silicon. I think this will be the system design of the nineties.

Altos Xerox's first personal computer.

ASIC Application Specific Integrated Circuit. An integrated circuit designed and manufactured for a single customer.

Auto/Interactive Place and Route A computer-aided technique for IC layout that uses automatic algorithms to locate and interconnect elements on a chip, but still allows human interaction.

Automatic Schematic A computer aid that generates a schematic diagram from a non graphical description.

Back-Annotation A computer aid that extracts interconnection detail from the chip layout so that the circuit delays may be more accurately modeled.

Behavioral Simulation A computer simulation of a circuit that utilizes more abstract high-level (i.e., not transistor or gate-level) descriptions.

Bunny Suit The protective uniform worn in wafer fabs.

CAD Computer-Aided Design. Computer programs that assist the user in design activities; within the context of this book, the design of integrated circuits.

CAE Computer-Aided Engineering. Computer programs to assist the user in engineering activities; within the context of this book, the engineering of ICs; synonymous with CAD.

Cal University of California at Berkeley.

Calma A computer-based graphics design system that was a standard IC design tool in the seventies. Calma was purchased and mismanaged by GE and sold to Valid Logic which was merged into Cadence in 1992.

Caltech California Institute of Technology, located in Pasadena, California.

Channel Free LSI Logic's name for a gate array without specific wiring channels.

Clock Speed A measure of circuit performance.

CLM A 1970 Fairchild name for what is now called a PLA.

C-MDE "Concurrent Modular Design Environment." LSI Logic's third-generation design-automation system, circa 1992.

CMOS Complementary MOS. Currently the most popular semiconductor technology because of its density, speed, and low power.

CPU Central Processing Unit. The brains of a computer.

CRT Cathode Ray Tube. The screen on a computer or TV, for example.

Custom Circuit Term used before 1983 for Application Specific Integrated Circuits.

David Mann Pattern Generator The earliest automated mask generation system, circa 1970.

Design Center A resource for custom ASIC design support, including customer training, workstations, and application engineers. Typically located near the customers.

DIP Dual-Inline Package. An IC packaging technology invented at Fairchild in the 1960s.

DRAM Dynamic Random-Access Memory. A memory IC in which stored data must be reconstituted on a regular basis.

DRC Design-Rule Checker. A computer program that checks if a chip layout meets manufacturing design rules.

DTL Diode-Transistor Logic. The second Fairchild integrated circuit logic family, circa late 1960s.

ECL Emitter-Coupled Logic. A bipolar process which in the early 1980s offered the highest performance.

8051 Intel's 8-bit microprocessor.

8085 Intel's 8-bit microprocessor.

8086 Intel's 16-bit microprocessor.

Electronic Design Automation Computer programs that automate portions of electronic system design.

EPROM Erasable Programmable Read-Only Memory. A PROM that can be erased by shining ultraviolet light through a window on the IC.

Evergreen License A license in perpetuity.

Extraction A process in which after the actual interconnection parameters are known the "extracted" values of resistance and capacitance are used to fine-tune logic simulation. Same as back-annotation.

Fairchild Fairchild Camera and Instruments Corporation. Inventor of the integrated circuit in 1958 and the father of all Silicon Valley semiconductor companies, based in Mountain View, California. Fairchild Semiconductor was sold to National Semiconductor in 1990.

FAIRSIM The Fairchild logic simulator, circa 1967.

575 Tektronix Curve Tracer An instrument that analyzes the DC performance characteristics of transistors.

Floor Planning Planning the layout of the major functions of an IC.

FMGA The first gate array invented at Fairchild in 1966.

FPGA Field-Programmable-Gate Array. A logic element that emulates a gate array, but whose function is programmed after manufacture.

Gate Array An ASIC that is fabricated from the interconnection of a standard array of components, typically transistors.

Gates A measure of ASIC complexity. In CMOS, four transistors per gate.

Genesil The computer tool from Silicon Compilers Inc., circa 1983.

Glitch Detection The detection of very short elecrical pulses that may cause malfunction in an electronic system.

Going Public Synonymous with IPO.

Golden Simulator The logic simulator that an ASIC manufacturer uses prior to final commitment on an ASIC prototype. The actual circuit is guaranteed to meet or exceed that predicted by the "golden simulator."

Graphics Editor A computer system that allows manipulation of graphical elements.

IC Integrated Circuit. Circuit elements such as transistors, resistors, and capacitors interconnected on a single monolithic semiconductor chip.

Interconnection Delays The electrical time delay caused by interconnection of active elements.

IPO Initial Public Offering on a public stock exchange.

ISL Integrated Schottky Logic. A bipolar process popularized by Signetics, circa 1980.

LDS LSI Design System. LSI Logic's first CAE ASIC design-tool set.

Logic Simulator A computer program that simulates a digital chip or system.

LSI Large Scale Integration. An integrated circuit of at least 500 gates on a single chip. Also an acronym for LSI Logic Corporation.

LSIM The LSI Logic Corporation logic simulator, embedded into MDE.

LSSD Level-Sensitive Scan Design. A structure for testing ICs, boards, and systems developed by IBM.

Macrocell A logic element in an ASIC, usually 20 gates or less.

Masterslice The standard array of components that is custom interconnected to become a gate array.

MDE Modular design environment. LSI Logic's second-generation design automation.

MDS Microprocessor development system. Intel's name for the hardware and software used to develop microprocessor-based equipment.

Megacell A physical block of logic of over 1,000 gates.

Metals Fab A manufacturing facility that adds the metal interconnection to a masterslice. A metals fab provides a lower cost option to manufacturing the entire IC.

Micromatrix Fairchild's name for gate arrays in the 1960s.

Micromosaic Fairchild's name for Standard Cell ASIC, started in 1968.

MITI Japan's Ministry for International Trade and Industry.

Moore's Law Gordon Moore, then Fairchild's Vice President of Research and Development postulated, in the late 1960s that the number of components (i.e., transistors, resistors, capacitors) that could economically be implemented on a single chip of silicon would double every 12 to 18 months.

MOS Metal Oxide Semiconductor. A type of semiconductor technology that came into vogue in the 1970s.

Motorola 68030 A 32-bit microprocesor from Motorola.

MSI Medium-Scale Integration Standard ICs that provided generic function of 50-1,000 gate complexity.

Multi-Chip Module A small electronic module containing multiple chips.

Multi-Chip Simulation Logic simulation of two or more ICs.

Netlist An alphanumeric description of an IC.

NSI Nippon Semiconductor Inc. A joint venture of Kawasaki Steel and LSI Logic that manufactures ICs in Japan.

NRE Non-recurring Engineering cost. The cost to design and produce ASIC prototypes.

NUMMI A GM-Toyota joint venture to manufacture cars and trucks, located in Fremont, California.

PAL Programmable-Array Logic. Simple, programmable logic ICs.

PARC Xerox's Palo Alto Research Center. The personal computer, laser printer, and Ethernet were invented at PARC.

PC A personal computer that is compatible with IBM personal computers.

PC Clone A computer that is program-compatible with the IBM personal computer, but not supplied by IBM.

Peripherals In this context, special purpose ICs used to interface a microprocessor to various input/output devices.

PG Tape A magnetic tape containing the physical description of the multiple mask layers of an IC. This is used by the mask manufacturer to produce the masks.

Pin-to-Pin Delays Signal delays from the input to the output of a logic block.

PLA Programmable Logic Array. A regular memory-like structure that can perform logic.

Planar A process invented by Bob Noyce at Fairchild that made integrated circuits practical.

PLD Programmable-Logic Device. A logic IC whose function is programmed after manufacture.

PMOS The earliest MOS technology, subsequently replaced with the higher-performance NMOS.

Polygon IC mask tooling is made up of a series of polygons overlaid over one another.

Power Dissipation Electrical power consumption.

Programmable Logic Digital logic that can be customized after manufacture.

R-C Tree Analysis A signal delay analysis which incorporates the resistance and capacitance of interconnections.

RAM Random-Access Memory. An electronic data storage structure.

Regular Structure Portions of an IC that have a repetitive nature such as memory.

Respin Redesigning an ASIC and producing new prototypes..

Reverse Engineering Replicating the form, fit, and function of an IC or function.

RFQ Request for Quote. A customer request for price and delivery.

RISC Reduced Instruction Set Computer. A high-performance computer architecture.

Road Show A series of meetings with potential investors that takes place before an IPO.

ROM Read-Only-Memory. A semiconductor memory IC whose contents are permanently determined at the time of manufacture.

Route 128 The highway outside of Boston that is the East Coast equivalent of California's Silicon Valley.

RTL Resistor-Transistor Logic. The first integrated circuit logic family, circa mid-1960s.

Rubylith A mylar film used for mask design in the 1960s. Sturdy transparent mylar covered by a soft red film. Light areas are obtained by cutting and stripping the red portion.

Scaling Reducing device size and voltage to increase IC density and speed while reducing power dissipation.

Schematic Entry Defining an electronic circuit by the graphical interconnection of logic elements.

Schottky A high-speed bipolar process.

SCL Simulation Control Language, the alphanumeric program that controls logic simulation.

Sea of Gates A gate array without specific wiring channels. (See Channel-Free Arrays) .

SEC Securities and Exchange Commission.

Silicon Gate MOS A more advanced MOS process developed in the late sixties to allow higher densities and speeds.

Silicon Valley The southern section of the San Francisco Bay Area, and the center of semiconductor activity in the United States.

Simulation The use of computer modeling to determine the operation of a system.

Single Board Computer Intel's name for a computer on a small board.

SPICE A circuit simulator that operates at the transistor level developed by the University of California at Berkeley.

SRAM Static Random Access Memory. A memory IC that does not require data regeneration.

SSI Small-Scale Integration. Early ICs containing only a few logic elements.

Standard Cell A method of designing ICs by interconnecting predesigned, optimized logic elements.

STL A bipolar process used by Texas Instruments in the early eighties.

TEGAS A logic simulator circa 1980.

Test-Fault Coverage A measure of the completeness of an IC production test.

Test Synthesis Computer generation of IC production test patterns.

The Shoe The option reserved by investment bankers in an Initial Public Offering to sell an additional ten percent of shares.

TI Texas Instruments. A multinational electronics and litigation corporation based in Dallas.

Top-Down Design Electronic design done from the functional level.

TTL Transistor-Transistor logic. A bipolar logic family that replaced RTL and DTL. TTL was dominated by Texas Instruments.

Two-Layer Metal The interconnection of an IC using a two-layer matrix of metal interconnection similar to a two-sided printed circuit board.

Tymeshare A computer service company that sold time on its mainframe computers.

Venture Capitalist Individuals or groups who invest in new companies.

Verilog A logic simulator provided by Cadence.

VHDL A high-level, alphanumeric description of an electronic system or chip.

VLSI Very Large-Scale Integration. An integrated circuit of at least 10,000 gates on a single chip. Acronym for VLSI Technology Inc.

WESCON An electronics show held yearly on the West Coast in Los Angeles or San Francisco.

Yield The percent of ICs on a wafer that are manufactured free of defects.

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QUOTES FROM SILICON DESTINY

"At the risk of strengthening my competition, I believe America must get its act together in manufacturing. These "fabless" chip companies may look good for a while, but ultimately their lack of manufacturing capability will prove fatal. Americans don't seem to realize the problems we face in Japan, for example too few people and a very expensive infrastructure compared to the United States. You can be very competitive if you choose."

Tsuyoshi Kawanishi, Senior Executive VP, Toshiba Corporation

"When we were trying to finance VLSI, the venture capitalists turned us down so many times, I felt like a Hollywood starlet going to audition and hearing, "You're too tall and you've got no boobs. Get out of town."

Jack Balleto, Venture Capitalist

"We found that Japan is an entrepreneur's paradise in that they have minimal business tax and very close to zero capital gains tax. A Japanese businessman can't earn enough salary to get rich, but if he can somehow get a piece of a start-up company, he won't pay any tax on the capital gains."

Wilf Corrigan, Chairman and CEO, LSI Logic Corporation

"Jim Soloman wanted to put together a CAE start-up. He ended up getting National, Harris, and GE as industrial sponsors to invest in the company and then he got some venture guys to back him up. Jim left National in mid-1982 to found SDA. We all thought he was crazy. We gave him a going- away party, and after a few beers, someone asked, "What's with Jim? He's a bright guy. National loved him. He could have had any job in the company." We at National thought that design automation guys were the ultimate pits, so we laughed and joked when he took off, and we never understood his vision."

Joe Costello, President, Cadence Design Systems

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