MICROCOMPUTER SYSTEMS: A SURVEY

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ABSTRACT

Recent progress in metal-oxide semiconductor (MOS) large-scale integration (LSI) technology has yielded a new type of component, the microcomputer, or "computer-on-a-chip". Its impact is already proving to be spectacular.

The term of microprocessor has been heretofore reserved for microprogrammable processors. A new meaning has been introduced, and is now widely accepted: the word "microprocessor" designates here an MOS-LSI processor equipped with CPU-like functions. "Micro" is then a reference to the size. This does not refer to the control philosophy used in the processor design: a microprocessor is not necessarily microprogrammed. Other LSI processors, equipped with only minimal arithmetic functions (4 to 8 functions) are designated as calculators.

The main characteristic of an LSI MOS "chip" (silicon semiconductor die) is to achieve very high interconnect and logic density in a minute volume. Recent memories implement a 4K bit RAM in a single chip. The resulting advantages are economy and performance: low cost, size, weight, and power consumption, high reliability, logic complexity, and speed. The principal limitation is in speed which is currently lower than bipolar.

Microprocessors represent a natural evolution from calculator chips, and were first introduced by Intel in 1971. Most major companies are now in the process of producing microprocessor systems.

After an overview of MOS LSI technology, possible microprocessor organizations are analyzed. The main microprocessors currently available, or due to be introduced, are presented. Finally, applications of microcomputer systems are surveyed, and their impact is evaluated.

MOS LSI TECHNOLOGY

HISTORICAL EVOLUTION

The concept of the MOS field-effect transistor (FET) can be traced as early as the 1930's, prior to the bipolar transistor. The difficulties of the manufacturing process hampered development efforts. Development of the silicon planar process in the early 1960's made it possible to start developing MOS FET's. The first simple integrated circuits (IC's) were only produced in 1964, ten years after production of the conventional silicon transistors. It was until 1967 when MOS IC's started being produced by a sufficiently well controlled process to produce reasonable yields.

SEVERAL TECHNOLOGIES

MOS manufacturing technologies can be briefly summarized as follows:

1. p-channel : holes are the vehicle of current flow. It is inexpensive, easy to manufacture. High yield, high threshold voltage, relatively slow, reliable, limited LSI packing density. Typical access time for a p-channel memory is 300 ns.
2. n-channel : electrons provide the vehicle for current flow. Complex control of manufacturing process makes this very recent technology a difficult one. Low threshold and operating voltage. Due to higher electron mobility, n-channel is typically two to three times faster than p-channel. Higher packing densities have led to the recent introduction of 4K RAMs and to several announcements of microprocessors, to be introduced soon.
3. CMOS : from a manufacturing standpoint, it combines the n- and p-channel processes: expensive, low capacity But faster than

p-channel and cheaper than bipolar. Very high noise immunity and insensitivity to power supply voltage. However, less dense than n-MOS and difficult manufacturing.

4. SOS — Silicon-on-Sapphire (SOS): this new technology provides best speed prospects with relatively high packing density.

5. Special — Special Process Factors: Ion Implantation provides precise impurity and doping control. Relatively expensive, but reduces threshold and eliminates overlap capacitance.
Metal-Gate (Aluminum): introduces overlap capacitance, resulting in lower speed.
Silicon-Gate: reduces threshold and capacitance.

THE ADVANTAGES OF LSI

LSI devices offer two basic advantages: economy and system performance. In particular, LSI requires fewer packages, lower power supply, lower cooling requirements. As a result, fewer PC cards and connectors are needed, higher performance is obtained at the same cost, better reliability and maintainability are achieved.

The major limitations of LSI are essentially three:

1. economic: development cost, and cost of modifying a chip.
2. technological: slower speed than bipolar.
3. management: long lead-time and standard versus custom logic.

The major impact of MOS LSI is in reducing the cost per-logic-function so drastically that it is no longer a significant parameter. Computing and logic functions become essentially free compared to other costs. The cost of the whole microprocessor itself is typically a small fraction of the total system cost.

THE LSI MICROPROCESSOR

MOS became a reality in 1967/1968. The gate count per chip started to increase steadily: small-scale integration (SSI), medium-scale integration (MSI) (over 2000 transistors per chip), LSI (over 5000).

The basic problem in LSI technology was to design standard products. In fact, standardization started only two years ago. First with receiver-transmitters (UART's), then calculator chips (in mid'72), large arrays, and now microprocessors. At the same time, a large number of generalized arrays are being introduced: memories, sync generators, digital voltmeters.

The majority of such microprocessors is probably still custom-designed. The increasing availability of standard microprocessors may reverse this trend in the domain of processor chips.

MICROCOMPUTER ARCHITECTURES

MICROPROGRAMMED OR HARDWIRED

It has been explained above that a microprocessor need not be microprogrammed. The control section of a microprocessor may be either hardwired (low cost) or microprogrammed (flexibility). Both organizations have merits which make them valuable for specific applications.

Historically, microprocessors were introduced as modified calculator designs, i.e., were 4 bit wide and had a hardwired instruction set.

A competing philosophy appeared with 2-chip processors: they use a RALU and a CROM. The RALU is a register-equipped arithmetic logical unit (ALU). The CROM is a read only memory (ROM) for RALU control. The chip count may be increased as one CROM controls several RALU's or several CROM's control one RALU. The flexibility gained with a programmable control chip is beneficial for expanded or varying instruction sets as well as microcoded control algorithms.

This microprogramming facility may present disadvantages: increased engineering, development time for instruction set, cost penalty.

THE BIT WIDTH

The first microprocessors, derived from the calculators, were 4-bit wide. With improving technology, 4, 8 and 12-bit microprocessors have been realized. The quasi-universal width is now 8 bits, an optimum in view of current pin count limitations (40 pins) and of component standardization. Often, ALU chips may be used in parallel, like memory chips, resulting in modular 12, 16 or 24-bit systems based on 4 bit or 8 bit chips.

THE CHIP COUNT

Although a microprocessor resides on a small number of chips (one to three), the complete microcomputer system requires many more. Typically, a complete system will require 14 to 50 IC's, with clocks and timing, control logic, plus peripheral interface IC's (5 to 30 IC's). The total number of IC's is 19 to 80. New architectures seek to minimize the chip count by incorporating more functions within a chip: control, timing, buffering.

THE INTERNAL REGISTERS

As packing densities have increased, it has become possible to supply an increasing number of internal registers. From the user's standpoint the two essential functions are working registers and subroutine address stack. Typically, a microprocessor will now include 8 to 16 internal working registers (8 bit). The cost of providing more registers is not so much a hardware cost as a loss of address bits internally, for register selection.

It will also include a facility for subroutine nesting, the stack. Two philosophies compete: an internal set of hardware registers, or a pointer to memory.

An internal set of 8 to 16 registers offers a speed advantage in stacking operations (fast interrupt response). The disadvantages are a loss of flexibility (the number of levels is limited to the number of registers) and a significant increase in complexity.

The second approach uses a program counter and a stack pointer (plus perhaps a stack base). It allows an unlimited number of return address nestings, but is slower than the internal register approach. The gain in flexibility tends to favorize this design philosophy in the most recent microprocessors.

EXISTING MICROPROCESSORS

INTEL : MCS 8008

In addition to its four-bit MCS-4 microprocessor, Intel offers an eight-bit processor, the MCS-8. Its complexity is equivalent to 125 TTL packs.

The microprocessor chip incorporates:

1. an eight-bit parallel arithmetic unit
2. seven eight-bit data registers
3. eight forteen-bit registers (stack) for subroutine nesting.
4. instruction decoding and control logic (this is a hardwired processor). Interrupt capability. 48 instructions.

Typical macro-instruction time is 20 us for the 8008, 12.5 us for the 8008-1. Memory is ROM, PROM, RAM or shift registers, up to 16 K by 8-bit words. Addressing is implicit: a register must be loaded. This microprocessor uses an 18-pin package. It offers extensive software and prototyping support.

INTEL 8080

This is an n-channel silicon-gate, 40-pin microprocessor, due to be introduced shortly. Its design is analogous to the 8008. The CPU contains:

1. 8-bit parallel binary ALU
2. seven 8-bit data registers four testable flag bits
3. hardwired control. Externally TTL compatible
4. one 16-bit stack pointer and a 16-bit program counter.

Non memory referencing instructions are executed in 2 microseconds (2MHz clock).

In this processor, the address is 16-bit wide, and the stack is in external memory (unlimited). The microprocessor only contains a stack pointer. Upon interruption, the program-counter plus the data registers, the accumulator, and the flags, can be stacked.

Another difference lies in the bussing: the 8080 does not time-multiplex data and address over a single bus anymore. The 16 bit-address provides a 64 K-8 bit memory addressing capability without an external memory register.

The 74 instructions include the 48 instructions of the 8008 (compatibility). The packaging is 40-pin DIP.

NATIONAL SEMICONDUCTOR : IMP 16 C

National Semiconductor (NS) uses a building block approach for its systems, the IMP 16 C (16 bits) and the IMP 8 C (8 bits). They are built around microprogrammable four-bit processor modules. The IMP 16 C uses four RALU's and a CROM to form a 16-bit system.

Each RALU has:

1. seven internal registers: four general purpose, including one as index plus three for the microcode (PC, MAR, MDR)
2. 16-word stack (4 bits)
3. 4 status flags
4. 4-bit wide ALU (ADD, AND, OR, EOR and shift).

The CROM provides the control logic for up to eight RALU's. It stores the microprogram and offers a standard instruction set of 43 instructions. The ROM stores 100 23-bit microinstructions.

A typical macroinstruction requires 7 us.

The clock cycle of 1.5 us is divided in four phases. The commands specified between the RALU and the CROM are:

1. A-source register
2. B-source register
3. ALU operation select
4. R-address register.

The pin count is 24 for RALU and CROM.

FAIRCHILD : PPS 25

This is a four-bit processor intended for scientific calculations. It belongs to the family of processors directly derived from calculator chips. It uses a multichip approach: a 3805 arithmetic unit, a 3806 programmed function and timing unit, a 3810 ROM for microprograms, a 3808 for memory.

Its organization is 25-digit serial, 4-bit parallel, with a 62.5 us word time, 2.5 us bit time (addition of two 25 digit numbers in 62.5 us, multiplication in 50 ms). Each ROM stores 256 microinstructions. Up to 26 ROM chips may be used in one system. The memory chip stores digits, each 4 bits binary-coded (BCD). There are 3 25-digit registers per chip.

Its characteristics are :

. one 25-digit register
. 4 bits per digit
. BCD serial/parallel: 25 digit serial, 4 bit parallel
. 95 instructions
. bit time is 2.5 us, word time is 62.5 us (25 digits + 25 digits)
. 4 level subroutine stack
. external interrupt
. 1 to 7 25-digit memory registers
. 1 to 26 ROMS : 256 x 12 bits.

TOSHIBA TLCS 12

Toshiba's microprocessor is 12-bit wide and incorporates the control ROM within the microprocessor chip.

Its main characteristics are :

. 12 bit ALU with fast-carry logic
. 5 working registers
. 8 12-bit general-purpose registers (7 available to the user, plus program status word).

A minimum system configuration necessitates the microprocessor, three memories, and one memory control unit.

Microinstructions are 29 bits wide. The system accomodates up to 128 microinstructions.

The packaging is 42-pin DIP, logic density is claimed to be equivalent to 11000 p-channel MOS transistors (silicon-gate technology).

ROCKWELL MICROELECTRONICS : 10660

This is a fast four-bit parallel processor (5 us) with 50 wired instructions. It uses ROMs, RAMs, and 10 chips. They are 42-lead flat packs.

Subroutine nesting is performed in RAM. The address bus is 12-bit wide. Two decimal digits are added in 30 us.

COMPUTER AUTOMATION : NAKED MINI

Computer Automation developed a seven-chip MOS/LSI processor to build a basic 16 bit-system. It uses four RALU's and three control-chips with Programmable Logic Arrays (PLA's) rather than ROMs. All bussing is 16-bit wide.

The newly developed LSI-2 processor replaces the LSI-1, is faster, and compatible.

GENERAL AUTOMATION : LSI-12/16

The former SPC-12 processor board is replaced by a single chip. It uses LSI, n-channel SOS technology. It offers high-speed of n-channel SOS and high density (2000 gates or 4000 to 5000 transistors). The basic board accomodates the microprocessor system with up to 2 K of memory, operator console and system operation features.

It features complex memory addressing of up to 4 K words (12 bit address).

For microprogramming flexibility, this system uses a "ROM patch" technique with two ROM boards. One holds 32 patch addresses, the other holds the 32 patches. The system is structured in 12 bit-parallel for addresses, 8-bit parallel for data. Fifty-two basic instructions are offered. Basic instruction cycle is 2.6 us.

FORTHCOMING MICROPROCESSORS

AMERICAN MICROSYSTEMS INC (AMI) : 7300

The system is described for its architectural interest. It has been announced recently that it will not be implemented.

This microprogrammed 2-chip processor is parallel, 8-bit. It uses a RALU plus CROM philosophy. Both chips are p-channel, silicon-gate, ion-implanted. The RALU contains :

1. ALU with A and B-source registers, status register, result register
2. thirty-two general registers which can be used as either one or two stacks and or one or two register sets
3. seven-address stack.

The control ROM is called Microinstruction ROM or MIR. It is a 512-word by 22-bit mask programmable ROM. The instruction cycle is 4 us. There is a four-level interrupt system.

SIGNETICS

Signetics plans the introduction of an 8-bit fixed instruction processor with extensive addressing capabilities: direct, indirect, relative, absolute, immediate. It will be an n-channel silicon-gate processor. Instruction time is 5 to 10 us. The ALU contains 4 general registers, an eight-register stack, and implements 75 instructions. The address bus is 15-bit wide. instructions are structured in a 6-bit opcode and 2-bit register pointer. It uses a 40-pin package. Introduction planned for 1974.

OTHERS

Monolithic Memories and Raytheon have announced a bipolar microprocessor. Raytheon's is a seven-chip system, with 3 CROMs and 4 RALUs to produce a 16 bit system. Due to the bipolar technology, the expected speed is 200 ns.

Siemens has announced development plans for an MOS n-channel 8 bit-microprocessor analogous to the Intel 8080. Texas Instruments, American Microsystems, and Microsystems International are said to be considering licensing agreements for second-sourcing the 8080.

Inselek has announced plans for a CMOS, SOS microprocessor with a 300 ns cycle time.

RCA has announced a 2-chip CMOS 8 bit microprocessor using a 16 x 16 scratchpad for memory accesses.

Western Digital and other manufacturers are announcing plans for new microprocessors. In view of the long lead-time for development, it is likely that only a few more will be effectively introduced this year.

APPLICATIONS OF MICROCOMPUTERS

GENERAL RULES

Originally intended for desk-calculator usage, microcomputer systems are now being used in an increasing range of applications.

The general rules for using a microprocessor instead of a hardwired device can be summarized as follows:

1. sequential digital application requiring over 50 hardwired IC's
2. non-trivial program sequence
3. logical or arithmetic requirement
4. no super-speed, although multiple microprocessors may be used.

APPLICATIONS

Microprocessors are used in the following applications:

- Small business machines, including calculators
- Point of Sale Terminals (cash registers, credit card verifiers)
- Data Communication (communications preprocessor, smart terminal, test equipment, data concentrator, message switching, signal processor)
- Peripherals Controllers (card reader, floppy disc, cassette tape unit, line printers, CRT)
- General Control (machine tool, process control, environment control for building, traffic control, elevator control, appliances, automobiles)
- Data Acquisition Systems
- Instrumentation and device tester
- Programmed games.

THE IMPACT OF MICROCOMPUTERS

The impact of the microprocessor can be expected to be more significant than the mini revolution a few years ago. The range of microcomputer systems extends throughout a wide spectrum of performance and cost, from the calculator at the low end, to the minicomputer at the high end. Typical execution times for microcomputers are still 2 to 10 times slower than those for minis, but are constantly shrinking. Microprocessors have evolved as standard OEM products, and cater exclusively to the OEM users, while minicomputers usually provide extensive support geared to the end-user. Their major impact is felt on economical and "smart" OEM digital products. As MOS LSI costs keep decreasing, the number of microcomputers should exceed by far the number of any other type of computer being produced.

REFERENCES

1. C.G. Bell and al, "The Architecture and Applications of Computer Modules: A Set of Components for Digital Design", COMPCON 73, March 1973, pp. 177-180.
2. S. Davis, "A Fresh View of Mini-and Microcomputers", Computer Design, May 1974, pp. 67-79.
3. C.C. Foster, "A View of Computer Architecture", CACM July 1972, Vol. 15, number 7, pp. 557-565
4. S. Fuller and D. Siewiorek, "Some Observations on Semiconductor Technology and the Architecture of Large Digital Modules", Computer, Oct 1973, pp. 15-19
5. M.E. Hoff, Jr, "Applications for Microcomputers in Instrumentation", 1973 IEEE Intercon.
6. R. Holt, M. Lemas, "Current Microcomputer Architecture", Computer Design, February 1974, pp. 65-73.
7. G. Lapidus, "MOS/LSI Launches the Low Cost Processor", Spectrum, Nov 1972, pp. 33-40.
8. G. Reyling, Jr, "LSI Building Blocks for Parallel Digital Processors", 1973 IEEE Intercon.
9. T. Tarui, and al, "Twelve-bit microprocessor nears minicomputer's performance level", Electronics, March 1974, pp. 111-116.
10. J. Weisbecker, "A Simplified Microcomputer Architecture", Computer, March 1974, pp. 41-47.
11. W. Wickes, "A Compatible MOS/LSI Microprocessor Device Family", Computer Design, July 73, pp.75-81.