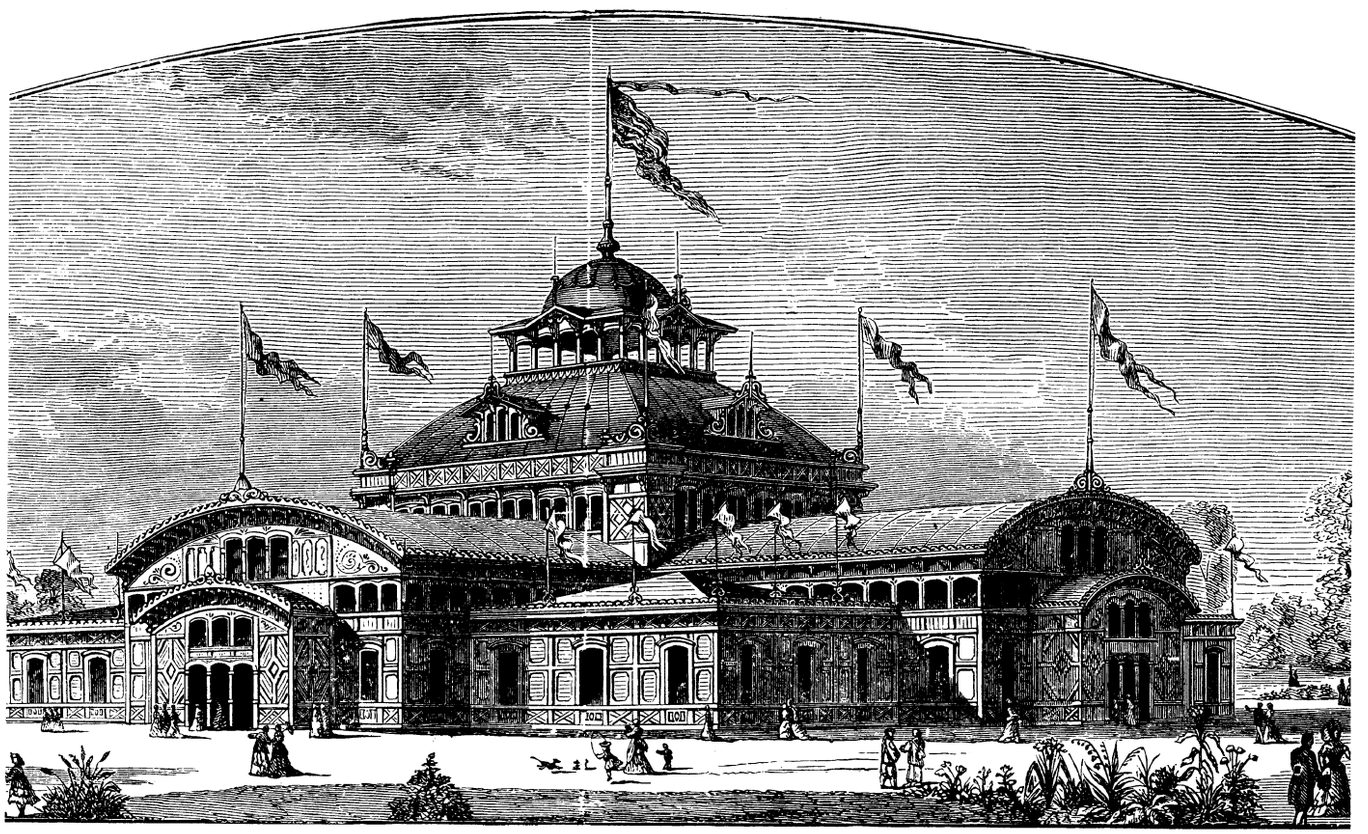


New Products

FEATURING MEMORY TECHNOLOGY

With this issue, the New Product emphasis is structured toward providing an understanding of technological developments, as well as providing the traditional source of product information pertinent to the system developer.

As evidenced by the New Product announcements, semiconductor technology has moved out of the laboratory and into the commercial market place. The improvement in price/performance characteristics should provide additional stimulus in developing systems which provide the broader consumer base needed by the electronics industry.

—Cecil Frost
New Products Editor

Associative Memory Chip

Fairchild Semiconductor has introduced the MμL4102, a bipolar integrated circuit associative memory that combines logic circuits and memory cells on the same silicon chip. The MμL4102 is designed to signal a match whenever data at its inputs correspond to data already stored. Each match output indicates a comparison between four input lines and four corresponding bits in a read/write contents addressable memory. Featuring a 35-nanosecond maximum match time, this high complexity TTL product allows computer designers to achieve high system speeds for repetitive information while still making use of a slower main core memory. It provides a low-cost method of increasing the speed of data processing similar to its use in the "Cache system" used by IBM's 360/85. In this application, the Mμ4102 is connected directly with the 9035 semiconductor random access memory to reduce total access time to 70 ns.

The 4102 is organized into four 4-bit words, each with its own address line. When a word is addressed, the contents appear on four output lines. A bit masking feature is available. The device has a write enable capability that provides non-destructive readouts. Uncommitted collector outputs make it possible to achieve bit expansion and word expansion. Packaged as a Dual-In-Line unit with 24 pins, the MμL4102 costs only $50 in quantities of 100 to 999. The price is $75 at 1-24 quantities and $60 at 25-99 quantities.

CIRCLE 22 ON READER SERVICE CARD

"Circuit-Stik" Packaging

CIRCUIK-STIK, the new concept in electronic packaging offers cost savings and flexibility not found in previous prototype packaging systems.

Engineers at CIRCUIT-STIK, INC. have developed a complete family of circuit sub-elements and circuit materials designed as a total packaging system. A wide variety of items have been selected for presentation in a prototype kit. The kit has been designed to allow "INSTANT" fabrication of several circuit boards as well as provide serious evaluation of the "CIRCUIT-STIK CONCEPT."

This system reduces design and drafting expenses and saves weeks of valuable schedule time normally lost to outside manufacturing services. Individual circuit boards can now be assembled and tested directly from engineering sketches, schematics and logic flow diagrams the same day.

CIRCUIT-STIK sub-elements are available in a wide variety of patterns for all commonly used electronic components including "flat-pack," "dual-in-line," and "TO-5" packaged integrated circuits, transistors, diodes, resistors, test point jacks and plug-in printed circuit connectors. Also included are pressure sensitive copper tapes, donut pads and ground planes, plain and pre-punched epoxy-glass boards, and plug-in connectors.

The Prototype Kit, Part No. 8951, contains a total of one hundred eighty parts — enough to mount over four hundred components and fabricate many instant circuit boards. The kit #8951 contains $110.00 worth of parts when purchased individually and sells for $89.50.

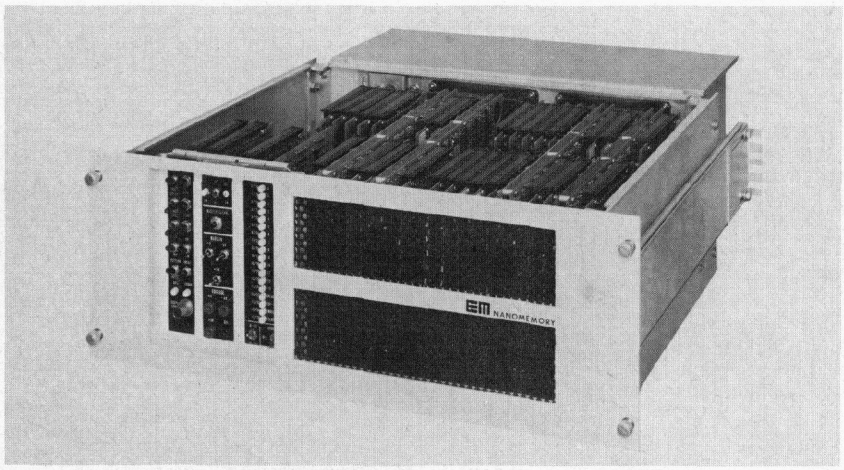
CIRCLE 32 ON READER SERVICE CARD

Core Memory System

Information Control Corp. has announced the Model ComRac 1100 mainframe core memory system. Cycle time is 900 nanoseconds and access time is 350 nanoseconds. All 1100s are delivered completely wired for full 16K x 18 capacity. The full 16K x 18 system requires only 5¼" of rack space, complete with power supply. Operating margins are guaranteed to be ±5% over the temperature range of 0-50°C. An unusual feature of the 1100 is its ±5% margin switch, which is easily accessible from the front panel.

Standard features include half cycle operation which allows the system to either read or write only at 600 nanosecond cycle times, and byte control, which permits selection of either the upper or lower 9 bits. MTTR for the system is under 10 minutes when spare cards and stacks are available. MTBF is greater than 10,000 hours. Operating temperature is 0°C to plug 50°C. Input power is 117 VAC ±10%, 47-400 Hz. Options for the 1100 include a built-in memory exercisor for completely testing the memory at 900 nanoseconds, field expansion kit, Read/Modify/Write mode, Buffer Read, Buffer Write, Data Guard and Zone Control. Price is less than $10,000 for an 8K x 18 with tester and power supply. Delivery is from stock.

CIRCLE 25 ON READER SERVICE CARD



Fast Core Memory System

Do-it-yourself Electronic Calculator

Electronic Arrays has developed the EAS100, a set of MOS LSI circuits for a 16 digit calculator with 8 digit display capability. The calculator set consists of six circuits, each contained in a 24 pin dual-in-line package. These circuits accomplish the complete electronic portion of the calculator exclusive of the display. The set includes a control array which utilizes a 1920 bit ROM to issue the basic control sequences that operate the calculator. The additional circuits consist of an input array, a control logic array, a register array, an arithmetic array and an output array.

In addition to the normal arithmetic operations, the logic accommodates chained operations (continued arithmetic operations), negative sign and overflow indication and electronic interlock. Applications material is available and the six MOS LSI circuits are available for immediate delivery.

CIRCLE 24 ON READER SERVICE CARD

Fast Core Memory System

Electronic Memories has developed a core memory system with a cycle time of 500 nanoseconds and an access time of 300 nanoseconds. The new NANOMEMORY 2500 operates at the threshold of current core speed capability using proven design technology. The NANOMEMORY 2500, a medium capacity 2½D core memory, is capable of storing up to 294,912 bits in a single standard 19-inch wide rack 7 inches high and 21 inches deep. Memory configurations are available in 4096 or 9148-word configurations with word sizes ranging from 9 to 36 bits. Memories of 16,384 words or bigger are available with word sizes of 9 to 18 bits. The operating temperature range is 0 to 50 degrees centigrade. Delivery is 90 days and price range from 5 to 7 cents-per-bit depending upon the configuration.

CIRCLE 26 ON READER SERVICE CARD

LSI Minicomputers

Data General Corporation has announced a new line of three 16-bit word length minicomputers: the Nova 1200, the Nova 800, and the Supernova SC. The new minicomputers feature two major technological accomplishments: the use of large scale integrated circuitry (LSI) and the development of an all semiconductor minicomputer. All three new computers are compatible with each other and with Data General's current models, the Nova and Supernova. First deliveries on the Nova 1200, the Nova 800, and the Supernova SC are scheduled for February, April, and June respectively.

The Nova 1200, with a base price of $5450 including 4K by 16-bit word core memory, Direct Memory Access (DMA) channel, and Teletype interface, is the least expensive computer in the Data General line. At the same time, the Nova 1200, with a cycle time of 1.2 microseconds, is effectively 2½ to 3 times faster than its predecessor, the Nova, and executes arithmetic and logic instructions in 1.35 microseconds. The Nova 1200's central processor, which uses very reliable LSI circuits and a high degree of medium scale integration, is contained on a single 15-inch printed circuit board.

The Nova 800, a fully-parallel minicomputer with an 800-nanosecond cycle time, is a faster computer than the Nova 1200, and uses the same mechanical package. The Nova 800 is designed especially for use in applications with high input/output requirements; it has a built-in data channel with a high-speed capability for fast devices and a standard capability for slower devices. The Nova 800 costs $6950 including a 4096-word by 16-bit word core memory, DMA channel, and Teletype interface.

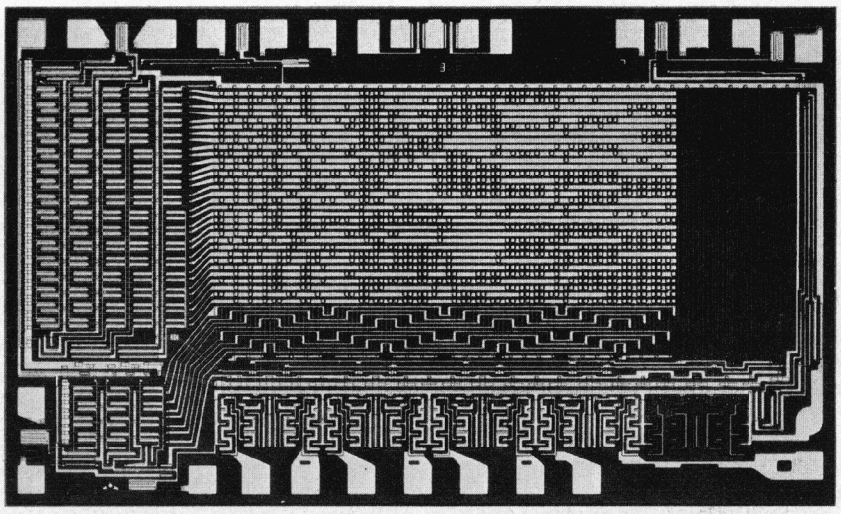
The Supernova SC is the first small computer to take full advantage of the inherent speed of semiconductor main memories and executes arithmetic and logical instructions in 300 nanoseconds. The Supernova SC central processor uses the non-destructive nature of the semiconductor memory (no re-write cycle is required as it is with core) by overlapping the instruction execution cycle with the read cycle of the next instruction. The basic configuration of the Supernova SC, with 4K by 16-bit semiconductor memory, DMA channel and Teletype interface, is $11,900.

CIRCLE 30 ON READER SERVICE CARD

Memory Options

A new line of mainframe memories available with Computer Automation, Inc. computers has been announced. The new line features read-only memories, scratch pads, and both large and small core read/write memories offering economy, high speed and building block flexibility. New options being offered include 1K, 2K and 4K core memories with a 1.5 μs cycle time, and a series of 400 ns read-only memories that can be mixed with 128 and 256 word scratch pad memories. All memory options plug into standard prewired memory slots in the computer, and can be installed in the field. No wiring changes to existing ground planes are necesary.

CIRCLE 31 ON READER SERVICE CARD



MOS Read-only Memories

MOS/LSI Computer

Four-Phase Systems, Inc. has announced its new computer display processing system, the System IV/70. Designed for data entry and retrieval to and from data bases and computer systems, System IV/70 — itself a computer — is all MOS/LSI and is one of the first computers to use an all semiconductor main frame memory. System IV/70 comprises a CPU, up to 96K bytes of memory, and up to 32 keyboards and CRT terminals. System IV/70 peripherals include a line printer, card punch and reader, disc, IBM-compatible magnetic tape, and paper tape. According to Four-Phase, System IV/70 has the computing power of an IBM 360/30. A combination of 16 $980 terminals and a 6K CPU would result in a per-terminal price of $1450. A complete 32-terminal system with a 24K CPU, disc drive, communications interface and printer would cost $1950 per terminal.

The System IV/70 Computer features 120 major instructions including variable length byte instructions, binary fixed and floating point arithmetic, translate/test, push/pull stacks, register to register, and list processing instructions. Typical instruction execution times include: character move, 2.5 μs/byte; character compare, 3.8 μs/byte; decimal add/subtract, 5.1 μs/byte; and binary add/subtract, 15.2 μs/24 bits.

The System IV/70 has an extensive I/O capability. The system can accommodate up to 8 I/O channels, and up to 64 devices per channel. Firmware initiated interrupts and up to 8 nested interrupt levels are standard. The maximum I/O rate is 265K-bytes per second.

CIRCLE 29 ON READER SERVICE CARD

MOS Read-only Memories

Intersil Memory Corporation has introduced a family of fully decoded static MOS read-only memories, with sense amplifier on chip, available for immediate delivery. The 7600 Series (IM7601, IM7602, IM7603, IM7604, IM-7605) has a typical access time of 350 nsec. These MOS ROMs have the flexibility of operating with bipolar circuits or all MOS systems. Additional features include OR- tie capability, chip enable/odd even logic capability and small power consumption below the typical value of 360mW. Wide-temperature-range commercial versions cost less than 2 cents per bit (in quantity) and military versions cost less than 3 cents per bit.

CIRCLE 23 ON READER SERVICE CARD

MOS Serial Memory

Electronic Arrays has developed the MOSTOR 100, a 1024 by 8 or 9 bit serial memory designed specifically for highly sequential memory applications. The sequential access time is 300 μsec. MOSTOR 100 also can be used as a non-synchronous random access memory in system applications where a relatively slow access time is acceptable and low cost is a requirement. Packaged on a single pc card, the memory uses the EA 1206, a 512-bit high speed dynamic MOS shift register, as the basic storage element.

Both DTL and TTL compatible, the MOSTOR 100's interface signal timing format can be used with most systems. Alternate interface formats can be provided to match special system applications.

CIRCLE 21 ON READER SERVICE CARD

Semiconductor "Drum" Memories

Advanced Memory Systems has delivered a 640,000-bit semiconductor "drum" memory system for minicomputers. System oriented, each SSU/m contains its own power supply and is as small as the minicomputers it is designed to work with. Each SSU/M contains 32K words of storage with word lengths of 8, 16, 32 or 64 bits. Random access times average 135 microseconds with a sequential access time of one microsecond.

The interface is word organized and each location is directly addressable by a 15-bit address. Address and data lines are TTL and DTL compatible. The 16-bit version requires 88 watts of power. The power is minimized by idling all semiconductor delay lines at a low pulse rate. The delay lines being addressed are cycled at the high clock rate (1 MHz). The 32K x 16-bit configuration has a 120-day delivery and costs $6,921.00 in small quantities (1.32 cents per bit).

CIRCLE 20 ON READER SERVICE CARD

Small Low-cost Buffer Memory

Honeywell Inc. has introduced a "midget" 1,000-word integrated circuit magnetic core memory system, the fifth member of its compatible ICM series. Measuring about 9 inches by 4 inches by 1 inch, the ICM-100 is organized in 8-, 9- and 10-bit formats to handle various combinations of read, write, restore, modify and clear functions in minicomputer-based random-access systems. It operates at a 1-microsecond full cycle time with an access time of 310 nanoseconds. Data also may be destructively read out of memory at 500 nanosecond rates. The ICM-100 uses a four-wire, 3D, coincident current magnetic core array. All logic, addressing, data buffering, control, selection, switching and sensing functions are performed by monolithic integrated circuits. It is compatible with all diode-transistor and transistor-to-transistor logic (DTL/TTL).

The memory should have broad applications as a buffer in CRT, tape or disk systems and other on-line real-time data communications systems. Other functions include use in numerical control and in data acquisition systems, and with digital controllers or testing equipment involving random-access memory and other peripheral equipment. The ICM-100 is priced from $595 per unit in quantities. Deliveries will begin immediately on a 30-day basis.

CIRCLE 27 ON READER SERVICE CARD

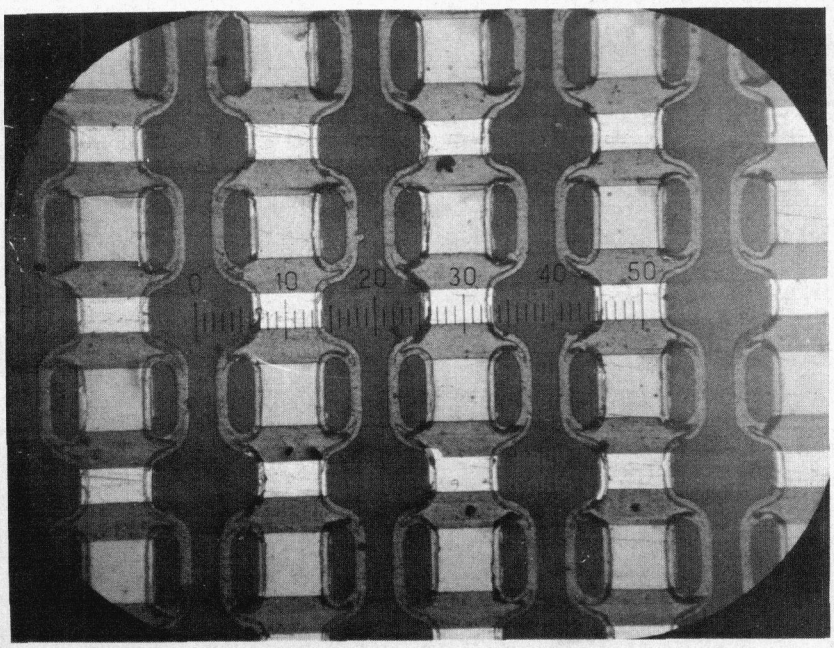
Thick-Film Memory

Signal Galaxies has announced a thick-film memory with cycle times of less than 100 nsec. The heart of the memory is a planar array of thick film elements providing storage for 8K to 32K bits with up to 16K elements in a 4″ square. Arrays will be offered with up to 64K bits in a single memory stack or array (two 32K bit arrays back to back) which, in turn, can be easily assembled into million bit memories by users. The new memories feature lower power than core, 100% bit redundancy, no deterioration of performance due to aging, low common mode noise, non-volatility and high packing densities.

Two adjacent "flux-ring" memory elements per bit are used in the new memory resulting in 100% redundancy, since although the failure of one of the two elements will cause a degraded output of that element, the remaining element will still function as a storage unit. The complementary bit structure and uniformity of the plane insures self-cancellation of common mode noise, one of the most troublesome problems in virtually every memory technique. A further advantage of the Flux Ring is "Magnetic Closure" a proprietary technique which provides non-volatility of memory bits since the elements remain locked in their magnetized state in case of power failure.

The manufacturer is currently producing 8K bit arrays (128x64) and 32-64K bit stacks for evaluation. These can be used with standard 50 mil center connectors. Since these small memories are non-volatile, faster than cores, cost competitive and can be readily modified in the field, they are ideally suited for control and micro-programming in peripheral controllers and mini-computers. Price is approximately 0.7¢ to 1¢ per delivered bit at the array level. Delivery 90 to 120 days.

CIRCLE 28 ON READER SERVICE CARD



Thick Film Memory