3800

8-BIT PARALLEL ACCUMULATOR

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3800 is a LSI-MOS integrated circuit containing approximately 200 gates. It functions as an eight bit slice of an arithmetic unit, which may be connected to form any word length. It is capable of parallel addition and subtraction, and by simultaneously shifting the sum or difference right or left, multiplication and division algorithms. A direct subtraction capability eliminates the need for the usual carry input to the LSB during subtraction, thus allowing operands to be located anywhere in the truly variable word length accumulator. The parallel data organization of the 3800 improves speed and greatly reduces the amount of random control logic when compared to the same function performed serially.

FEATURES

- **DIRECT SUBTRACTION USED TO PROVIDE VARIABLE WORD LENGTH CAPABILITY**
- **STROBED OUTPUTS FOR HARD WIRE COMMON BUS SYSTEMS**
- **DC TO 200 kHz ADD AND SHIFT RATE**
- **3.0 μs, 8 STAGE CARRY PROPAGATION TIME**
- **LOW POWER — 180 mW**

APPLICATIONS

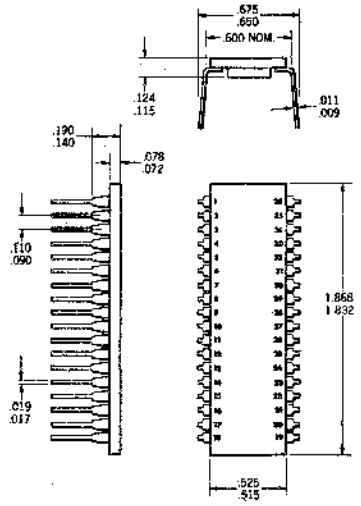
Basic Accumulator Block
Index Register
$>, =, <$ Comparator
General Logic Control
Up-Down Counter
Divide By N Counter

ABSOLUTE MAXIMUM RATINGS

Input Voltages	−30 V to +0.3 V
V_{GG} and V_{DD} Supply Lines	−30 V to +0.3 V
Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +85°C

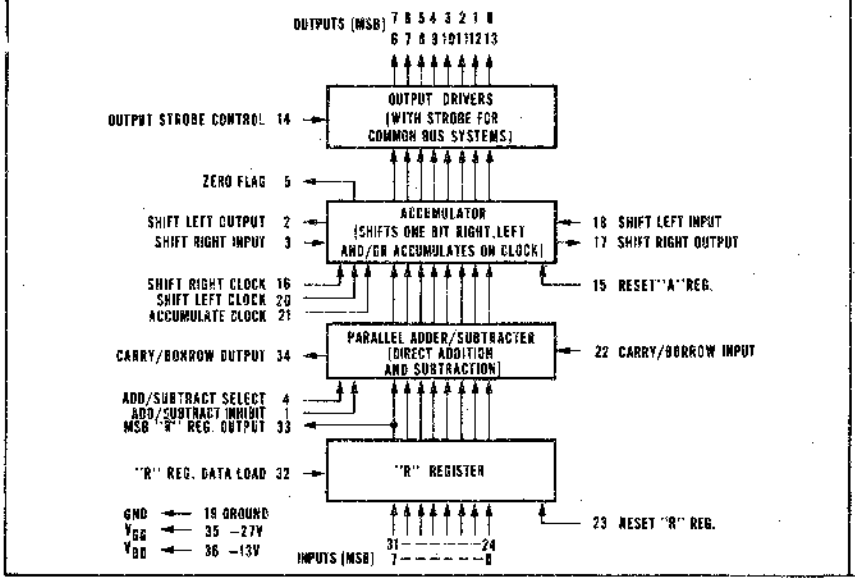
PHYSICAL DIMENSIONS

35-Pin
Dual In-Line Package

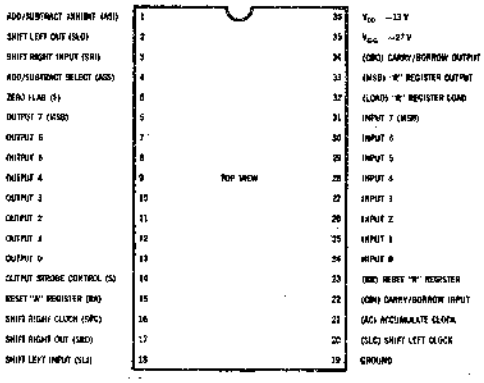


ORDER PART NO. A6H380014X (−55°C to +85°C)
A6H380019X (0°C to 70°C)

BLOCK DIAGRAM



PIN CONFIGURATION



FAIRCHILD SEMICONDUCTOR
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FAIRCHILD MOS INTEGRATED CIRCUIT 3800

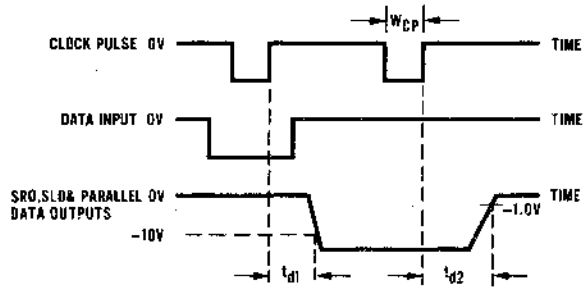
ELECTRICAL CHARACTERISTICS $V_{GG} = -27\ V \pm 1\ V$, $V_{DD} = -13\ V \pm 1\ V$, $R_L = 10\ M\Omega$, $C_L = 10\ pF$ (unless otherwise specified)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Logic inputs					
	Logic "0"	0		−2.0	Volts	$V_{GG} = -27\ V$
	Logic "1"	−10		−30	Volts	$V_{GG} = -27\ V$
	Clocks					
	Amplitude	−10		−30	Volts	
	Width	1.0		10	μs	
	Shift frequency	DC		300	kHz	
	Shift & add frequency	DC		200	kHz	
	Delay Times					
t_{CB}	8 stage carry		3.0	5.0	μs	See Figure 1
t_{d1} & t_{d2}	Output delay		1.0	3.0	μs	See Figure 1
I_{LX}	Input leakage current			5.0	μA	$V_{IN} = -20\ V$
	Logic outputs					
	Logic "0"	0	−0.5	−1.0	Volts	
	Logic "1"	−11	−12		Volts	
	Logic "1"	−10	−11		Volts	$R_L = 40\ k\Omega$
	Supply current drain					
	V_{DD}			7.0	mA	$V_{GG} = -27\ V$, $V_{DD} = -13\ V$
	V_{GG}			5.0	mA	$V_{GG} = -27\ V$, $V_{DD} = -13\ V$
	Network dissipation		180		mW	

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	Add/subtract inhibit	ASI	When ASI is a logic "1", no addition or subtraction will occur when the ACC, SRC or SLC clock are pulsed. The accumulator register will shift right or left normally however. The carry/borrow through line is not affected, allowing numbers to be shifted and compared when the subtract mode is selected.
2	Shift left output	SLO	SLO is the MSB output of the ACC and may be connected directly to the SLI input of the next eight bit section of the accumulator. Shift and add function normally.
3	Shift right input	SRI	SRI accepts the SRO output of a higher order, 8 bit slice. Shift and add function normally.
4	Add/Subtract select	ASS	When ASS is a logic "1", addition is performed, and when ASS is a logic "0", subtraction is performed.
5	Zero flag	F	The zero flag output is a logic "1" only if the accumulator register contains all zeros. This output is independent of the strobe control.
6-13	Outputs	7-0	When the strobe control STR is a logic "0", all outputs represent the contents of the accumulator register.
14	Output strobe control	STR	When STR is a logic "1", all parallel outputs, 0-7, are disconnected from the power and ground lines allowing them to float. Thus several similar outputs may be hard wired together for a common buss system.
15	Reset Accum. register	RA	When RA = logic "1", the accumulator is reset to zero. This asynchronous signal overrides all others.
16	Shift right clock	SRC	Pulsing the SRC with a logic "1" shifts the contents of the accumulator one bit position to the right. If the add/subtract controls are enabled, the sum or difference of the accumulator register and the "R" register is shifted one bit to the right and written into the accumulator.
17	Shift right output	SRO	SRO is the LSB end of the 8 bit accumulator and may be connected directly to the SRI of an adjacent 8 bit slice.
18	Shift left input	SLI	The SLI accepts the SLO output from a lower order, 8 bit slice.
19	Ground	GND	Circuit common and substrate ground are both connected to this pin.
20	Shift left clock	SLC	Pulsing the SLC with a logic "1" shifts the contents of the accumulator one bit position to the left. If the add/subtract controls are enabled, the sum or difference of the accumulator and the "R" register is shifted one bit to the right and written into the accumulator.
21	Accumulate clock	AC	Pulsing the AC input adds the contents of the accumulator and the "R" register if ASS = logic "1". The "R" register is subtracted from the accumulator if ASS = "0". If ASI = "1", no action occurs.
22	Carry/borrow input	CBI	A logic "1" on CBI enters a carry or borrow into the LSB position of the add/subtract logic.
23	Reset "R" register	RR	Placing a logic "1" on RR asynchronously resets the "R" register.
24-31	Inputs	0-7	Inputs are entered into the "R" register asynchronously when RL is activated.
32	"R" register data load	RL	When RL is a logic "1", data presented at the inputs are loaded into the "R" register. RL may be permanently a logic "1", effectively bypassing the R register during normal operation. Note that RR overrides the data inputs regardless of the load command.
33	MSB "R" register output	MSB	It shows the MSB of the "R" register. When the "R" register is used to temporarily hold operands during multiply, divide, etc., the MSB output indicates the sign of the stored operand.
34	Carry/borrow output	CBO	The CBO is the asynchronous carry or borrow output from the MSB of the add/subtract logic. It is not affected by the ASI control.
35	V_{GG} power supply	V_{GG}	−27 V supply.
36	V_{DD} power supply	V_{DD}	−13 V supply.

SHIFT COMMAND TIMING DIAGRAM



CARRY/BORROW 8 STAGE PROPAGATION TIME

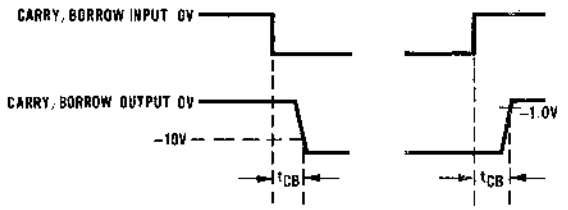
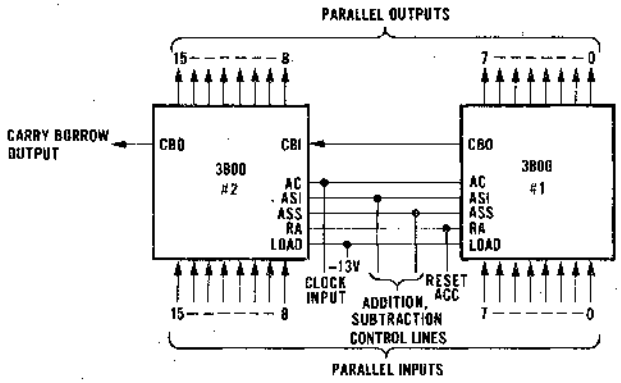


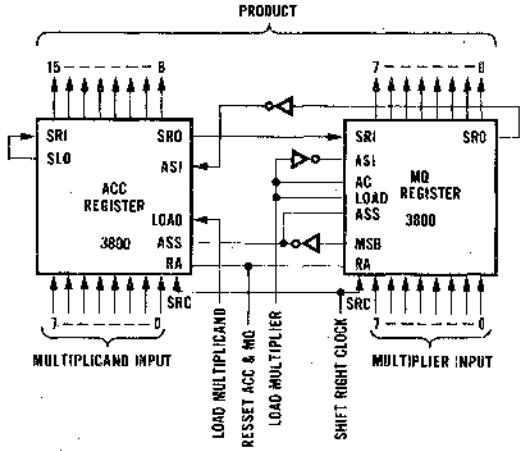
FIGURE 1

STANDARD CONNECTIONS FOR ADDITION AND SUBTRACTION



SIXTEEN BIT PARALLEL ADDITION (SUBTRACTION)*: The addition (subtraction) operation begins by resetting the accumulator, then transferring the augend (subtrahend) through the "R" register into the accumulator by pulsing the AC clock line. The operation is completed by loading the addend (minuend) into or through the "R" register, then adding (or subtracting if ASS = logic "0") it from the accumulator by again pulsing the AC clock. Multiple addition and subtraction or combinations of both operations may be performed by repeating the last operation. Thus a running total may be kept in the accumulator.

STANDARD CONNECTIONS FOR MULTIPLICATION

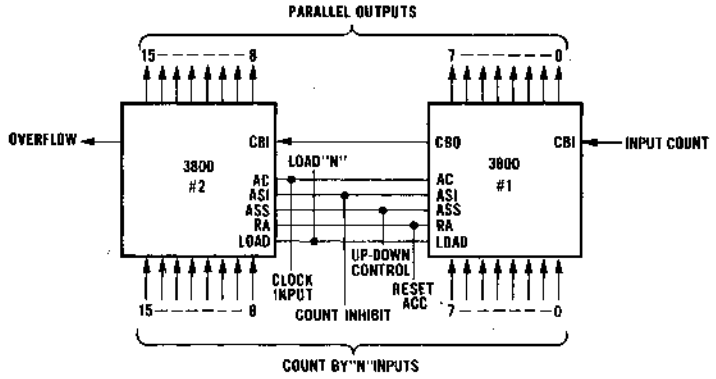


MULTIPLICATION: The multiplication operation, shown above, begins by clearing the ACC and MQ registers, then loading the multiplier into the MQ "R" register. If the MSB of the MQ's "R" register is a "1", ie. the multiplier is negative, the ACC and MQ subtract lines are enabled before the multiplier is transferred into the MQ. Thus the multiplier in the MQ is always positive. However, the multiplicand, which has been loaded into the ACC "R" register for temporary storage, will be subtracted from the partial product in the ACC if the multiplier was negative. The multiplicand is added to or subtracted from the partial product and shifted one bit to the right each time the LSB of the MQ register is a "1". If it is a "0", only a shift right occurs. Neither the multiplicand nor the resulting product require any further sign corrections as the answers will automatically be in two's complement.

DIVISION: The division algorithm is similar to the multiply and is described in detail in The Logic of Computer Arithmetic by Flores. The most straightforward way to perform division is to convert both the divisor and dividend to sign magnitude numbers the same way the multiplier was converted in multiplication. Then proceed through a successive subtraction division. The resulting positive quotient must however then be corrected to two's complement rotation if the signs of the dividend and the divisor were not the same.

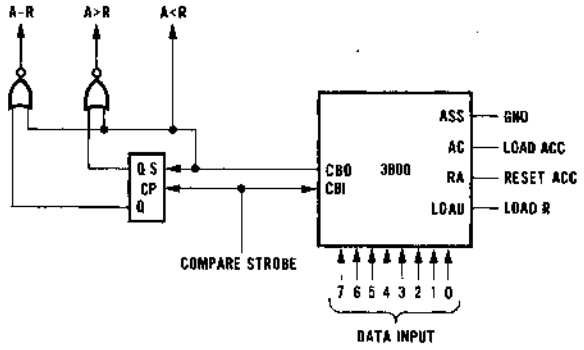
NOTES: 1. Input logic levels may be selected by referring to the list of Pin Function Descriptions.
2. All unused input or control pins should be grounded.
3. All operands are in two's complement notation.
4. All diagrams are BASIC BLOCK DIAGRAMS and no electrical levels are indicated. See Logic Diagram for correct 806B notation.

APPLICATIONS



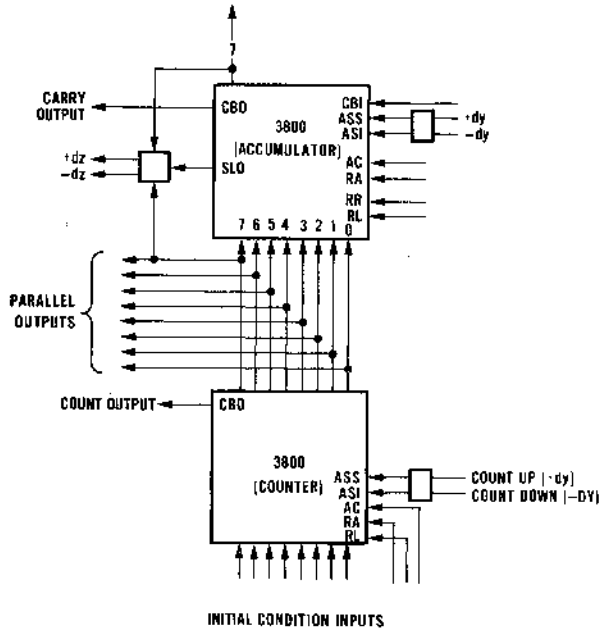
UP-DOWN COUNTER

SIXTEEN STAGE UP-DOWN COUNTER: Operation begins by resetting the registers and enabling ASS, which determines the count direction. Counting by one may be accomplished by enabling CBI or INPUT "0". To count by n, set n into the "R" register.



L, = > COMPARATOR

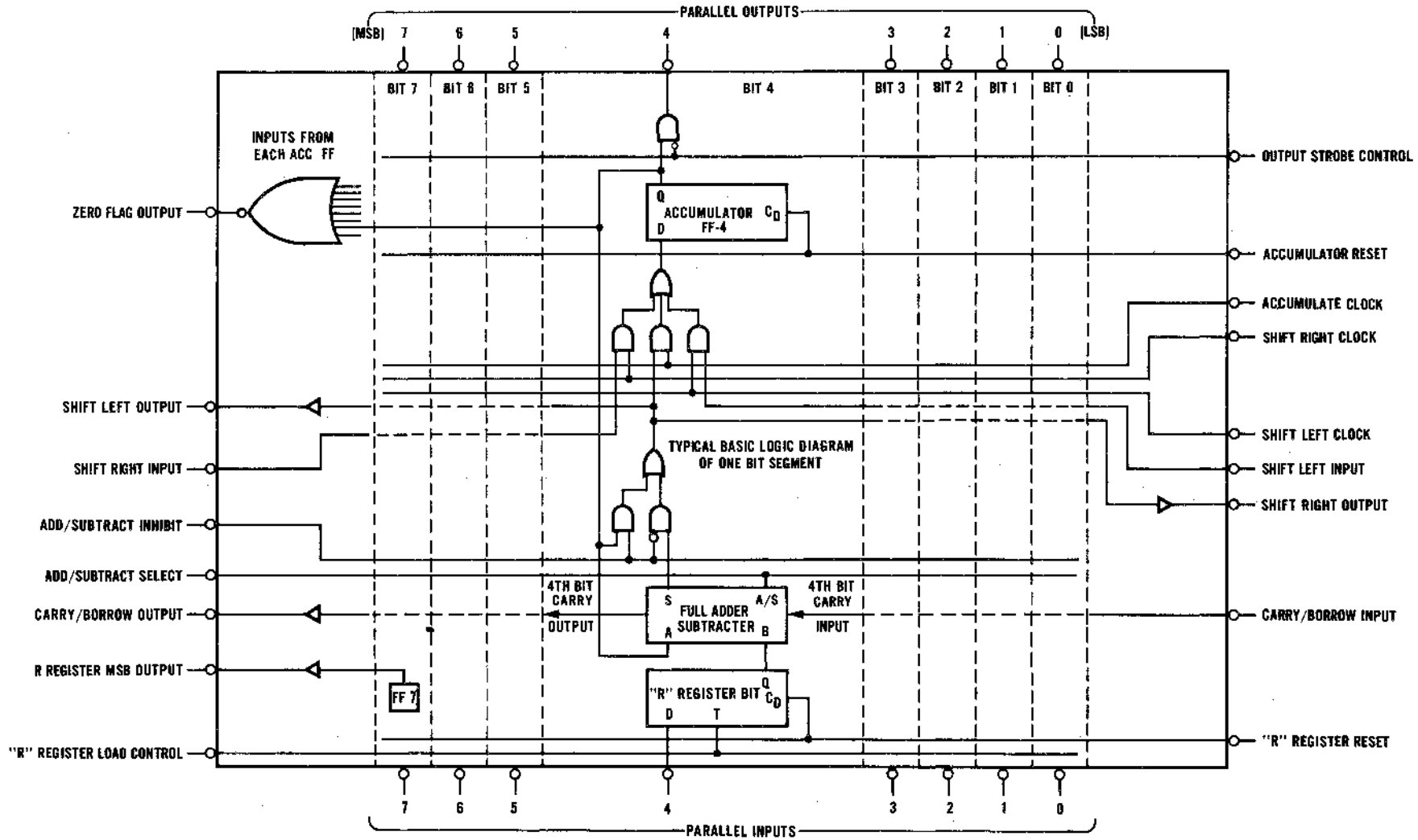
COMPARE OPERATION: To compare two numbers, simply insert the first into a previously cleared accumulator by pulsing AC. Enabling the subtract control will immediately indicate whether R>A, as a borrow output will appear. If the borrow output follows a pulse on the borrow input, the numbers are equal. If neither, then R<A. The logic is shown above.



DDA CONNECTIONS

The DDA shown above utilizes one 3800 for a remainder register and a second 3800 for a y accumulator counter.

LOGIC BLOCK DIAGRAM



NOTE: Polarity indicators (0) external to the solid box conform to MIL-STD-806B where 0 indicates the less positive state is active. Internal to the box and in the remainder of this data sheet conventional MOS polarities are used, where HI = "1" ≈—10 V and LO = "0" ≈ Gnd.

SCHEMATIC DIAGRAM