ADVANCES IN DIGITAL WAVEFORM ANALYZERS

GAUBATZ

ADVANCES IN DIGITAL WALSH ANALYZERS

by

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SCOPE AND CONTENTS : Digital logic techniques emphasizing economical implementation as applied to Walsh function generation and a digital Walsh analyzer are considered. The Walsh function generator design presented features sequency programmability of the dual orthogonal output and the generator operates in the megahertz range with an orthogonality error measurable in nanoseconds. The generator is a central component of the digital Walsh analyzer which provides a pair of Walsh coefficients after only two cycles of an unknown periodic waveform. All analyzer functions, including timing, sample processing, and Walsh function generation are provided complete in only seventy integrated circuit modules.

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ABSTRACT

The application of digital logic techniques to Walsh Spectral Analysis is considered. Specific advances are achieved in the areas of Walsh function generation and spectral analyzer arithmetic processing.

The Walsh function generator features a dual orthogonal output whose sequency is determined by a fully-decoded 6-bit parallel binary input. The sequency programmability feature is economically implemented by two Binary Rate Multipliers and a 6-bit parallel full adder. The rate multiplier outputs become toggle logic functions which are fed to synchronously clocked T-type flip-flops. The resultant Walsh waves exhibit an orthogonality error on the order of nanoseconds due only to the difference in switching times between the two flip-flops. The complete Walsh function generator implementation to a maximum sequency of 63 requires only 7 integrated circuits. The generator design is inherently flexible and may be adapted to very high speed or to low power applications and also to Walsh array generation.

The Walsh Spectral Analyzer design presented is also economically implemented with Medium Scale Integration digital logic circuits. Digitized samples of the periodic analogue input waveform are provided by an Input Sampling System composed of an analogue-to-digital converter preceded by low-pass filters and a sample-hold module. The low-pass filters assure accordance with the Sampling Principle for input signals of unknown bandwidth, and the sample-hold module circumvents voltage rate-of-change limitations at

the analogue-to-digital converter's input. A Time Period Generator-Divider supplies the Walsh cycle interval clocking pulses to the Walsh function generator, and a Dual Arithmetic Processor receives the digitized signal samples and the sal and cal values and produces the Walsh coefficients, A_s and B_s. The generator-divider makes extensive use of four-stage integrated counters, achieving period measurement and T/64 interval generation to 0.1% timing accuracy with only 11 integrated circuits. The arithmetic processor simultaneously performs signed accumulation and programmable division which eliminates the number-of-samples term in the output coefficients. Because of the fixed sampling rate, this term would otherwise constitute a variable in the output coefficient which is dependent on the input-waveform period. The Walsh coefficients are available immediately at the end of the second cycle of the input waveform, the first cycle being used to measure the waveform's period. The Walsh coefficients are available in Binary-Coded Decimal format and are easily normalized with respect to the input waveform analogue voltage. Analyzer system control is straightforward and lends itself easily to special-purpose hard-wired logic implementation or to interfacing with a minicomputer. The latter method provides on-line real-time Walsh spectral analysis of periodic waveforms. The Walsh spectral analyzer produces pairs of Walsh coefficients up to and including a sequency of 31 and accepts periodic input signals of unknown bandwidth having fundamental frequencies in the four decade ranges from .005 Hz to 50 Hz.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

LIST OF SYMBOLS AND ABBREVIATIONS

a,b,c...	:	sequency programming address
a_n	:	even ordered Fourier coefficient
a_0	:	zero order or "dc" Fourier coefficient
A,B,C,D	:	cal toggle sets
A,B,C,D,E,F,G	:	Binary Rate Multiplier rate inputs
A/D	:	analogue-to-digital
A_s	:	even ordered Walsh coefficient
A_0	:	zero order or "dc" Walsh coefficient
b_n	:	odd ordered Fourier coefficient
B_s	:	odd ordered Walsh coefficient
BCD	:	binary coded decimal
C_e	:	count enable
C_i	:	carry in
CLI	:	clocking input
CLO	:	clocking output
CMOS	:	complementary metal-oxide semiconductor
db	:	decibel
DWT	:	Discrete Walsh Transform
f	:	frequency
F	:	frequency (normalized)
f_m	:	maximum frequency signal component
f_c	:	low-pass filter cutoff frequency
f_s	:	sampling frequency

H	:	number of samples
Hertz	:	cycles per second
HI	:	positive true logic state (TTL: > 2.0 volts)
ISS	:	Input Sampling System
J	:	number of counts (time measurement)
K, K	:	variable representing binary counter stages
kilohertz	:	cycles per second X 10^3
L	:	set of Walsh cycle intervals
LO	:	positive false logic state (TTL: < 0.8 volts)
lsb	:	least significant bit
lsd	:	least significant decimal
M	:	mode control
Mhz	:	cycles per second X 10^6
microsecond	:	second X 10^{-6}
millisecond	:	second X 10^{-3}
msb	:	most significant bit
msd	:	most significant decimal
MSI	:	medium scale integration
n	:	number of Walsh cycle interval
N_a	:	number of counts (accumulator)
NAND	:	positive logic negated AND gate function
nanosecond	:	second X 10^{-9}
NOR	:	positive logic negated OR gate function
p	:	number of A/D converter quantization states
P,Q,R,V	:	sal toggle sets
PRO	:	processor

P_+	:	polarity
Q_h	:	digitized analogue voltage sample (hth)
R	:	remainder counts (time measurement)
s	:	sequency
S	:	sequency (normalized)
S_{max}	:	maximum sequency
SGN	:	sign
$\overline{STATUS}$	:	status of A/D converter (inverted logic)
SC	:	Sample Counter
S-H	:	Sample-Hold (Module)
SRG	:	Sampling Rate Generator
SRS	:	Sampling Rate Signal
SYSC	:	System Clock
T	:	period of analogue waveform
T_a	:	aperture time
T_c	:	conversion time
T_{cl}	:	clock period
TTL	:	transistor-transistor-logic
T/64	:	period of Walsh interval
$U/\overline{D}$	:	up or down counter mode control
V_i	:	input voltage
$V_{i_{max}}$	:	maximum input voltage
V_{i_p}	:	maximum input voltage accepted by A/D converter S-H module
V_{max}	:	maximum input voltage accepted by A/D converter
x,y,z	:	binary state-counter output variables
zps	:	zero crossings per second

α, β, γ	:	sequency address variables (= s-1)
τ	:	time of Walsh cycle interval
ω	:	radians per second
$\oplus$	:	modulo-2 binary adder function (EXCLUSIVE-OR)
θ	:	Walsh cycle interval

CHAPTER I

INTRODUCTION

Analysis of the audio and sub-audio frequency ranges via a Walsh Spectral Analyzer is an attractive alternative to the more common Wave or Fourier Analyzers. Conventional wave analyzers for periodic electrical waveforms are constructed with analogue circuit elements which must be adjustable, accurately calibrated and stable. These requirements pose greater difficulties with decreasing frequency, and an added problem is the long measurement time, often several cycles of the input signal, needed to produce the result. However, Walsh Spectral Analysis via digital techniques does not suffer any implementation penalty with decreasing frequency. The digital Walsh analyzer produces the spectral coefficients in only one cycle of the input waveform, after the waveform period is known. One additional cycle is required to measure the period. Also, the digital Walsh analyzer can operate well into the audio region and still produce coefficients after only one cycle of the input waveform.

Spectral analysis via Walsh functions may be described by comparison with the more familiar Fourier Analysis. A periodic waveform, f(t), may be expressed as a Fourier series:

$$f(t) = a_0 + \sum_{n=1}^{\infty} [a_n \cos(n\omega_0 t) + b_n \sin(n\omega_0 t)] \qquad (1\text{-}1)$$

where

$$a_0 = \frac{1}{T} \int_0^T f(t)\,dt \qquad (1\text{-}2)$$

$$a_n = \frac{2}{T} \int_0^T f(t) \cos(n\omega_0 t)\,dt \qquad (1\text{-}3)$$

$$b_n = \frac{2}{T}\int_0^T f(t)\sin(n\omega_0 t)dt \qquad (1\text{-}4)$$

The period of the fundamental frequency is T. The coefficients a_n and b_n provide information relative to harmonics in the "frequency" domain whereas Walsh analysis yields harmonics in the "sequency" domain. Sequency refers to zero crossings per second (zps) whereas frequency refers to cycles per second. However, there is still similarity to the Walsh series expression of a periodic waveform f(t):

$$f(t) = A_0 + \sum_{s=1}^{\infty}[A_s\,cal(s,\theta) + B_s\,sal(s,\theta)] \qquad (1\text{-}5)$$

where

$$A_0 = \frac{1}{T}\int_0^T f(t)\,cal(0,\theta)dt \qquad (1\text{-}6)$$

$$A_s = \frac{1}{T}\int_0^T f(t)\,cal(s,\theta)dt \qquad (1\text{-}7)$$

$$B_s = \frac{1}{T}\int_0^T f(t)\,sal(s,\theta)dt \qquad (1\text{-}8)$$

The binary-valued Walsh functions sal and cal assume only the values of +1 and -1 and are easily compatible with binary-valued digital logic circuits. Once the Walsh coefficients are calculated, they may be converted to Fourier coefficients, if desired.

The digital Walsh analyzer presented in this thesis is developed from the design formerly considered by Siemens [1] and reported by Siemens and Kitai [2]. Equations (1-7) and (1-8) are implemented as a Discrete Walsh Transform (DWT) in which the periodic input waveform, f(t), is sampled and digitized, thus allowing the Walsh coefficients to be determined completely in the digital realm. When f(t) is periodically sampled to provide Q_h, the digitized value of the sampled analogue voltage, equations (1-7) and (1-8) become the instrument equations:

$$A_s = \frac{V_{max}}{pH} \sum_{h=1}^{H} |Q_h| SGN(Q_h) cal(s,\theta)_h \qquad (1\text{-}9)$$

$$B_s = \frac{V_{max}}{pH} \sum_{h=1}^{H} |Q_h| SGN(Q_h) sal(s,\theta)_h \qquad (1\text{-}10)$$

The term V_{max} denotes the maximum voltage which may be presented to the analogue-to-digital (A/D) converter, and p represents the number of the converter's quantization states. The term H gives the number of samples taken during the cycle. The values of the sal and cal functions at the time of each sample are a function of s, the sequency order, and θ, the Walsh cycle interval.

The digital Walsh analyzer implements all of the arithmetic and timing operations indicated in the instrument equations via digital circuitry. The functions required are provided by 1) a Time Period Generator-Divider which produces the Walsh cycle interval clocking pulses for any waveform period, 2) an Input Sampling System which band-limits, samples and digitizes the input waveform, 3) a Dual Aritheetic Processor which executes the instrument calculations, and 4) a Walsh Function Generator which produces the sal and cal values. Extensive use of Medium Scale Integration (MSI) multi-function integrated circuits requires only 70 integrated circuits to perform these analyzer functions, excepting only the analogue and conversion modules used in the Input Sampling System. The analyzer system operates over 4 decade ranges of input signal fundamental frequency, the highest range being 5.0 Hz - 50 Hz. The low frequency limit is set at 0.005 Hz, but there is no theoretical lower limit to the analyzer's operation. When the input signal to be analyzed is known to be band-limited to no more than 32 harmonics of the fundamental

frequency, the upper fundamental frequency limit of the highest range may be extended to 150 Hz.

Chapter 2 presents the Time Period Generator-Divider which produces the Walsh cycle interval clocking pulses. The generator-divider has two modes of operation: the first mode corresponds to the first cycle of the analogue waveform in which a measure of period T is established. The second mode corresponds to the waveform's second cycle during which the Walsh coefficient calculations are made. After the start of the second cycle, the generator-divider produces an interval clock pulse each T/64 seconds. These pulses are fed to the Walsh Function Generator.

The generator-divider obtains its reference time period from the spectral analyzer 10 megahertz system clock. Timing error figures are discussed in two areas: period (T) measurement and interval (T/64) generation. It is shown that the generated interval clock pulses are accurate to within 0.1% for all analyzed waveform fundamental input frequencies. This accuracy is achieved with a generator-divider design requiring only 11 integrated circuit MSI modules.

Chapter 3 considers the problems of sampling and digitizing a periodic waveform of unknown bandwidth. Two approaches are discussed: the use of a variable sampling rate which allows the same number of samples to be made for a waveform of period T, and a fixed sampling rate which requires that the Walsh coefficients be calculated for any number of samples. The final design for the Input Sampling System features operation over four decade ranges with a fixed sampling rate for each range. This allows a low-pass filter with a fixed cutoff

frequency to be used with each range and also maintains the number of samples between 200 and 2000. The highest sampling rate is 10 kiloHertz which establishes a minimum time of 100 microseconds during which the A/D conversion must occur. A sample-hold module is required to circumvent voltage rate-of-change limitations at the A/D converter's input.

The Dual Arithmetic Processor is presented in Chapter 4. This subsystem performs the calculations dictated by the instrument equations and provides the sal and cal coefficients immediately at the end of the second or calculate cycle. Two main elements of the processor are the programmable overflow divider and the coefficient output accumulator. The programmable overflow divider combines the functions of signed accumulation and variable-modulus counting to provide division by H, the number of samples made during the calculate cycle. The term H is made available at the end of the time period measurement cycle by a special counter which is clocked by the sampling rate signal. The coefficient output accumulators feature a 3-place fractional BCD format, the same format of the A/D converter output, thus simplifying normalization of the output coefficient with respect to the analyzer input voltage.

Chapter 5 contains the Walsh Function Generator. The design is based on the manipulation of T-type flip-flop toggle logic functions to achieve sequency programmability of the dual orthogonal Walsh outputs. The derived toggle logic functions are economically implemented by a Binary Rate Multiplier integrated circuit. The resulting generator provides orthogonal Walsh pairs to a sequency of 63, a synchronizing

output, an end-of-cycle indicator, and requires only 7 integrated circuits. An additional feature is very low orthogonality error of a few tens of nanoseconds, due only to differences in switching times between synchronously clocked flip-flops.

Variations of the basic Walsh Function Generator design are presented, discussing both the generator structure and hardware implementation. Since the Walsh analyzer described in this thesis requires Walsh pairs to a sequency of only 31, a method for reducing the sequency capacity of the generator is presented. Also, additional Binary Rate Multipliers may be cascaded to expand the generator's capacity. Adaptation of the design for array generation is also possible. Hardware implementation alternatives are Schottky-Clamped TTL to increase the generator clocking frequency from the 10 megahertz region to above 50 megahertz while reducing orthogonality to a few nanoseconds, and Low Power CMOS to provide a flexible Walsh Function Generator with extremely low power requirements.

Chapter 6 considers the Walsh analyzer as an operating system and details the function of each of the subsystems. Additional economy in implementation is achieved by combining the decade-ranging counting circuits into one subsystem which provides both system clock and sampling rate signal for the entire analyzer. Complete analyzer operating control requires only two mode controls and five reset controls. Decade range selection must be provided to the clock circuits and to the Input Sampling System and sequency programming to the Walsh Function Generator.

Chapter 7, the conclusion, summarizes the major features and

specifications of the Digital Walsh Spectral Analyzer. Also indicated are directions along which further Walsh analyzer development might proceed, including a possible system reconfiguration, depending on digitally programmable analogue components which may become available. Further investigation of low power hardware implementation is suggested.

The Digital Walsh Spectral Analyzer designed and constructed in this thesis project has demonstrated a straightforward yet flexible approach to spectral analysis. Efficient operation and economy of implementation especially characterize the design advances presented in these areas:

- the Walsh cycle interval or T/64 generator which uses both counting and storage functions to achieve 0.1% timing accuracy while using only 11 integrated circuits,
- the dual arithmetic processor which simultaneously performs signed accumulation and programmable division to eliminate the number-of-samples term, H, in the Walsh output coefficients, and
- the Walsh function generator which provides sequency programmable dual orthogonal Walsh outputs with extremely low orthogonality error while requiring only 7 integrated circuits.

CHAPTER 2

TIME PERIOD GENERATOR-DIVIDER

2.1 Introduction

The approach to time period division via digital means as originally reported by Siemens [3] is considered. The fundamental relationships between finite time intervals and switching mechanisms as used in this method are derived. These derivations provide the basis for a detailed error analysis, yielding the limits of frequency ranges over which this method may be used and the respective accuracy figures for those ranges. A final circuit configuration for the generator-divider is presented and its operating characteristics and timing accuracies are indicated.

The hardware implementation of the final generator-divider design makes extensive use of the multiple functions provided by MSI counters which have become available. It is shown that detail changes in the execution of the necessary counting operations which are readily accommodated by these counters, when used with additional MSI functions, afford a package count reduction of 36 to 11 over previous designs [3].

2.2 Basic Time Period Generator-Divider Requirements

Once the fundamental period of the signal to be analyzed has been determined, either by detecting, in general, an even number of consecutive positive-going zero crossings, or via external "start" and "stop" signals, means must be available whereby this period can be divided into 64 time segments of equal length. Further, these 64 smaller periods, each of duration T/64 seconds, must be located within the period T such that the

period T and the first T/64 segment are initiated simultaneously and also that T and the last T/64 segment terminate simultaneously, or very nearly so. When the first T/64 segment terminates, an output pulse is generated and the second T/64 segment is initiated. This sequence repeats itself until the final T/64 segment and the period T expire, nearly simultaneously. Figure 2-1 illustrates for the ideal case the relationship of all the time segments involved including the corresponding signal pulses.

2.2.1 Measuring Period T

The first operation of the Time Period Generator-Divider is to establish a measurement of the fundamental Time Period T upon which subsequent timing operations will be based. This is achieved by recording with a counter the number of pulses produced by a free-running clock. Illustrated in Figure 2-2 is a binary counter for the general case of K stages or flip-flops. A set condition at stage K represents 2^{k-1} counts. For the total counter of K stages, the highest number of counts that can be represented is $\sum_{k=1}^{K} 2^{k-1}$. Calculation of this series, or simply by inspection of the binary counter, shows the total number to be 2^K-1 counts. Hence, for an K stage counter, 2^K-1 represents the highest number of clock pulses which can be recorded during T.

The counter circuits start at the all-zero state and are incremented up one count for each clock pulse produced between the "start" and "stop" pulses. The first stage is clocked or toggled by the system clock. The toggle input to any following stage is determined by the state of the preceding flip-flop(s), in accordance with the binary code. The final digital word, J remaining in the counter, in binary format, represents what multiple

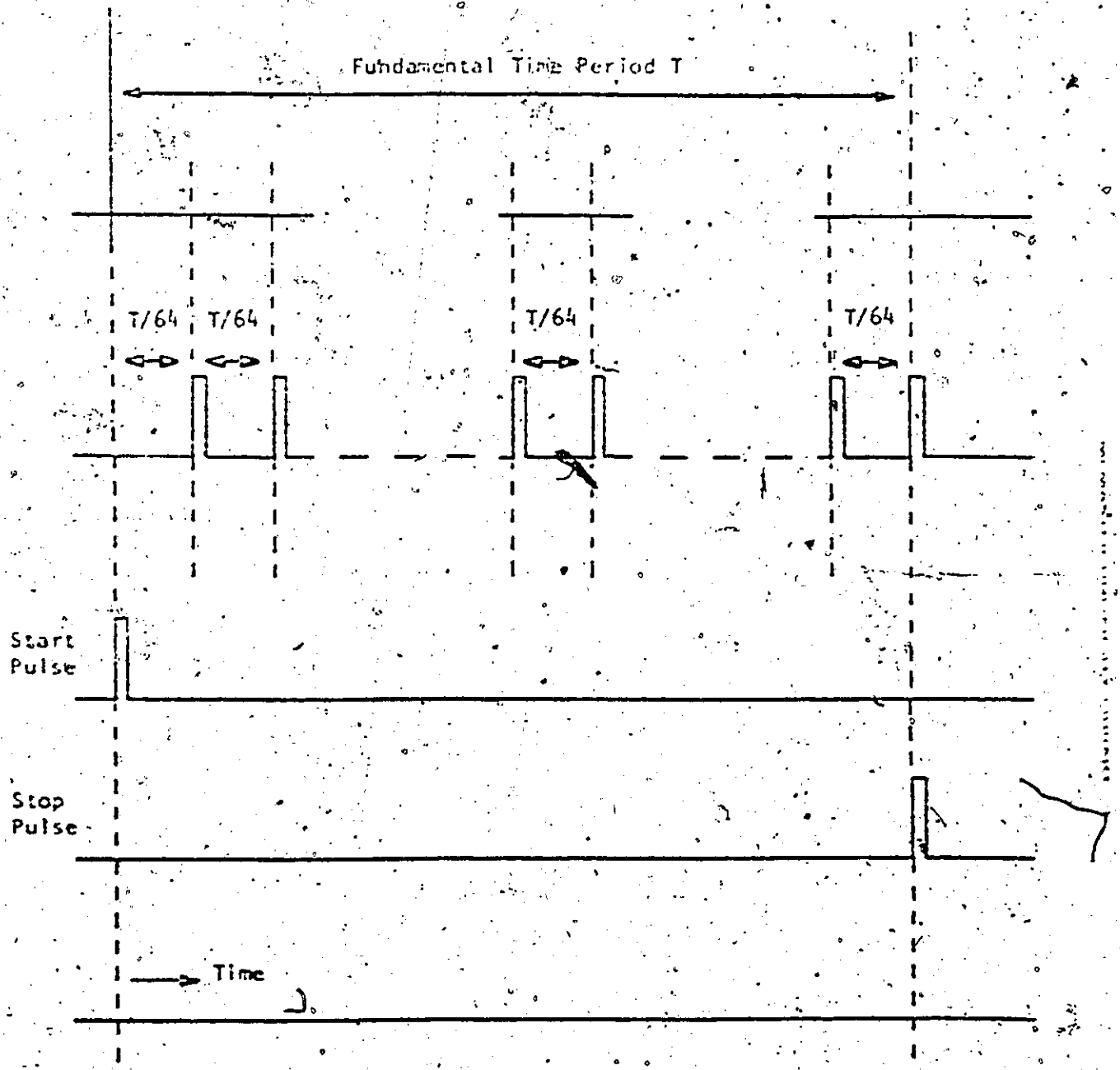


Figure 2-1 Period (T) and Interval (T/64) Timing for the Ideal Case

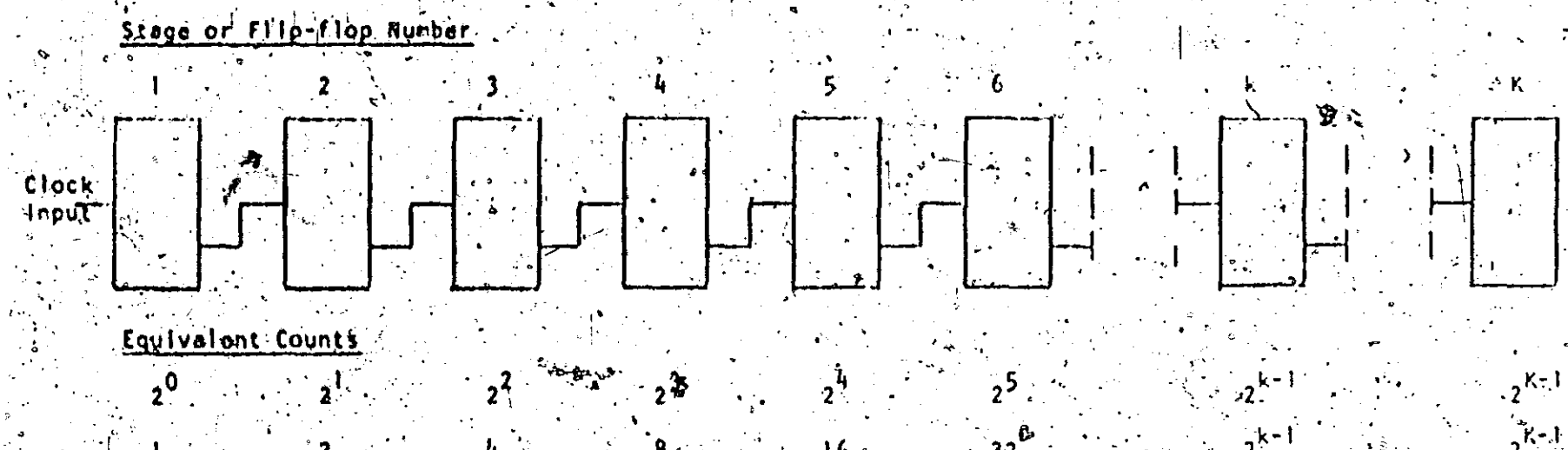


Figure 2-2. Counting Capacity for a Binary Counter of K Stages

T is of the clock period T_{cl}. In the general case the relationship is not exact, ie. T is not exactly equal to JT_{cl} seconds. The error is due to practical gating considerations and the finite duration of T_{cl}. These error contributions and others are investigated in a following section.

2.2.7 Generating the T/64 Segments

Since the binary word, J, remaining in the counter after the up count operation effectively records whole or integer clock pulses, the radix point of this word is located just to the right of the lsb. A radix point shift of 6 places toward the msb yields a digital word representing J/64 thus accomplishing a binary division by 1000000. This J/64 word represents the final count-state of a second counting operation whose duration is equal to the desired T/64 time segment. This is achieved by using the same clock pulses of period T_{cl} seconds to increment a secondary counter which will terminate its count operation $(J/64)T_{cl}$ seconds after initiation. This operation is subsequently repeated, producing a pulse each time the counter reaches the J/64 state which successively marks a time period approximately equal to the ideal T/64 increment.

Again, the error contributions introduced here will be examined in a following section.

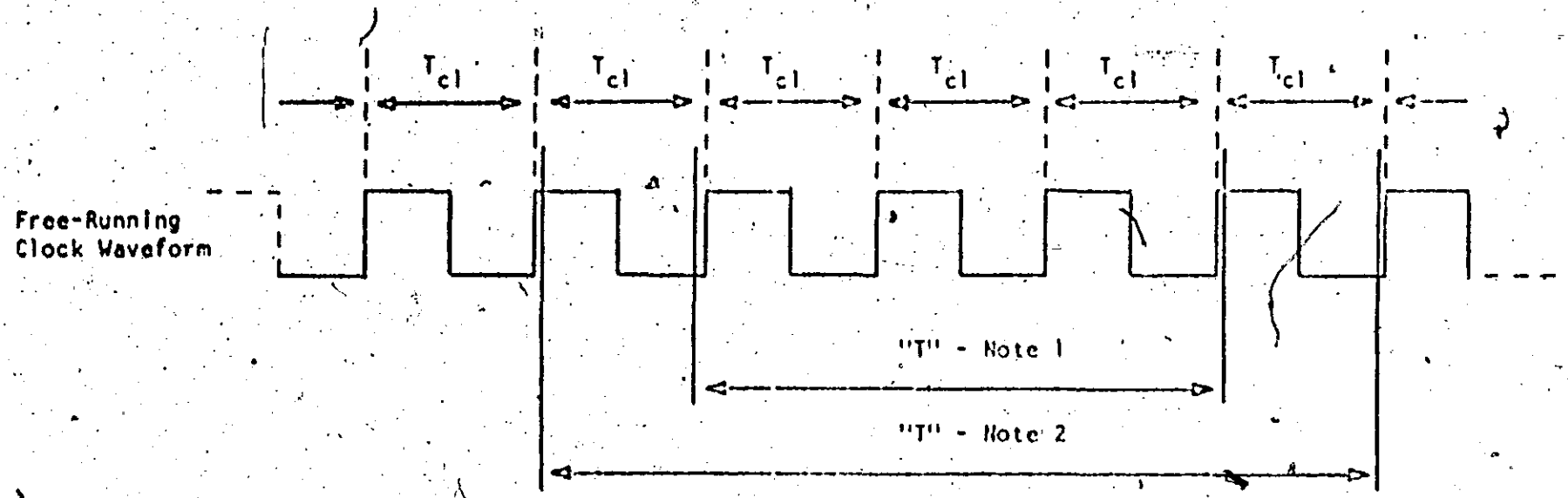
2.3 Error Considerations

The operation of the Time Period Generator-Divider has thus far been discussed qualitatively, with the implication that T_{cl} is very much smaller than T. The following section defines a limit for this relationship and also considers the inaccuracies resulting from the "free-running"

systems clock. The next section deals specifically with the errors related to T/64 increment generation. A general error expression is derived and a worst-case figure is calculated and discussed.

2.3.1 Errors Related to Overall Time Period Measurement

To assess the errors in this area, it is sufficient to consider the "free-running" nature of the clock and the ratio of T_{cl} to T, T being the fundamental period of the signal being analyzed. The first error occurs because there is no determinable relationship between the arbitrary "start" of the time period T and the clock pulse cycles. Also, there is an equally arbitrary relationship at the end of T. Since the period T is being measured in multiples of T_{cl} seconds, the greatest error possible is T_{cl}. Therefore, the expression of the measurement of T is $JT_{cl} \pm T_{cl}$ seconds where J is the number of counts remaining after the first up-count operation. These two boundary conditions ($+T_{cl}$ and $-T_{cl}$) are illustrated in Figure 2-3. In the first case, period T approaches $3T_{cl}$ and, in the second case, it approaches $5T_{cl}$ segments in length of time. The case of coinciding events at the start of period T is defined to be a no-count condition. Each unit count represents a full cycle of the clock waveform of duration T_{cl}. Since 4 counts, marked by LO to HI clock transitions, are contained within the boundaries of T for both cases shown, the resultant J will be identical, namely 4 counts. Thus, this example demonstrates the maximum error of $\pm T_{cl}$. From this it can be seen that the ratio of T_{cl} to T will determine the measurement accuracy of the overall period T. Hence, the expression for maximum error in percent as a function of these variables is $(T_{cl}/JT_{cl}) \times 100\%$ or $(1/J) \times 100\%$. Table 2-1



Note 1 - "T" for case approaching maximum negative error

Note 2 - "T" for case approaching maximum positive error

Figur 2-3 Minimum and Maximum Period (T) Measurement Error

COUNTS J	ERROR (1/J) X 100%	COUNTER REQUIRED K STAGES
2,048	0.049 %	12
8,192	0.012 %	14
32,768	0.0031 %	16
131,072	0.00076 %	18
524,288	0.00019 %	20
2,097,152	0.000048%	22
8,388,608	0.000012%	24

Table 2-1 Maximum Period (T) Measurement Error for K Stage Binary Counter

shows some error percentages as related to counts J. A count of 2048, for example, would need at least a 12 stage counter thereby limiting the maximum error to 0.049%. Therefore, if the twelfth stage of a counter is set and no high stages are set, the error cannot exceed 0.049%. If other additional stages below the twelfth are set, the error will be decreased.

2.3.2 Error Related to T/64 Generation

The most significant contribution to timing error in the generation of the T/64 output pulses is revealed by considering the effective radix point shift operation. In the general case, the binary word which extends from the shifted radix point location to the lsb of the primary up counter will not be all zeroes. This word represents the remainder when J is not evenly divisible by 64. For example, if the final counter state after the up-count phase was all zeroes with the exception of the seventeenth bit, J would be 2^{16}, or 65,536 counts, which when divided by 64 yields 1024 with no remainder. Hence, the sixty-fourth T/64 output pulse would occur simultaneously with the expiration of T seconds during the secondary counting phase, subject only to the error of overall time period determination. In the case where a non-zero word remains in the first five counter stages after the up-count phase, this word represents the number of counts the final T/64 output pulse falls short of the actual expiration of period T. Since all the T/64 output pulses produced by this generator must mark equal intervals in time, it is seen that the true timing error relative to the ideal location in time of any T/64 output pulse

increases with the number of the output pulse generated. For example, the largest remainder which can be left in the first five stages of the up counter represents 63 counts. Hence the final, or sixty-fourth, output pulse would arrive $63T_{c1}$ seconds earlier than it should. This leads to an expression for the error of the last output pulse as positioned in time of (63/J) X 100%. The important values calculated by this expression result from final counter states as illustrated in Figure 2-4. Here only one bit-position outside the remainder word representing a number evenly divisible by 64 is set. The remainder word in the first 6 stages corresponds to the maximum 63 counts. Table 2-2 shows the error figures calculated again as a function of K, the number of counter stages. The instance of a set condition in any flip-flop between the sixth and the last still represents a quantity of counts evenly divisible by 64 and thus decreases the error calculated by the expsession. Any number of counts in the remainder word location smaller than 63 reduces the error by a proportionate amount.

A more general expression enables the calculation of the T/64 output pulse timing error for any T/64 pulse. This expression requires an additional variable, n representing the number of the output pulse of interest. The error in percent equals n/64 X (R/J) X 100%, where n is the pulse number (from 1 to 64), and R is the remainder count (from 0 to 63). The contribution to timing error associated with the overall time period measurement as discussed in section 2.3.1 is ignored in this equation because its worst case magnitude of (1/J) 100% is comparatively insignificant.

Figure 2-5 illustrates via two detail diagrams the significant departures from the ideal timing scheme shown previously in Figure 2-1.

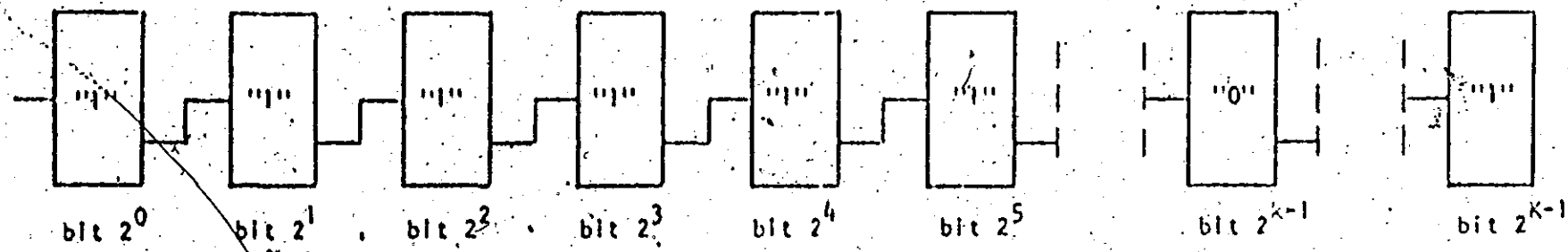


Figure 2-4 Maximum Error-Count Condition for Interval (T/64) Generation

COUNTS J	ERROR (63/J) X 100%	COUNTER REQUIRED K STAGES
2,048 + 63	3.1 %	12
8,192 + 63	0.78 %	14
32,768 + 63	0.20 %	16
131,072 + 63	0.049 %	18
524,288 + 63	0.012 %	20
2,097,152 + 63	0.0031 %	22
8,388,608 + 63	0.00076%	24

Table 2-2 Maximum Generated Interval (T/64) for K Stage Binary Counter

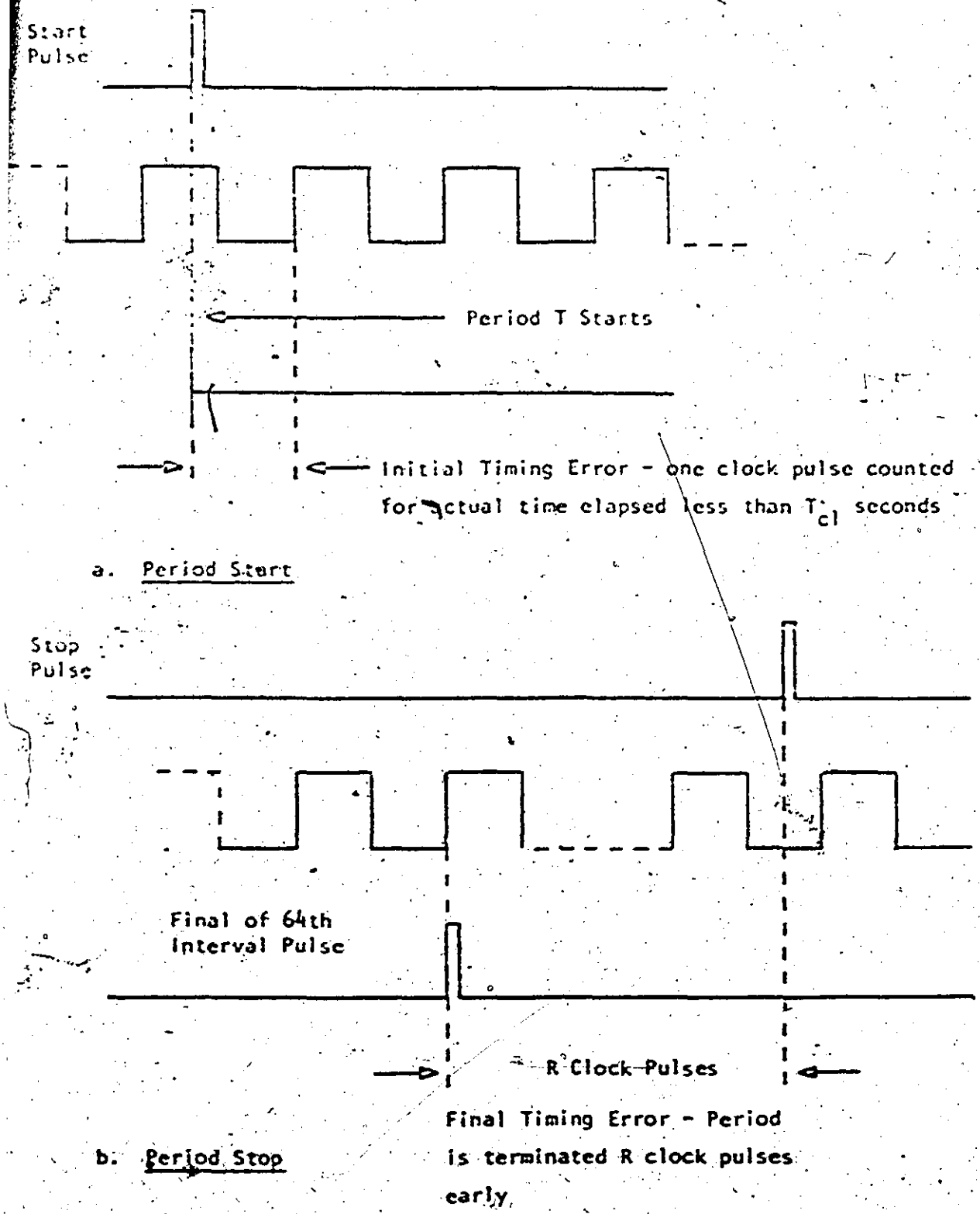


Figure 2-5 Period (T) and Interval (T/64) Timing for the Practical Case

The two areas considered are at the beginning of T, and near the end of T where the final T/64 pulse is produced.

2.4 Final Design and Hardware Details

The preceding sections have derived general criteria for the sequential or counting operations necessary to achieve the desired time period division and output pulse generation. Accompanying this, performance criteria have been presented which illustrate the accuracies obtainable for counters of various sizes. Using these relationships, the possible configurations of generator designs are now discussed. The final design makes extensive use of the multiple function capability of currently available MSI counters. The design accommodates a large range of input time periods T and also provides under and over-range indication. Further, it is demonstrated that the error figures previously derived are achievable with standard 74-series TTL integrated circuits.

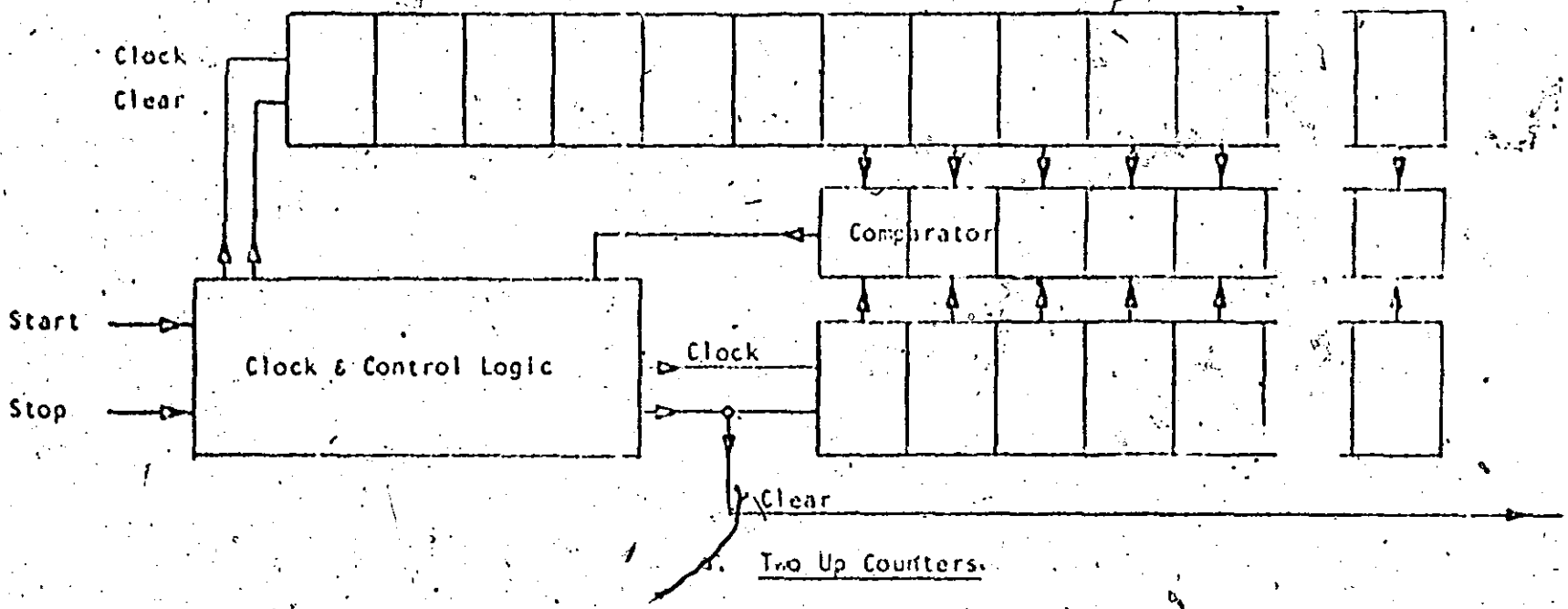
2.4.1 Circuit Configurations, Error Figures and Range Limits

The counting operations which need to be implemented may be summarized as follows: a first or primary phase in which an up counter, having its clocking input gated on and off coinciding with period "start" and "stop" signals, establishes the number of counts J, and a secondary phase in which a counter is clocked for a predetermined number of counts approximately equal to J/64, thus generating the time segment T/64. The design employed earlier by Siemens[3] met these requirements by means of two separate up counters. In the secondary phase, a counter was started at zero and a comparator circuit detected the arrival of the counter at

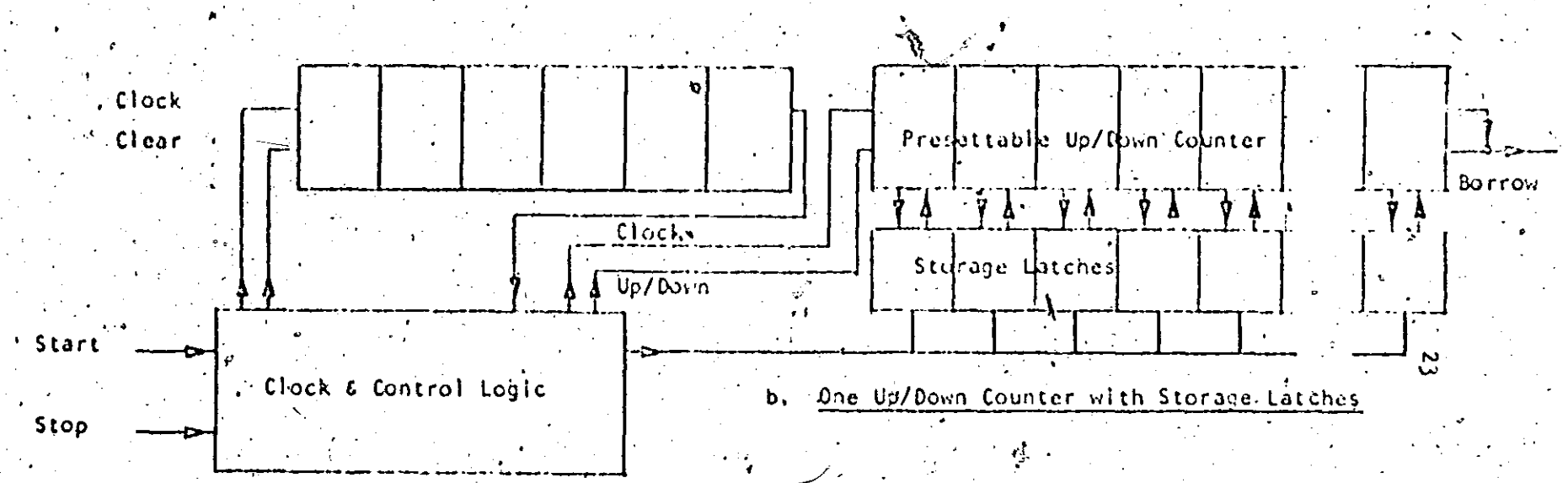
J/64 counts. The counter was immediately cleared and the operation repeated another 63 times during period T. The counter clearing pulses provided the T/64 generator output. However, to supply a constant reference for the comparator, the first-counter was required to remain undisturbed after reaching its J counts. Figure 2-6a illustrates the main elements of this generator design. An alternate approach is based on the fact that a counter which can be preset to a state equivalent to J/64 and can count down to the zero state will also mark a time segment equal to T/64 seconds. In this way the same type of counter may be used for both phases and the down-count operation, and it eliminates the previously necessary comparison function. When the down counter reaches the all zero state, the next clock pulse produces a borrow pulse from the counter. This borrow pulse is used as the T/64 output pulse. Also, if the binary word representing J/64 can be stored external to the first counter, the same counter can be used in the down count mode accomplishing also the T/64 pulse generation. It is merely necessary to then return or to preset the counter to the J/64 state and repeat the down-count operation. Figure 2-6b illustrates this design approach. Here only one chain of counters is employed and the comparator is replaced by simple storage latches. After the first six counter stages, the count mode must be controlled and this is achieved via separate clocking inputs.

The actual number of counter stages to be used in the generator is determined by two basic constraints: one is the error figure as listed in Table 2-2 and the other is the maximum number of counts the counter is required to accept. These criteria determine the minimum and maximum number of stages, respectively. The first six stages of the total counter

Figure 2-6 Alternate Time Period Generator-Divider Circuits



a. Two Up Counters.



b. One Up/Down Counter with Storage Latches

are only required to count in the up-mode and therefore are considered separately. Following these stages, 16 further stages are employed giving a total of 22 flip-flops. A set condition in the twenty-second flip-flop is used as the over-range indicator which holds the maximum acceptable count to a state in which all the other stages are set. This state represents $2^{21}-1$ counts or 2,097,151 counts. At the other count extreme, means are provided to assure a minimum count which reaches at least the 16th flip-flop. This constraint assures a maximum error in T/64 output pulse timing of 0.20%, as listed in Table 2-2. The logic circuitry required to assure that this constraint is satisfied will give indication if none of the flip-flops from the 16th to the 20th, inclusive, are set at the termination of the primary up-count phase.

The range of time periods T which constitute acceptable input to the generator-divider are calculated after choosing a reasonable value for the system clock time period. This value of T_{cl} is 100 nanoseconds, which corresponds to a clock frequency of 10 Mhz. The error-limited minimum number of counts is 32,831, i.e. only the 16th stage in the set condition, and the counter capacity-limited maximum is 2,097,151. Hence, the boundaries on T are 3.2831 msec and .2095151 seconds. This corresponds to an approximate frequency range of 5 to 300 Hz, with a maximum timing error in T/64 pulse generation of 0.2%. The same timing accuracy can be maintained over a lower frequency range simply by reducing the clock frequency. For example, a 1 Mhz clock would allow divider-generator operation in the 0.5 to 30 Hz range. It is desirable to operate the divider-generator near the lower extreme of any given frequency range; this results in a greater number of counts stored and a lower timing

error as shown in Table 2-2.

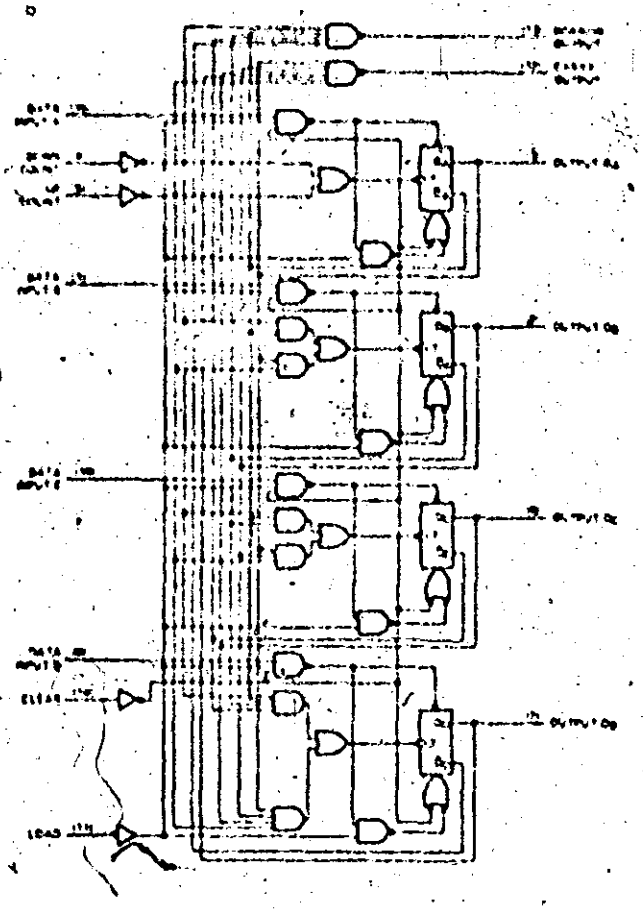
2.4.2 Hardware Implementation: Integrated Circuits

The circuit function of primary importance to the implementation of the line period generator-divider is provided by the SN74193, a 4-bit binary synchronous presettable counter with up-and down-count inputs. The internal circuitry and essential timing and switching information are reproduced [4] in Figure 2-7a and 2-7b. All the necessary cascading circuitry is provided internally; the carry and borrow outputs connect directly to the up-and down-count inputs of the succeeding stage. Figure 2-8 illustrates the complete wiring diagram for the generator-divider. The necessary data storage operation is provided by integrated circuit type SN7475, a 4-bit bistable latch. This device is employed because the change from "follow data" to "store data" is a simple HI to LO level transition at its clock inputs. The first 6 binary counter stages are provided by the type SN7497 6-bit binary rate multiplier. It provides many functions in addition to division by 64 and these are discussed in detail in the chapter on Walsh function generation. It is employed here, however, because it provides the divide-by-64 function complete in one package. One package of SN7402 positive logic NOR gates provides all the clock and control gating necessary. Two of the gates are used as inverters; one inverts the control sense which routes the clock pulse either through the divide-by-64 module or direct to the programmable counter stages, the other maintains the LO to HI transition as the active clocking edge in the down count mode.

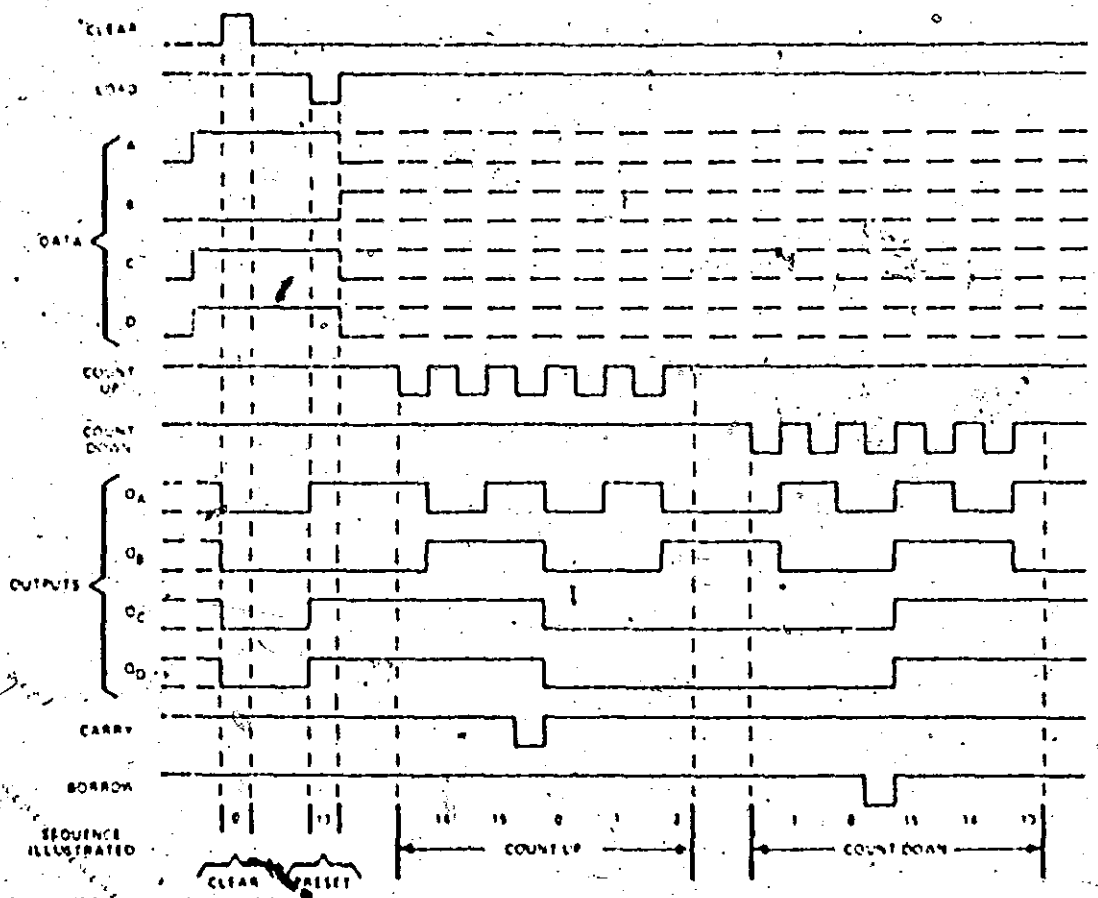
typical clear, load, and count sequences

Illustrated below is the following sequence

1. Clear outputs to zero
2. Load (preset) to binary thirteen
3. Count up to fourteen, fifteen, carry, zero, one, and two
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen



a. Internal Circuitry



b. Timing Details

Figure 2-7 4-bit Binary Synchronous Presettable Up/Down Counter: Type SN74193

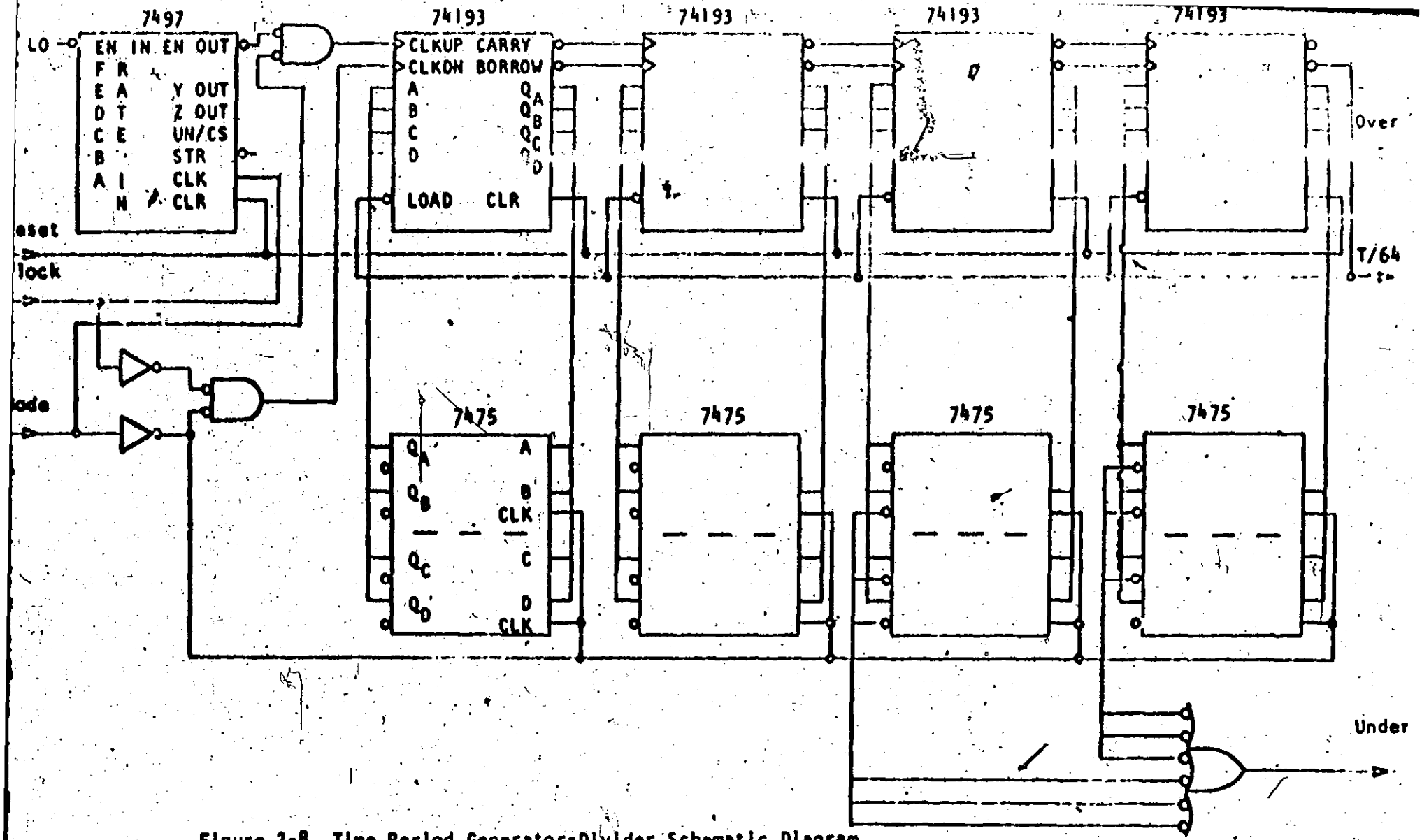


Figure 2-8 Time Period Generator-Divider Schematic Diagram

Over-range indication that the clock is too fast and/or T is too long is provided by a HI state in the last stage of the counter. To assure operation within the maximum error bound of 0.2% in T/64 pulse generation, a logical 1 must be present at the 2^{15} bit location, or higher. Bits 2^{15} through 2^{20} appear in inverted sense at the output of their respective storage latches. A 6-input negative logic OR gate, implemented by a SN7430 8 input NAND gate provides this under-range indication.

It is convenient that at the termination of the up-count phase, the digital word representing J/64 counts versions in the proper counter stages. Then, when the down-count phase proceeds, the counter reaches zero and produces a borrow pulse which reloads the counter with the J/64 word. Hence, the expiration of the first T/64 segment corresponds with the first borrow pulse.

2.5 Summary

The Time Period Generator-Divider design as derived here requires only 11 integrated circuit modules for its implementation. This is achieved by making extensive use of the multi-function capacity of the MSI types chosen. For a given system clock frequency of 10 Mhz the generator-divider accepts input time periods in the range of 5 Hz to 300 Hz and produces T/64 output pulses with a maximum timing error of 0.2%.

When used in the Walsh analyzer system, the generator-divider is required to operate normally over the decade range of 5 Hz to 50 Hz with a 10 Mhz system clock. The actual timing accuracy specification therefore becomes 0.033% at 50 Hz and 0.0033% at 5 Hz. The optional upper limit for fundamental frequency of 150 Hz gives the maximum error of 0.099%.

CHAPTER 3

SIGNAL SAMPLING CONSIDERATIONS

3.1 Introduction

An important use of the Walsh Spectral Analyzer is to produce Walsh coefficients which may be converted to Fourier coefficients. It has been shown by Siemens and Kitai [5] that if the input signal is band-limited, a Walsh Analyzer may be used to precisely evaluate the signal's Fourier coefficients. The constraint is that F, the highest normalized frequency component of the band-limited signal, must be less than or equal to S, the highest normalized sequency component of the analyzer (FSS).

The analyzer produces the signal's Walsh coefficients by implementing a DWT (Discrete Walsh Transform) via digital circuitry. The input signal is fed to the analyzer through a converter which periodically samples and digitizes the analogue voltage. The limitations placed on the analyzer operation by the sampling process are discussed in two areas: maximum input signal frequency as related to sampling frequency, and maximum signal voltage rate-of-change as related to the conversion time. Additional considerations imposed by the input low-pass filters which are required when performing analysis of unknown signals, are presented. The instrument calculations necessary to produce the Walsh coefficients from the digitized samples are also discussed.

3.2 Sampling Rates for Unknown Signals

The specific area of interest in the frequency domain begins with the determined fundamental frequency, f, of the input signal and includes frequency components which are multiples of this. Any frequency component below the fundamental will be averaged out and taken as the zero order or "dc" term, A_0. The Walsh Spectral Analyzer produces the Walsh coefficients A_s and B_s up to and including a sequency order of 32. Therefore, the amplitude quantized input waveform samples must contain information relevant to an input bandwidth of no less than 32f, where $f = 1/T$. To be consistent with the Sampling Theorem [6], at least 64 samples will need to be taken during T. If only 64 samples are taken, the input signal will need to be band-limited to 32f to eliminate possible aliasing effects. It is permissible, however, to have a sampling rate which will yield more than 64 samples during T and, given proper frequency band-limiting, these samples will be valid. Thus there are two options for the analyzer sampling system design and they are described in the following sections.

3.2.1 Variable Sampling Rate

A possible approach is to take the minimum allowable number of samples. This means that once T is determined, samples are taken only every T/64 seconds during period T, thus satisfying the $2f_m$ sampling rate requirement, where f_m is the maximum frequency component of the input signal. For this analyzer,

$$f_m = 32f. \qquad (3\text{-}1)$$

But to assure the validity of the sampling rate, 64f, it is necessary to feed the analogue input through a low-pass filter which will eliminate frequencies above 32f. Further, the filter must be adjustable to satisfy the 32f bandwidth limit requirement for all f. Thus, both the sampling rate and the low-pass filter cutoff frequency can be established only after the input signal fundamental frequency has been determined. It is also significant that low-pass filters with desirable passband and attenuation characteristics are not easily realized in a tunable configuration.

An advantage of this approach, however, is that the same number of samples are made for any waveform that is analyzed. Recalling the instrument equations from Chapter I, it is seen that if H is constant, some computational simplification will result.

$$A_s = V_{\frac{max}{pH}} \sum_{h=1}^{H} |Q_h| \; SGN\ (Q_h)\ cal(s,\theta)_h \qquad (1\text{-}9)$$

$$B_s = V_{\frac{max}{pH}} \sum_{h=1}^{H} |Q_h| \; SGN\ (Q_h)\ sal(s,\theta)_h \qquad (1\text{-}10)$$

A constant H term with a value of 64 suggests that the division operation could be performed by a radix point shift in a properly organized binary accumulator. But this advantage has to be weighed against the problem of providing an adjustable low-pass filter. An added problem is the positioning of the one sample within the T/64 segment, a position which should be maintained throughout all the succeeding segments of T.

3.2.2 Fixed Sampling Rate

The alternate approach is to establish a fixed sampling rate and a fixed low-pass filter which exhibits the proper cutoff frequency and attenuation characteristics. This means that the number of samples taken during T will change as T changes from waveform to waveform. All the samples taken will still be valid due to proper prefiltering and the number of samples will need to be recorded to supply the H term necessary in the coefficient expressions (1-9), (1-10). In addition to the advisability of a fixed filter, a constant sampling rate has the advantage that the timing circuitry which controls the A/D converter can be optimized for stability in its repetition rate. This is especially important if sample-hold circuits need to be used.

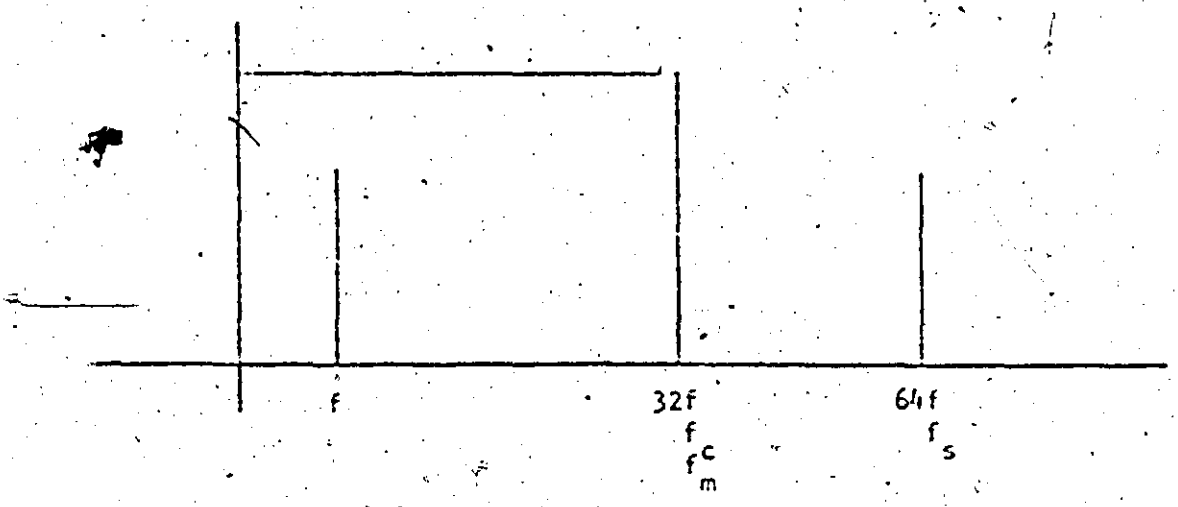
The practical implementation of the input low-pass filter will not exhibit the ideal characteristic of infinite attenuation above the cutoff frequency. Figure 3-1 illustrates the effect the non-ideal filter characteristics have on the relationship between the input signal frequency components and the sampling frequency. In the ideal case, Figure 3-1a, the cutoff frequency, f_c, of the low-pass filter is located at 32f. This assures that no frequency components above 32f will be passed on to the converter and justifies a sampling frequency, f_s, of

$$f_s = 2f_m \qquad (3\text{-}2)$$

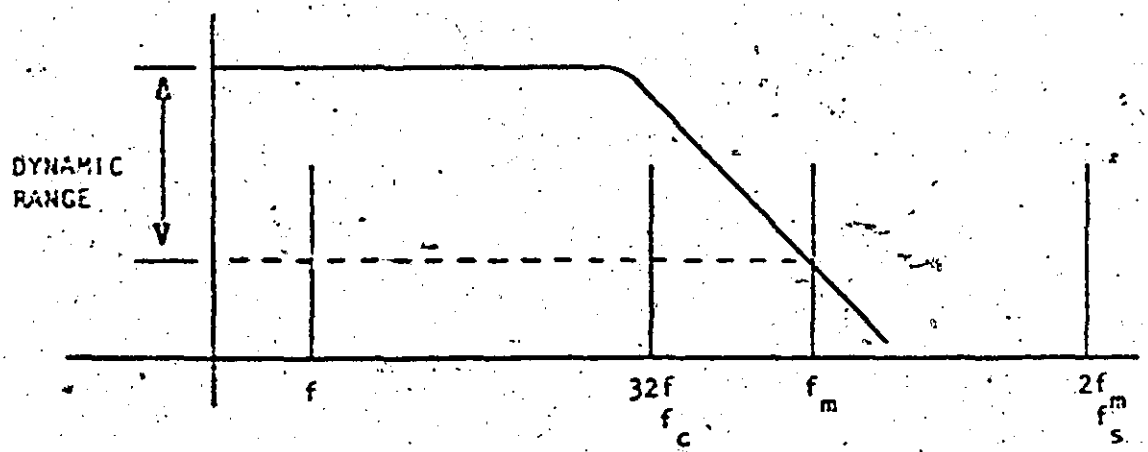
or

$$f_s = 64f. \qquad (3\text{-}3)$$

In the non-ideal case it is necessary to consider the filter's rolloff characteristics in the context of the converter's dynamic range. The criterion here is that any frequency component at half the sampling



a. Ideal Case



b. Practical Case

Figure 3-1 Low-Pass Filter Characteristics

rate, $f_s/2$, must be attenuated below the smallest amplitude which can be resolved by the converter. For example, a converter with 60 db dynamic range sampling at a rate of 10,000 samples per second has to be preceded by a low-pass filter whose attenuation with respect to the passband is at least 60 db at a frequency of 5 kilohertz. The filter's attenuation slope establishes the relationship between $f_s/2$ and 32f. It is assumed that the filter's cutoff frequency coincides with 32f, the highest signal frequency component of interest. The region in the frequency domain between f_c and f_m thus establishes the necessary filter guard band. A practical estimation of the guard band may be made by referring to Figure 3-2 which contains the low-pass characteristics of the Bessel and Butterworth filter modules available from Datel Systems Inc., Canton, Massachusetts. The filter exhibiting the best attenuation characteristic is the 6-pole Butterworth: 60 db attenuation occurs at 3 times the cutoff frequency. This figure compares favorably to the dynamic range of the A/D converter used in the analyzer. The maximum encoded output is 3 BCD digits giving 0.999. The converter therefore resolves to 1 part in 1000 which yields a dynamic range of 60 db.

Using this relationship and again locating f_c at 32f, f_m is now $3f_c$, or

$$f_m = 96f. \qquad (3\text{-}4)$$

Doubling f_m to get the sampling frequency gives

$$f_s = 192f. \qquad (3\text{-}5)$$

Thus for an input signal of unknown harmonic content, the sampling frequency must be approximately 200 times the signal's fundamental frequency when using the assumed 6-pole low-pass filter.

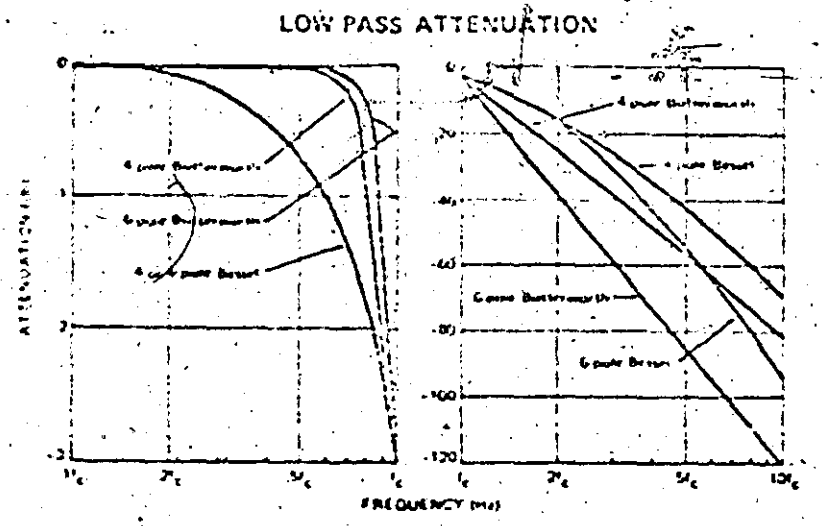


Figure 3-2 Bessel, Butterworth Low-Pass Filter Curves

For a sampling frequency of 10 kilohertz the highest fundamental input frequency is $10 \times 10^3/200 = 50$ Hertz. However, this filter guard band is necessary only with input signals of unknown harmonic content. If it is known that there are no harmonics present above 32f, the filter and thus the filter guard band can be eliminated, giving an f_s of 64f. Keeping f_s constant at 10 kilohertz allows the input signal fundamental to be increased to $10 \times 10^3/64$, or about 156 Hertz. The penalty for not knowing the input signal bandwidth is approximately a reduction by 2/3 of the analyzer's maximum fundamental input frequency.

When operating the analyzer with a low-pass filter, the filter's phase shift characteristics may, in some cases, demand consideration. Uhran [7] has discussed the use of the DWT in signal discrimination and points out certain phase sensitivity aspects of the Walsh power spectra. Whether or not this kind of effect is significant can be determined only after considering each step of the analysis program, from analogue signal conditioning to the manipulation of the output coefficients. In many practical cases, spectral content is highest near the fundamental. Thus any possible effect due to phase disturbance at the higher harmonics ($s = \ldots, 31, 32$) should be negligible in the actual measurement.

3.3 Sampled Data and Instrument Calculations

The output of the signal sampling system is fed to the Dual Arithmetic Processor which produces the Walsh coefficients at the end of each calculation cycle. The processor consists of special purpose accumulators and their maximum counting capacity is dictated by the speed

and resolving capability of the input sampling system. An examination of the calculations required to produce the A_0 coefficient,

$$A_0 = \frac{V_{max}}{pH} \sum_{h=1}^{H} |Q_h| \, SGN\,(Q_h), \qquad (3\text{-}6)$$

for a worst-case input signal illustrates the necessary maximum counting capacity. This condition exists when a constant full scale (V_{max}) input signal is applied to the sampling system for the complete duration of period T. The 3-digit BCD A/D converter used in this analyzer thus gives an output of 0.999 for each sample. In this discussion the decimal point may be neglected and the 999 counts are rounded to 1000. The term $SGN(Q_h)$ is assumed positive and remains unchanged during the period. The accumulator must have the capacity to store 1000 counts for each sample.

The number of samples, H, taken during the period is given by the product of the sampling frequency and T.

$$H = f_s \times T \qquad (3\text{-}7)$$

Since 50 Hertz is the upper fundamental frequency limit for unknown signals, T equals 20 milliseconds. At a 10 kilohertz sampling rate, 200 samples are taken. Hence, storage for a number of 200,000 is necessary. This signal example represents the maximum converter word output, but the shortest period. The analyzer is required to operate over the 4 decade ranges of 50 Hz - 5.0 Hz, 5.0 Hz - 0.5 Hz, 0.5 Hz - .05 Hz and .05 Hz - .005 Hz. At the low frequency extreme the accumulator would have to store a number equal to $.2 \times 10^9$. To eliminate this large variation in required accumulator capacity, the input sampling system is arranged for decade range switching of its important parameters. For an input signal fundamental

frequency in the range of 5.0 Hz - 0.5 Hz, the sampling rate is reduced by a factor of 10 via counting circuits and a different low-pass filter is switched in preceding the A/D converter. In this way the H term is limited to a convenient range (200 - 2,000) and the difficulty in implementing an infinitely tunable low-pass filter is avoided. There is also a computational advantage to decade range switching in that the decimal point, in the case of BCD format, is fixed in one position at the accumulator's coefficient output rather than floating.

The preceding discussion is equally valid for input signals of known bandwidth less than 32f. In this case the low-pass filter is not necessary. The only change in the above conclusions is that the number of samples taken lies in the range of 64 to 640.

Figure 3-3 shows a diagram of the range switching circuitry. The low-pass filter outputs are selected by solid state analogue switches which are directly driven by logic gate outputs. Logic gate switching is also used to select the sampling frequency as derived from the counting circuits.

3.4 Limitations of Data Converters

The conversion of the analogue input voltage to an encoded digital word is not accomplished instantaneously. The finite time required by the conversion process must be small in relation to the time required for the input voltage to change appreciably. This constraint assures accurate digital representation of the waveform sample.

The time-rate at which the input voltage changes is obtained from

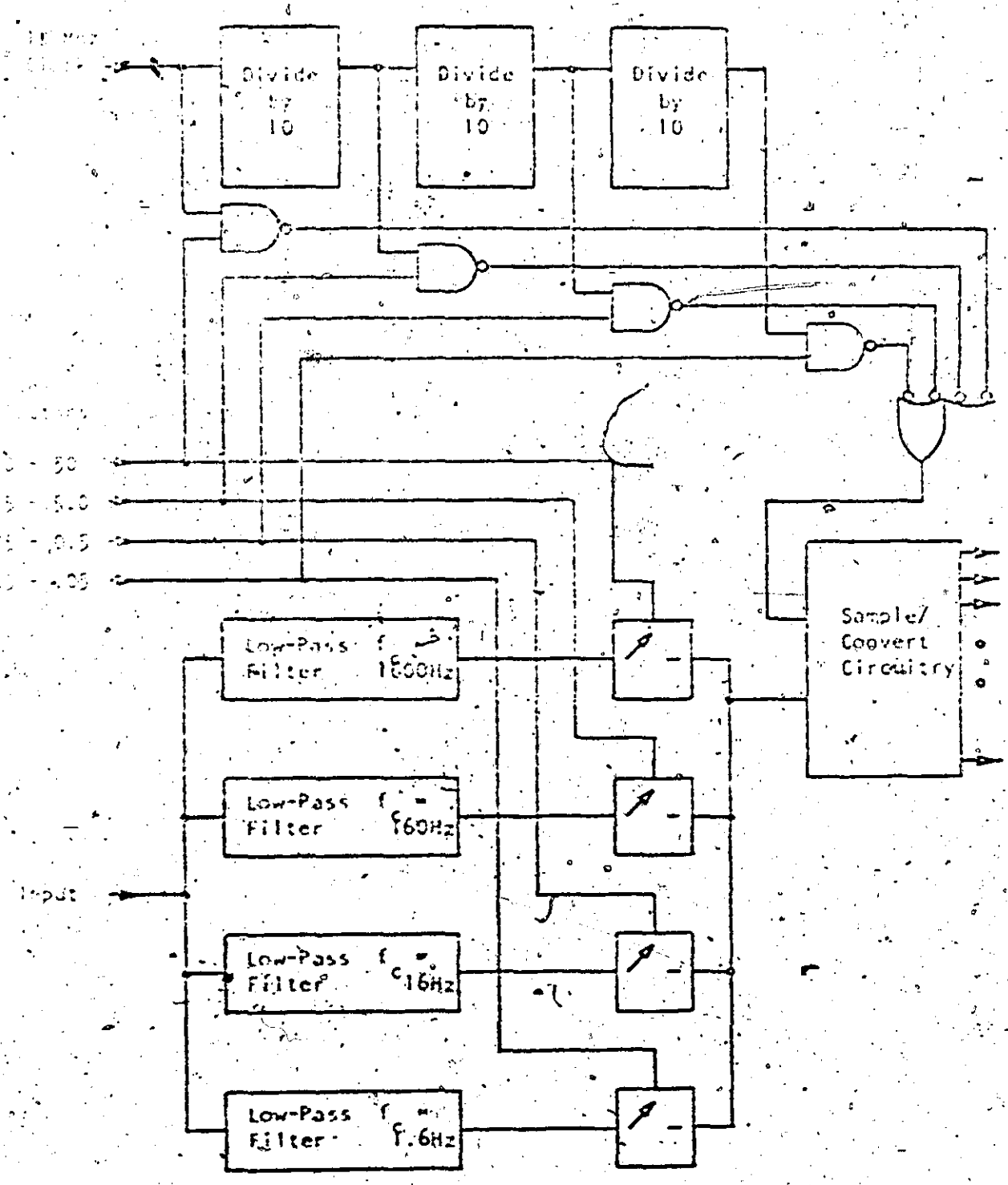


Figure 3-3 Decade Range Switching Input Sampling System

the first time derivative of the general expression for a sinusoidal waveform.

$$V_i = V_{i_p} \sin 2\pi ft \qquad (3\text{-}8)$$

where V_{i_p} is the peak input amplitude in volts and f is the frequency of the sine wave. Upon differentiating and setting the cosine term to 1, to yield the maximum rate, the result is as follows.

$$\left|\frac{dV_i}{dt}\right|_{max} = V_{i_p} 2\pi f \qquad (3\text{-}9)$$

For accurate analogue to digital conversion, the analogue voltage should remain essentially constant during the time that the conversion is taking place. "Essentially constant" is defined to be a change of one-half a voltage-equivalent lsb, or less. This term is expressed as

$$1/2(V_{i_p}/p), \qquad (3\text{-}10)$$

where p is the number of quantization levels and V_{i_p} is, in this case, the highest voltage the A/D converter will accept. T_c, the conversion time, is defined as the time required to accomplish the A/D conversion. The conversion time multiplied by the maximum expected rate of voltage change should be less than or equal to one-half the voltage-equivalent lsb.

$$T_c V_{i_p} 2\pi f \leq 1/2(V_{i_p}/p) \qquad (3\text{-}11)$$

This equation can be rewritten to show the upper bound for conversion time as a function of frequency, f, and the resolution states, p. It is assumed that the peak voltage of the input waveform equals the maximum input voltage of the A/D converter. Hence:

$$T_c = 1/4\pi f \qquad (3\text{-}12)$$

If f equals 5 kilohertz and p is 1000, T_c is 15.9 nanoseconds. This is much too short a time in which to complete the A/D conversion process. However, the sampling rate is 10 kilohertz which allows 100 microseconds between samples. The use of a sample-hold module [8] in addition to the basic A/D converter enables the conversion process to be completed during the 100 microsecond period, thus circumventing the conversion time restriction.

Figure 3-4 illustrates the operation of a typical sample-hold module. It operates in essentially two modes; a sample or track mode and a hold mode. During "sample" the output follows the input as a unity gain voltage follower and during "hold" the output retains the voltage present at the module's input at the initiation of the "hold" command. Figure 3-5 shows expanded detail of the two mode-to-mode transitions. When the mode is changed from hold to sample, a certain time must elapse until the output begins to track the input within a specified accuracy. This accuracy is generally 0.1% and it is reached after 10 microseconds or less. Following the opposite transition, from sample to hold, is a smaller delay referred to as the aperture time, T_a. This is the time between the actual mode control transition and the point where the output stops following the input. T_a is usually on the order of 10 nanoseconds. There is also a droop effect evident in the output during hold of about 50 microvolts per microsecond. It is during this interval that the A/D converter performs its conversion and its input, now the sample-hold module's output is essentially constant. The change in voltage due to droop effect over the 50 microseconds required for A/D

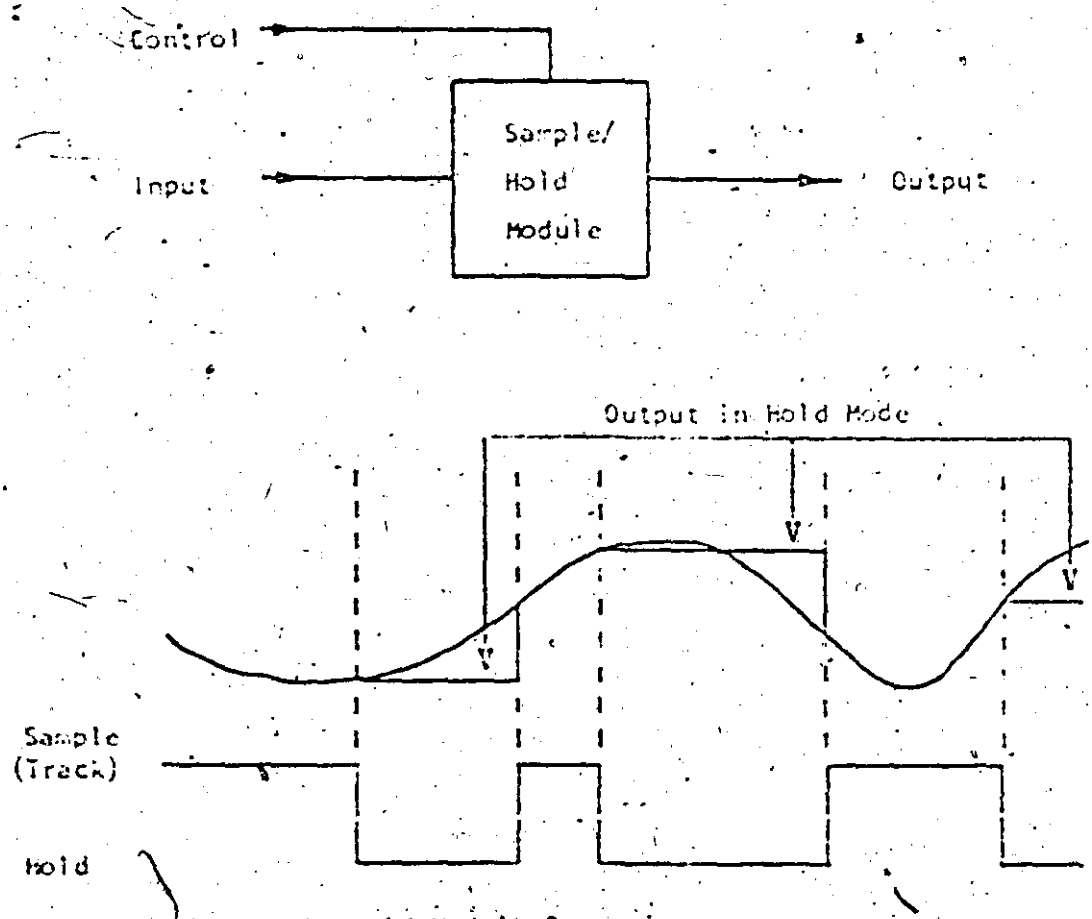


Figure 3-4 Sample-Hold Module Operation

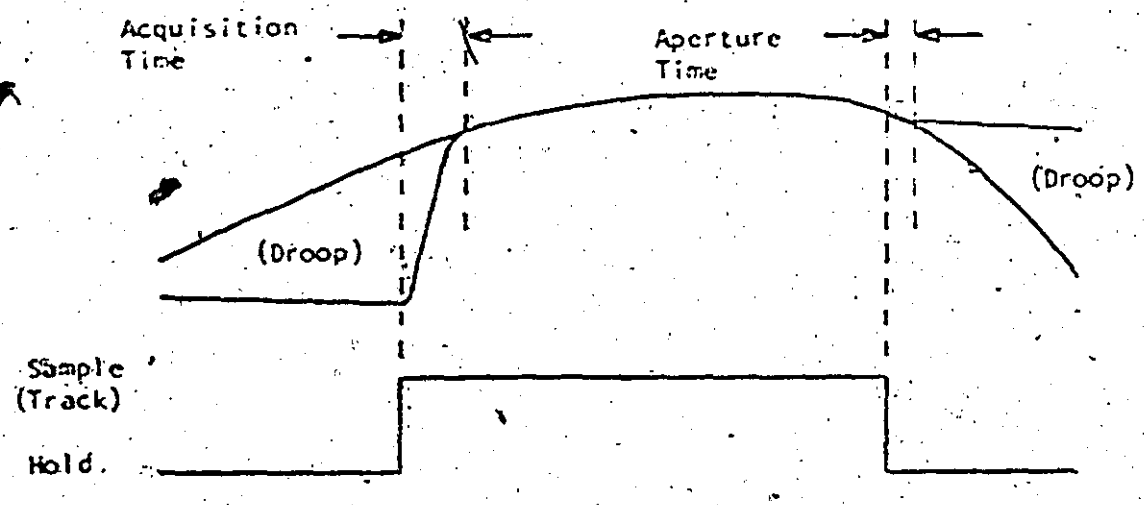


Figure 3-5 Sample-Hold Mode Transition Detail

conversion to be completed is insignificant. Figure 3-6 contains the specifications of a representative sample-hold module available from Datel Systems Inc., Canton, Massachusetts.

To optimize the performance of the input sampling and conversion system the sequence and timing of the various operations must be arranged to minimize the contribution to final error made by each operation. The maximum sampling rate at which the complete process must be cycled is 10 Kiloherts, which allows 100 microseconds for one cycle. The A/D converter used requires approximately 30 microseconds to convert to 0.1% resolution. This leaves 70 microseconds which is divided into two segments, as illustrated in Figure 3-7. This timing diagram shows that a full 20 microseconds is allotted for the hold mode to stabilize before the A/D conversion is initiated. When the conversion is complete, the sample-hold module is immediately commanded to track the input signal. Tracking can continue in the case of the highest sampling rate for a full 50 microseconds before the hold command occurs again. For a lower sampling rate the duration of the track mode is of course longer.

Two monostable multivibrators and two dual input NAND gates are all that are required to implement this timing and sequencing scheme. Figure 3-8 illustrates the circuit diagram. The initiate pulse which starts the data conversion process sets both a latch and the first monostable. The output of the latch commands the sample-hold module to hold. The first monostable provides the time delay required for the hold mode to settle, at the end of which the second monostable supplies the start pulse for the A/D converter. When the A/D conversion is complete, a "done"

SPECIFICATIONS

ELECTRICAL

Analog Input:

Analog input voltage range . . . 0V to +5V FS, 0V to +10V FS, ±5V FS, ±10V FS

Input overvoltage . . . . . ±15V (max.) with a recovery time of 500 nsec

Input source current . . . . . 10 ma max.

Mode control input . . . . . DTL or TTL compatible, positive logic

Status	Input Code	Vinput Min.	Vinput Max.
Sample	"0"	0V	+0.8V
Hold	"1"	+2.0V	+5.5V

Rise and Fall time 10 nsec to maintain aperture time spec's

Analog Output

Output voltage range . . . . . 0V to +5V, 0V to +10V, ±5V, ±10V

Output current . . . . . ±5 ma

Dynamic Characteristics:

Bandwidth . . . . . DC to 500 KHz (max.) full power @ 3 db point

Acquisition time . . . . . 100 nsec (max.) to ±0.1% of FS of input signal

Aperture time . . . . . 10 nsec max. (8 nsec delay, 2 nsec jitter)

Settling time . . . . . 1 μsec (max.) to ±0.1%

Hold decay rate . . . . . 50 μv @ 1 μsec

Output slewing rate 30V/μsec

Performance:

Gain . . . . . +1.00 Max. to +0.999 Min

Accuracy (@ 25°C) . . . . . ±0.025% of FS

Linearity . . . . . ±0.01%

Temperature coefficient . . . . . ±30 ppm/°C

Long term stability . . . . . ±0.05%

Input power requirements . . . . +15 VDC @ 35 ma
−15 VDC @ 35 ma

PHYSICAL-ENVIRONMENTAL

Operating temperature range . . 0°C to +75°C.

Storage temperature range . . . . −55°C to +85°C

Relative humidity . . . . . Up to 100% non condensing

Size . . . . . 2" L x 1" W x 0.4" H plug-in module

Pins . . . . . 0.020" round gold plated 0.250" long minimum

Case material . . . . . Black diallyl phthalate, per MIL-M-14

Weight . . . . . 2 oz.

Model SHM-2 sample and hold module is fully encapsulated and features dual in-line pinning compatibility (i.e., 0.100" grid pin spacing and 0.600" between rows of pins), permitting direct plug-in to AUGAT, CAMBION, ELCO, etc., circuit boards.

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Figure 3-6 Sample-Hold Module Specifications for SHM-2, Datel Systems, Inc.

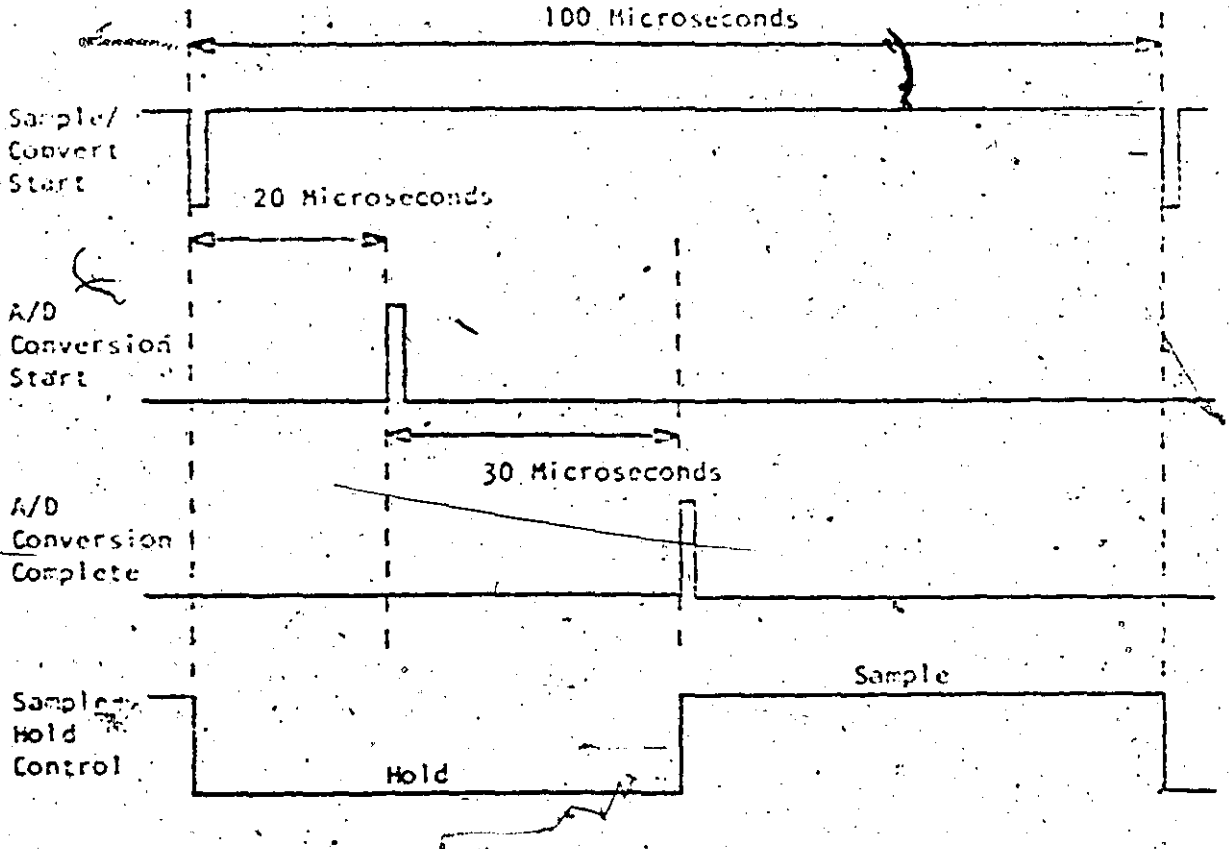


Figure 3-7 Sample-Hold Module and A/D Converter Sequence and Timing Diagram

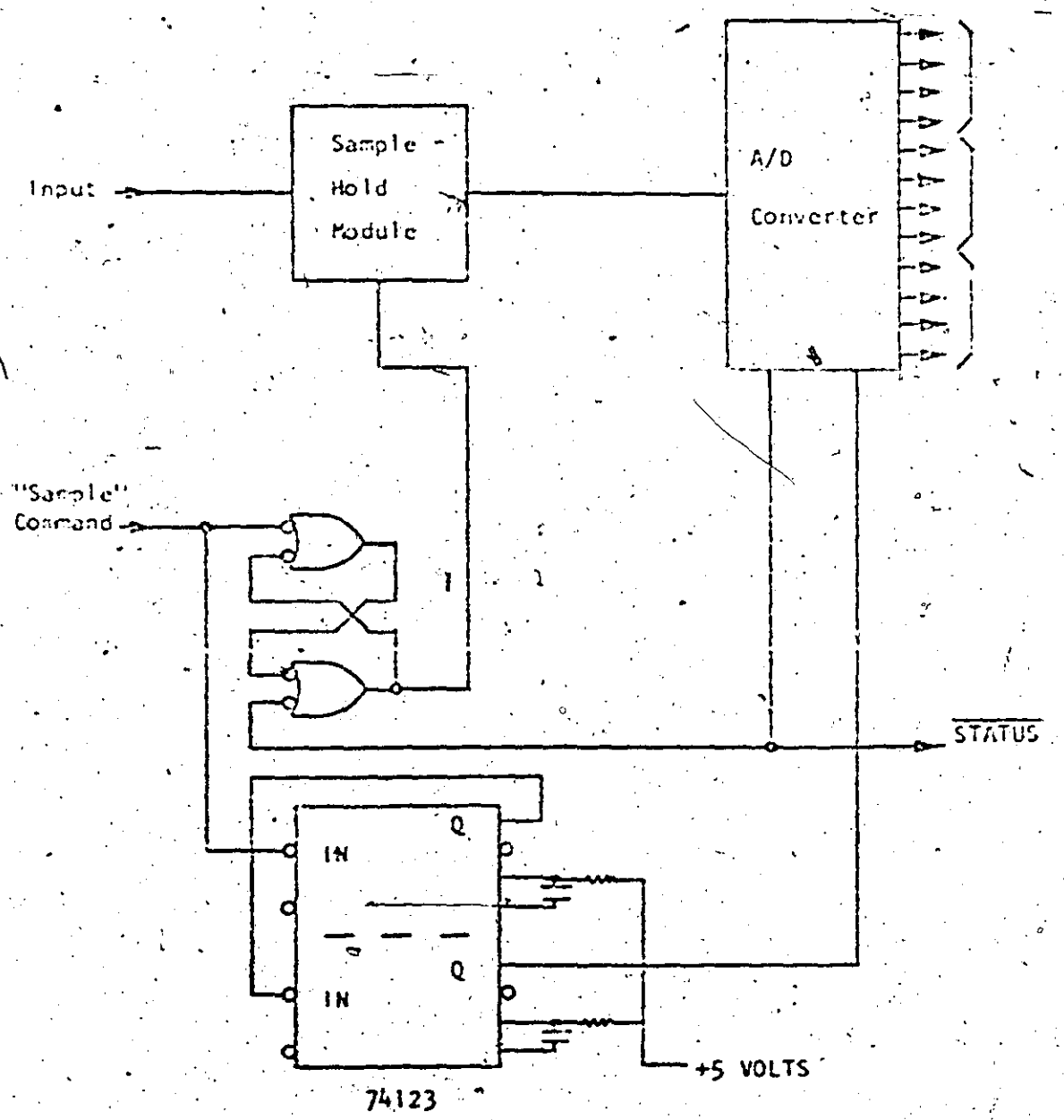


Figure 3-8 Sample/Convert Control Circuitry

pulse is produced which resets the latch and returns the sample hold module to the sample or track mode. The data conversion cycle could be re-initiated less than 50 microseconds after this point, but this would result in a higher sampling rate which is unnecessary in this analyzer system. The A/D converter "done" pulse is made available so that it can be used to initiate accumulator operations.

The operating characteristics of any voltage sampling and conversion system are determined by the speed and accuracy specifications of the individual components used in the system. The system presented here could sample at a higher frequency than 10 kilohertz due to the short acquisition time of the sample-hold module (about 100 nanoseconds). The contribution made by the addition of the sample-hold module is that the conversion time requirement expressed by T_c in equation (3-11) is, in effect, satisfied by the sample-hold module's aperture time specification, T_a. The figure listed for T_a of 10 nanoseconds is sufficiently less than the 15.9 nanoseconds calculated for T_c. The jitter figure of 2 nanoseconds listed in Table 3-2 is also very good. This means that the uncertainty in the location of each sample is only 2 nanoseconds, which is only 0.002% of the shortest sampling period of 100 microseconds.

3.5. Summary

It has been shown that the input voltage sampling system requires the use of a low-pass filter and a sample-hold module in addition to the basic A/D converter. The resulting sampling system produces valid digitized samples over the specified ranges of Walsh analyzer operation. The maximum

sampling frequency of 10 kilohertz allows the analysis of periodic waveforms with fundamental frequencies of 50 Hz for signals of unknown harmonic content.

The sampling system features decade range switching over the following ranges: 50 Hz - 5.0 Hz, 5.0 Hz - 0.5 Hz, 0.5 Hz - .05 Hz, .05 Hz - .005 Hz. This maintains the number of samples produced in each range between 200 and 2000 inclusive.

CHAPTER 4

DUAL ARITHMETIC PROCESSOR

4.1 Introduction

The Walsh analyzer design reported by Siemens [9] implemented the instrument equations,

$$A_s = \frac{V_{max}}{pH} \sum_{h=1}^{H} |Q_h| \, sgn\,(Q_h) \, cal(s,\theta)_h \qquad (1\text{-}9)$$

$$B_s = \frac{V_{max}}{pH} \sum_{h=1}^{H} |Q_h| \, sgn\,(Q_h) \, sal(s,\theta)_h \qquad (1\text{-}10)$$

by a combination of parallel and serial accumulators. The quantized data sample, Q_h, was fed first to a parallel accumulator which provided an overflow output at a count of 256. This accomplished division by p, the number of quantized states of the A/D converter used in that version of the analyzer. This overflow output, either positive or negative, depending on the Walsh function and the sample sign, was then fed to a signed accumulator which operated in the serial mode. The contents of this accumulator represented the Walsh coefficient and contained a factor of (H/V_{max}). Hence, it was necessary to employ a separate counter to record the number of samples taken during the calculation cycle of the Walsh analyzer and then to divide the accumulator contents by H after the calculate cycle was completed.

The arithmetic processor design presented here uses serial

counting methods exclusively. It is shown that the division by H can be performed by the combination of a variable modulus counter and a signed accumulator. The number H is made available immediately at the termination of the Walsh analyzer's timing cycle by a counter which is clocked at the sampling rate. Special timing circuitry assures that the counter's final state is exactly equal to the number of samples that will be made during the following calculate cycle. The term H then determines the count modulus of the signed accumulator and the Walsh coefficient is available immediately at the termination of the calculate cycle. Since this coefficient has not been divided by , it is in the same BCD fractional format as the digital word produced by the A/D converter. It is therefore simple to normalize the waveform input voltage in relation to the V_{max} of the A/D converter.

4.2 Number of Samples (H) Counter

The sample-convert system described in Chapter 3 receives its "convert" command at a 10 kilohertz rate when the Walsh analyzer is operating within its highest (50 Hz - 5.0 Hz) range. This 10 kilohertz signal is derived from the 10 megahertz system clock by a divide-by-1000 counter. After the convert command occurs, a finite time is required to complete the conversion. It is necessary to simulate this time delay during the analyzer timing cycle to produce an accurate count of H.

4.2.1 Sampling Rate Generator

Figure 4-1 illustrates the sampling rate generator and includes the 3 additional divide-by-10 counters needed to implement the range switching over 4 decades. The highest sampling rate, 10 kilohertz, is derived directly from the divide-by-1000 counter series. The next lower sampling rate, 1 kilohertz, is obtained by dividing down the system clock frequency by one additional decade counter. Switching the divide-by-1000 counter to the output of the second decade counter provides the sampling rate used in the third analyzer range, and so on. The decade range-switching divider circuits are situated at the input of the divide-by-1000 counter series so that its output can be permanently connected to the pulse shaping network. This network has an additional input which is connected to the generate/clear control input. Hence, the first "convert" command pulse is produced immediately when the sampling rate generator is turned on. The two pulse shapers within this network feed one output via an OR gating function which is connected to the H counter and then to the sample-convert system during the timing and calculate cycles, respectively. All of the counter modules shown in Figure 4-1 are asynchronous decade counter, number 7490A.

In controlling the sample rate generator, it is necessary to clear its counter at the end of any cycle. This assures that the "convert" commands always occur at the same point in time in relation to the start of the cycles.

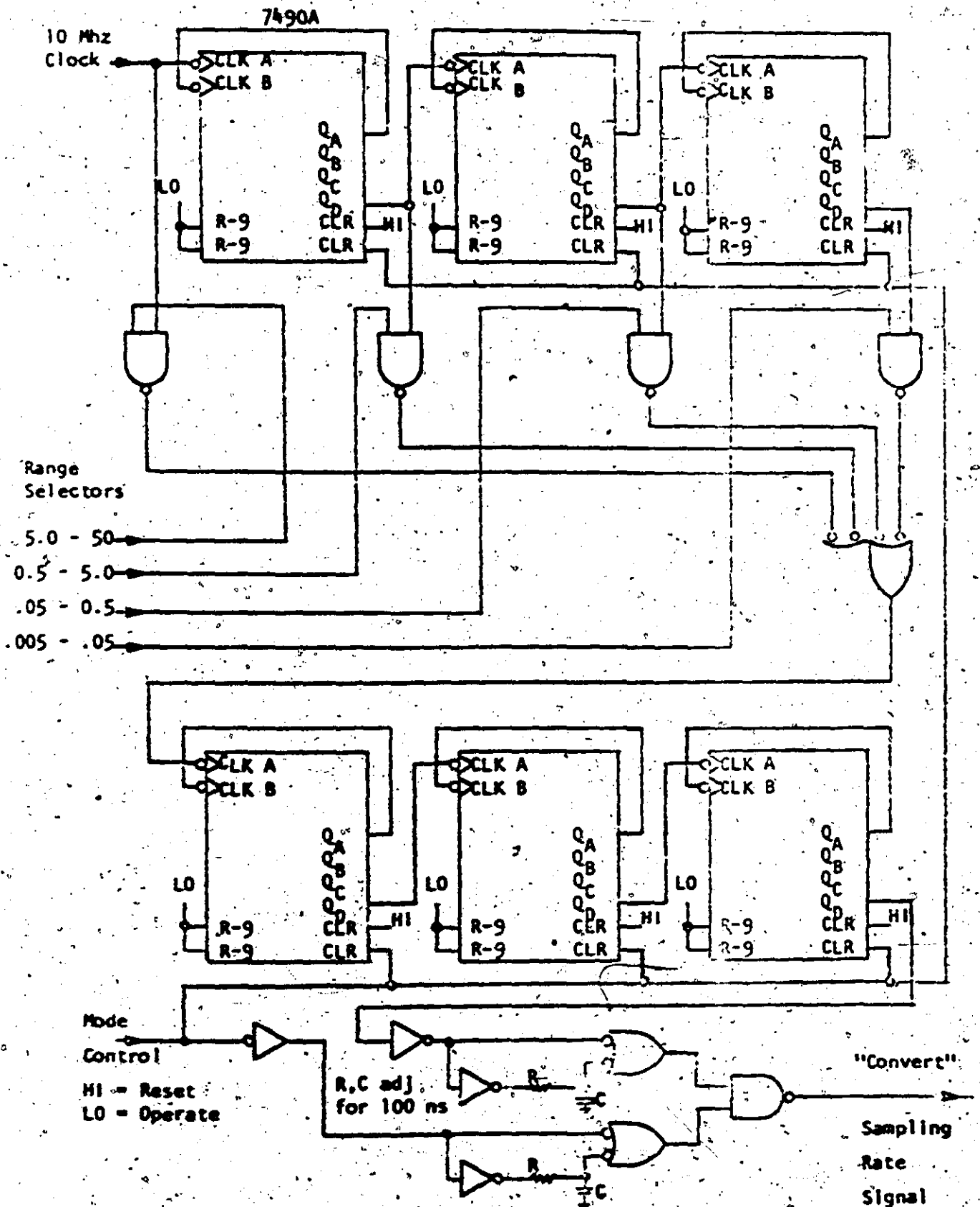


Figure 4-1 Sampling Rate (f_s) Generator.

4.2.2 Sample Counter Implementation

The highest number of samples that can be made in any operating range of the analyzer is calculated by dividing the range's low frequency limit by its sampling rate. For example, the low frequency limit of the top range is 5[illegible] Hz. Dividing this into 10 kilohertz yields 2000 samples. The result at the high frequency limit (90 Hz) is 200 samples. The decade range-switching feature of the Walsh analyzer maintains the number of samples between these two limits for all 4 operating ranges. Therefore, 4 decade counters are sufficient to count and store the number of samples, N.

Figure 3-7 of Chapter 3 illustrates the time delay necessary to complete an A/D conversion. A total of 50 microseconds is required after the "Convert" command is received for the digital word to become available at the converter's output. Figure 4-2, which contains a diagram of the complete sample counter, includes a dual monostable multivibrator, type 74123, to simulate the conversion time delay. The first half of the module provides the 50 microsecond delay and the second half regenerates the "convert" pulse which clocks the decade counters. Thus, a "convert" command which occurs too near the end of period T to result in calculable data will not cause an erroneous count in the H counter during the timing cycle.

The H counter is cleared prior to the start of the timing cycle by the analyzer control logic. When the timing cycle terminates, the sampling signal is no longer received by the Sample Counter. The counter is then

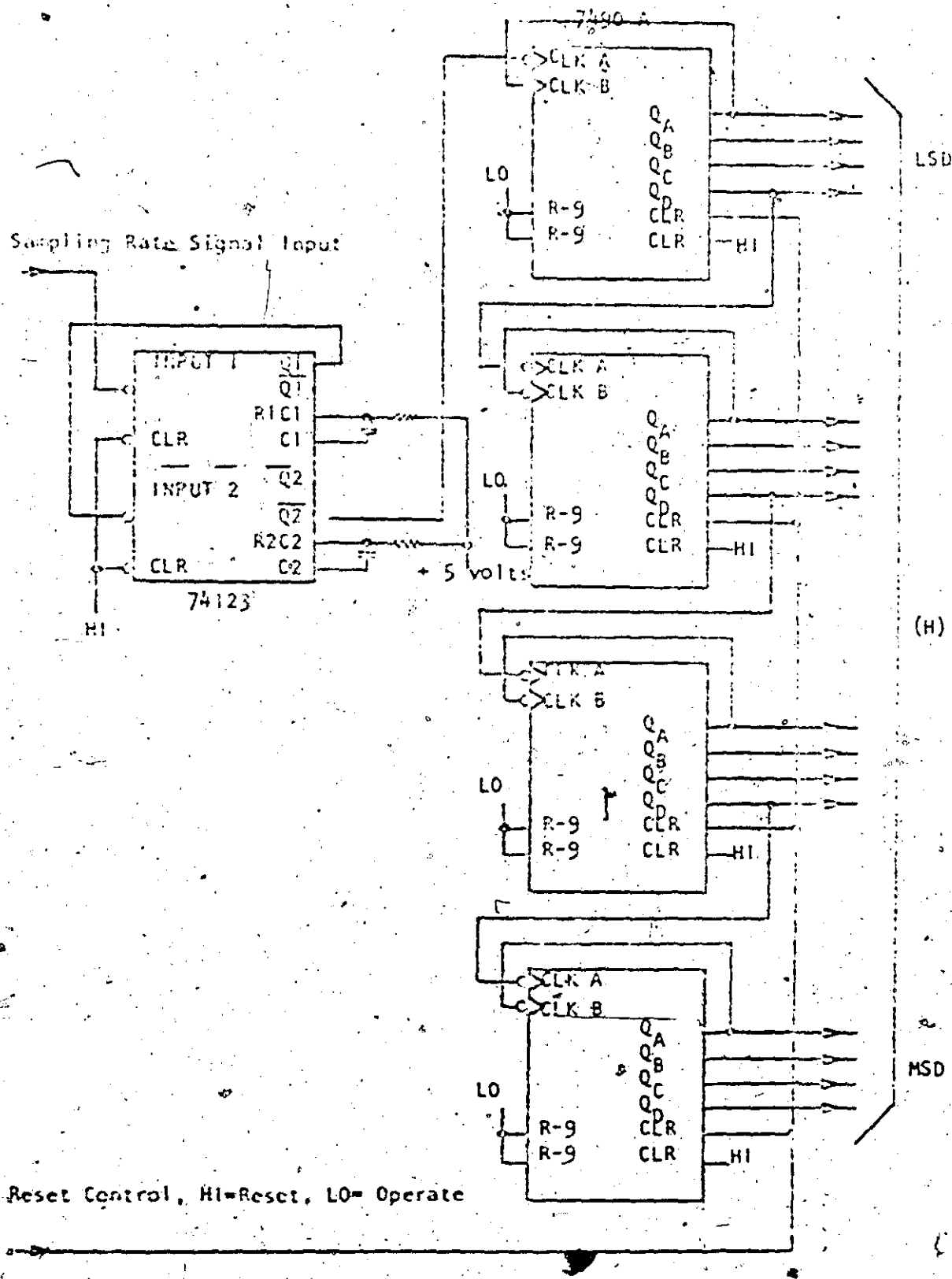


Figure 4-2 Sample Counter (H)

held in its final count-state making H available for the following calculate cycle or cycles.

The decade counter modules shown in Figure 4-2 are again type 7490A and they are wired for BCD operation. The set-to-9 inputs are unused.

4.3 Sample Pulse Generator

When the A/D conversion operation for a given sample is completed, the digital word is available at the converter's output as parallel data. This data, in the case of the 12-bit BCD A/D converter employed here, is presented as 3 digits on 3 groups of 4 lines. A voltage polarity output is also provided. Ignoring the polarity, there are 1000 possible output states ranging from 000 to 999. It is the purpose of the Sample Pulse Generator to convert this parallel data into an equivalent number of pulses which are to be counted in serial accumulators. The desired pulse train is produced by loading the A/D converter's output data into a 3-decade BCD down counter and clocking the counter down to the all-zero state. The number of clock pulses needed to do this is therefore equal to the converter's output code and appropriate gating feeds the clock pulses to the accumulator circuits. Figure 4-3 illustrates the Sample Pulse Generator diagram. The preset or load and countdown operation is handled efficiently by the 74190 MSI counter module. Its internal wiring diagram and characteristic timing details are reproduced in Figure 4-4. The 74190 provides a max/min

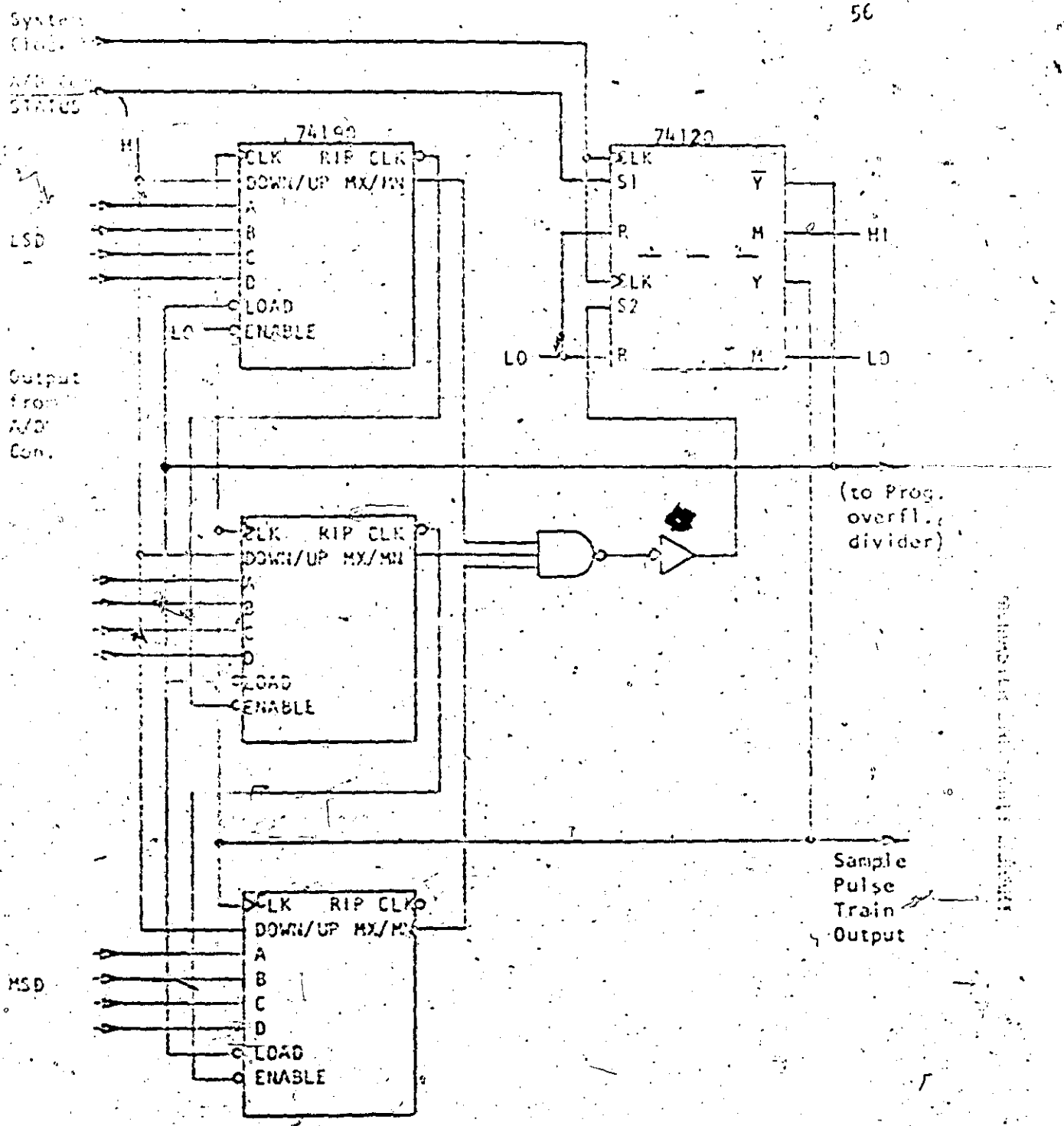
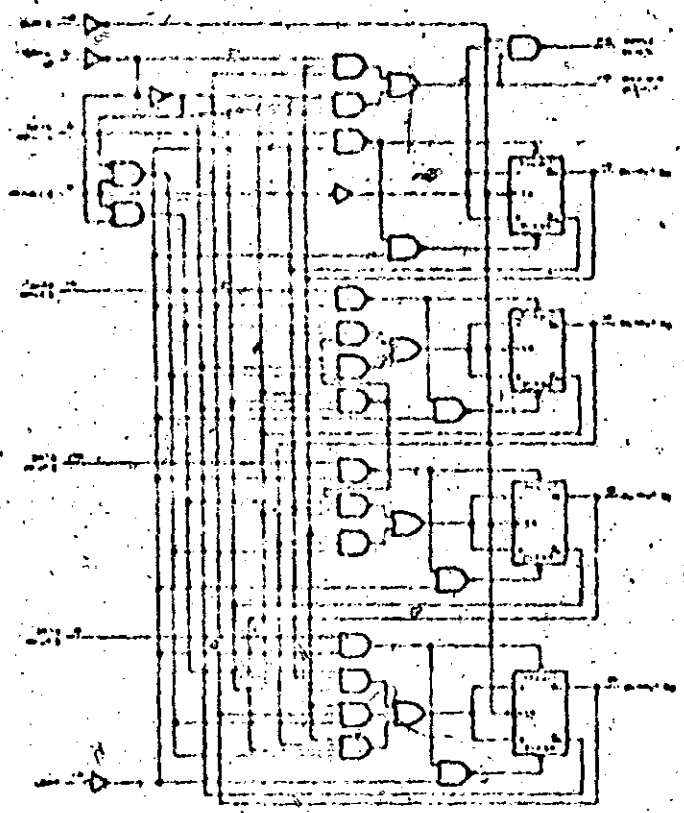


Figure 4-3 Sample Pulse Generator

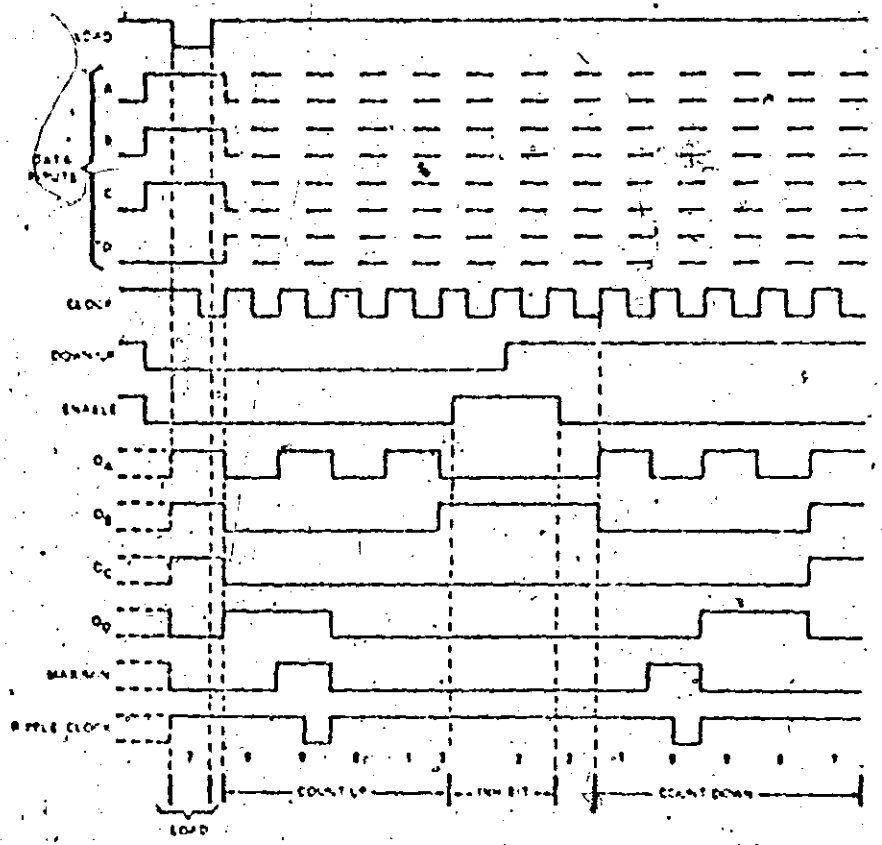


a. Internal Circuitry

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (max), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



b. Timing Details

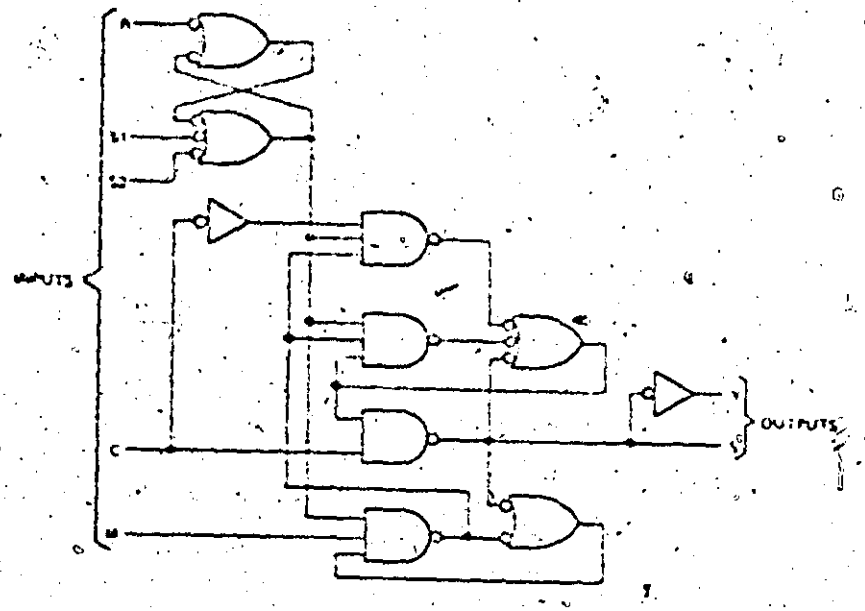
Figure 4-4 BCD Synchronous Presettable Up/Down Counter: Type SN74190

output signal as soon as the zero state is reached in any counter stage. A zero state in all 3 counter stages is detected by a NAND gate whose output stops the clock pulses.

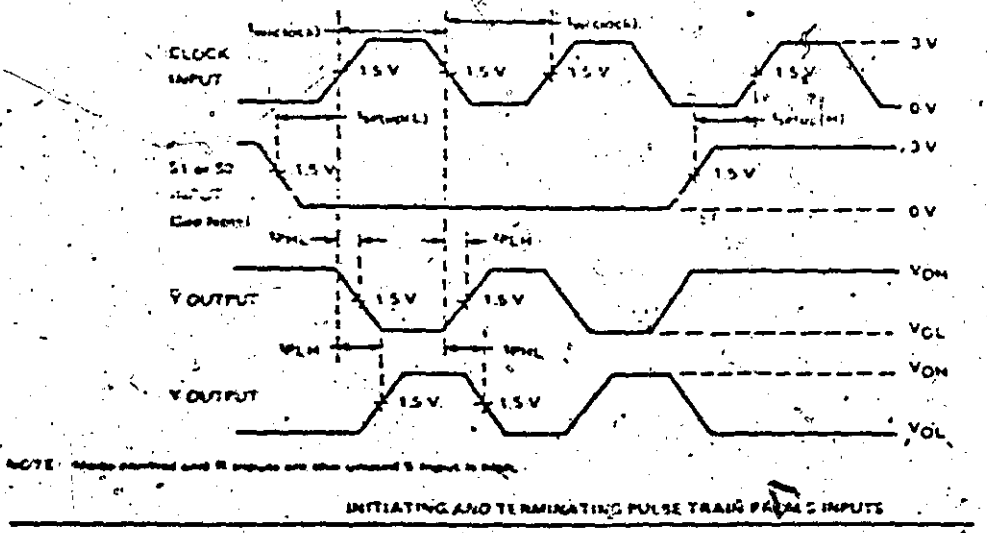
Proper clock pulse gating is provided by the SN74120 Dual Pulse Synchronizer. Its internal circuitry and characteristic timing details are reproduced in Figure 4-5. The pulse synchronizer makes use of latching circuitry which assures that only full clock pulses are gated through to the counters. This precludes the possibility of erratic counter operation due to shortened clock pulses. The pulse synchronizer has two modes of operation, controlled by pin M; when M is HI only one clock pulse will be passed by the internal latches, when M is LO, a pulse train will be passed which is terminated by the Set/Reset inputs.

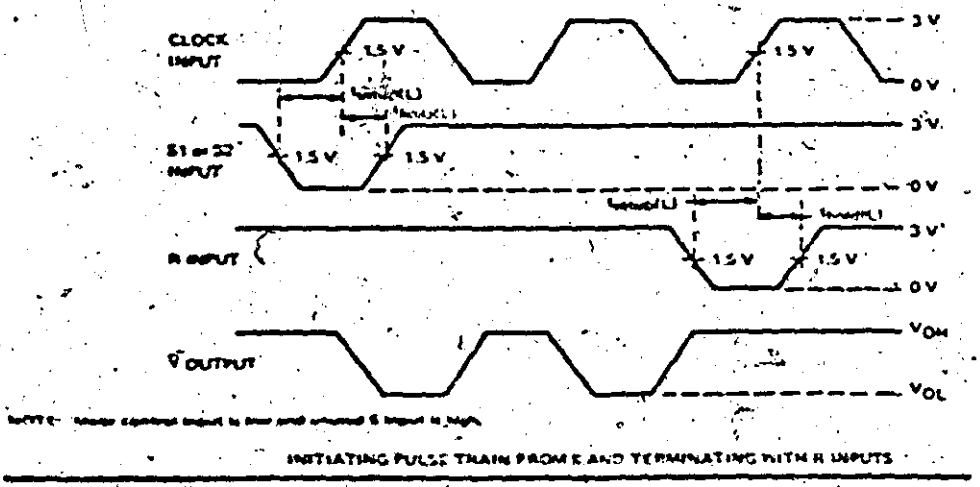
The single-pulse mode is used here to load the A/D converter output into the 74190 counter modules. When the $\overline{\text{STATUS}}$ output of the converter goes from HI to LO thus giving the "done" indication, one clock pulse is fed to the load control pins of the three 74190 counters. Another load pulse can be produced only after the $\overline{\text{STATUS}}$ output returns to the HI state and then repeats the HI to LO transition. This sequence occurs when another data sample is processed by the sample-convert system.

The pulse train mode is used to provide the counter clock pulses which are also the Sample Pulse Generator output pulses. The control input to this section of the dual pulse synchronizer is derived from the 3-input NAND gate which senses the all-zero state of the 3 BCD counters. When the counters receive the load command, their output pins assume the same state as the A/D converter output. Therefore, the all-zero state



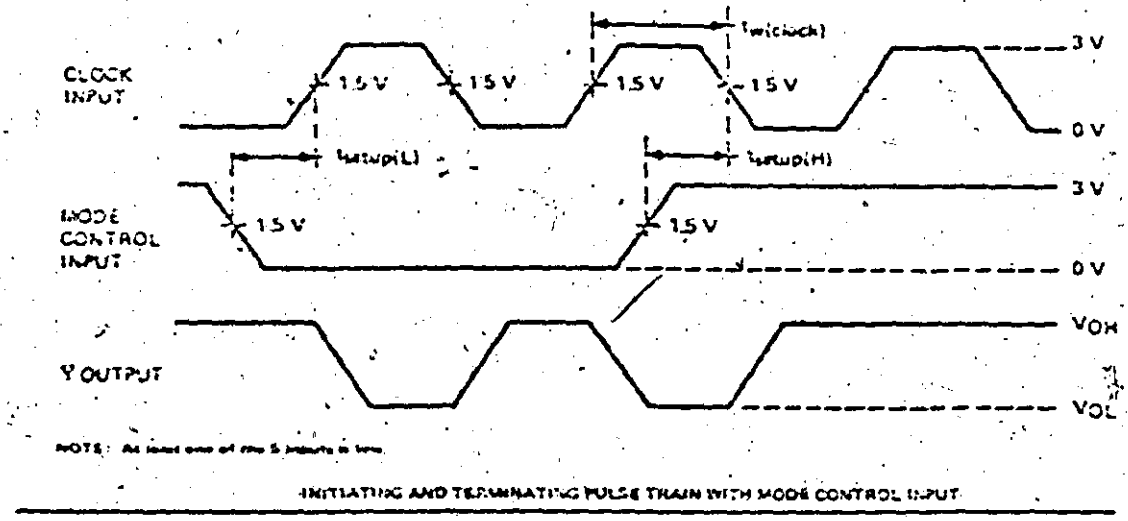
a. Internal Circuitry



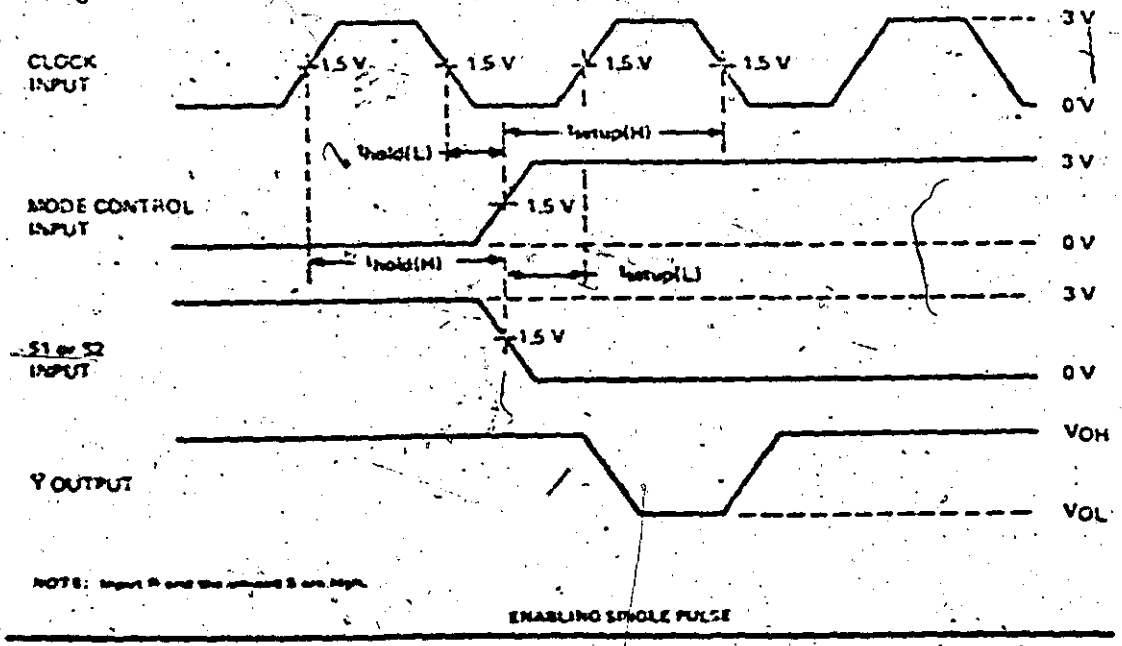


b. Timing Details

Figure 4-5 Dual Pulse Synchronizer: Type SN74120



INITIATING AND TERMINATING PULSE TRAIN WITH MODE CONTROL INPUT



ENABLING SINGLE PULSE

b. Timing Details (continued)

Figure 4-5 Dual Pulse Synchronizer: Type SN74120

is no longer detected by the NAND gate and the control input to the pulse synchronizer goes from HI to LO. This initiates the clock pulse train which is stopped after the preset or loaded number of pulses have returned the counters again to the all-zero state. The output of the NAND function then goes HI, terminating the pulse train. The counters then remain at zero until new data is loaded from the next sample.

The Sample Pulse Generator does not need any clearing operations. There are no CLEAR inputs on the 74190 counters; they always begin counting at the state determined by the A/D converter output.

Figure 4-6 contains a timing chart illustrating the important timing sequences which appear in the Sample Pulse Generator.

4.4 Programmable Accumulator-Divider

The accumulator stages receive their serial input data in the form of a counted pulse train. Accompanying this is a sign indication which is the calculated product of the sample polarity and the Walsh function. There are two accumulators which operate independently to process the sal and cal coefficients. The input stages of each accumulator make use of variable modulus counting techniques to provide division by H, the number of samples. Both these stages and the coefficient readout stages which follow comprise a dual signed accumulator which provides also the polarities of the final coefficient values. All counting and gating circuits employed in the accumulators are easily capable of functioning at the speeds required by the Walsh analyzer operation.

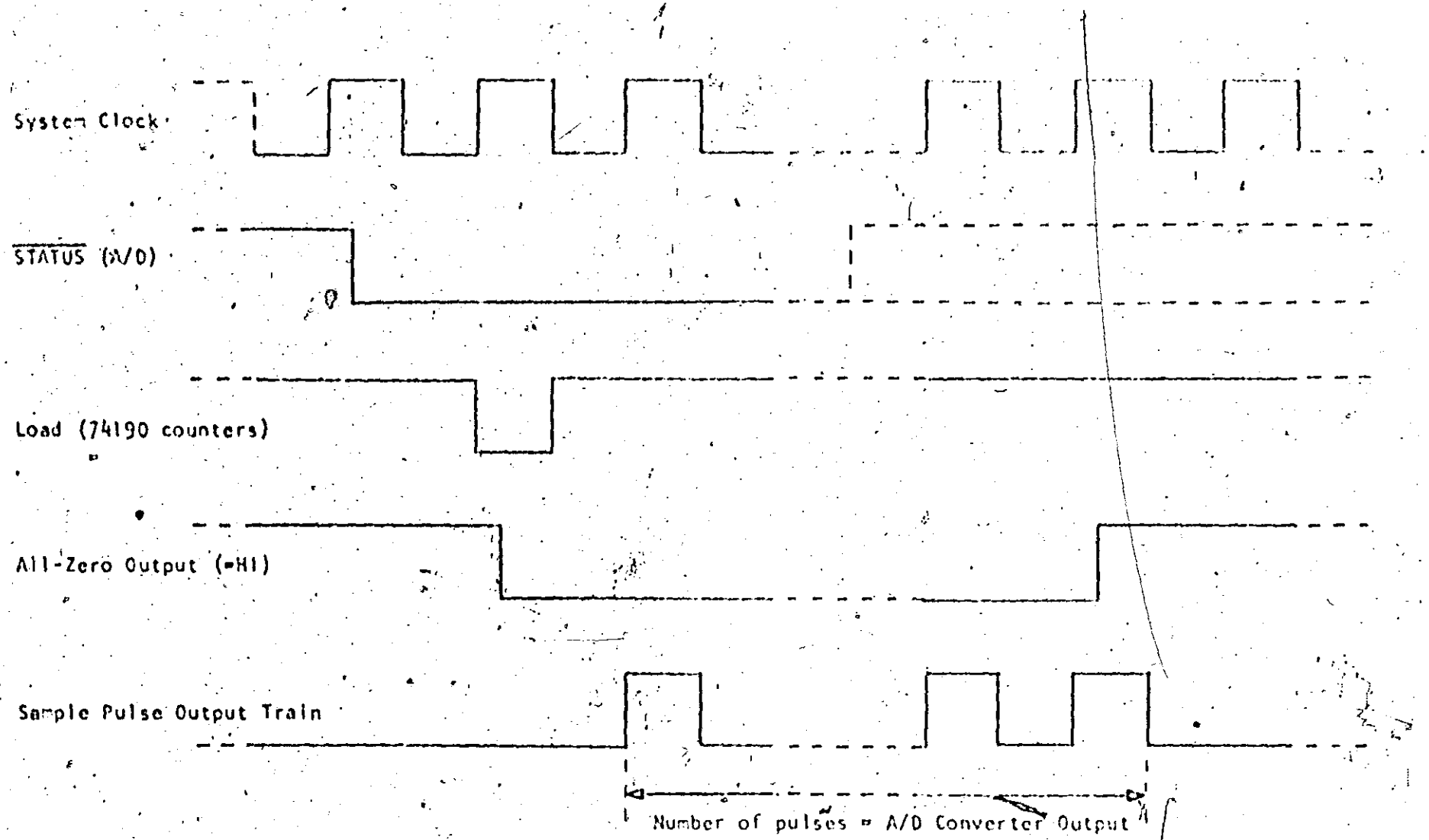


Figure 4-6 Sample Pulse Generator Timing Sequence

4.4.1 Signed Accumulator

The signed accumulator used in the Dual Arithmetic Processor is fundamentally the same assembly as that used by Siemens [10]. It consists primarily of a BCD up/down counter module for each decade of accumulator capacity. Also necessary are a latch and auxilliary gating to provide sign information. Figure 4-7 illustrates the operation of the signed accumulator. The input to the signed accumulator is, in general, a pulse train of variable length. Accompanying the input pulse train is a sign indication. Since the repetition rate of the pulses is constant, the magnitude of the count in the accumulator will change at a constant rate. Hence, the accumulator content as represented in Figure 4-7 changes along the same slope, either positive or negative. When the pulse train stops, the accumulator content remains fixed. Also apparent in Figure 4-7 is the fact that all points at which each successive pulse train is initiated are spaced equally in time. This places an upper bound on the number of pulses that can occur in any given pulse train.

The accumulator count-states equidistant from the zero line all represent the same state of the decade counters. The negative region in the accumulator count-state diagram is derived by combining the accumulator sign with the contents of the decade counters. Therefore, when the counters count down to zero, the count mode is changed and they then count up. The counters can also pass through zero in the up-count mode when all counters overflow at 9999 to 0000. In this instance the accumulator content sign does not change.

The sloped lines which indicate the change in the counter state

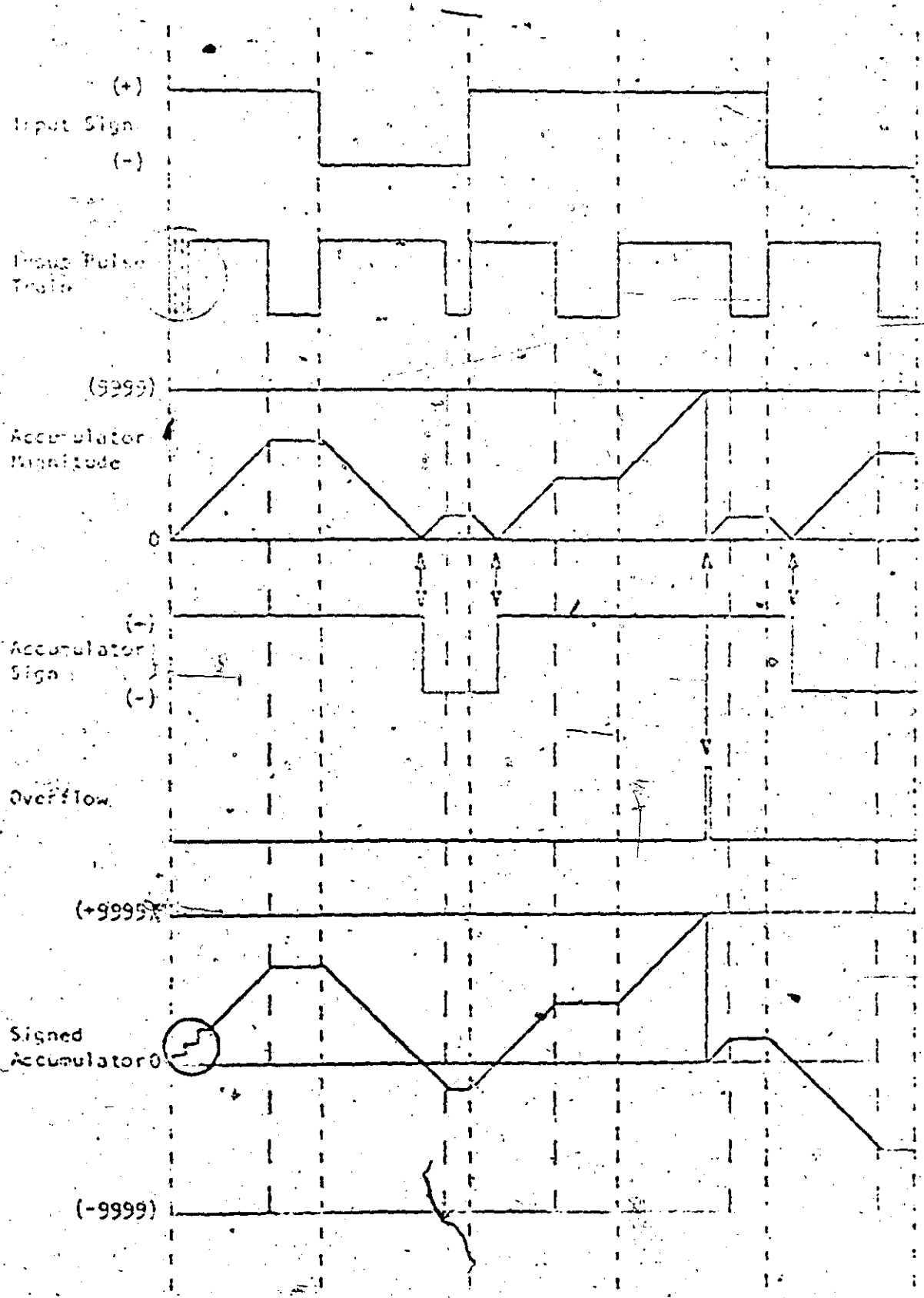


Figure 4-7 Signed Accumulator Operation

during the pulse train are actually not continuous, but represent discrete state changes as illustrated in the magnified section of Figure 4-7.

The type 8285 MSI up/down counter module conveniently provides all the counting functions necessary in the accumulator. Reproduced in Figure 4-8 is the internal circuitry of the 8285. This circuitry provides the interstage connections necessary to cascade decade sections for multi-stage counters. The CARRY OUT connections also provide control for the sign generator. The interstage connections for a 4-decade counter are shown in Figure 4-9. Parallel clocking is employed and the CARRY OUT of the first stage provides the COUNT ENABLE input of the following 3 stages. The sign generator suggested by Signetics Corporation [11] is illustrated in Figure 4-10. The sign generator combines the input count sign (SGN), the COUNT ENABLE and the CARRY OUT of the final counter stage to determine the sign of the accumulator contents and also the count mode of the 4 decade stages. The logic function provided at the output of the sign generator is

$$U/\overline{D} = SGN \cdot P_+ + \overline{SGN} \cdot \overline{P}_+ \qquad (4\text{-}1)$$

where

$$P_+ = \text{"1"} \quad \text{for} \quad N_a \geq 0 \qquad (4\text{-}2)$$

$$P_+ = \text{"0"} \quad \text{for} \quad N_a \leq 0 \qquad (4\text{-}3)$$

N_a = number of counts in counter

SGN = "1" for positive input count

SGN = "0" for negative input count

Listed in Table 4-1 is an example of the count sequence produced by the 8285 module and the sign generator.

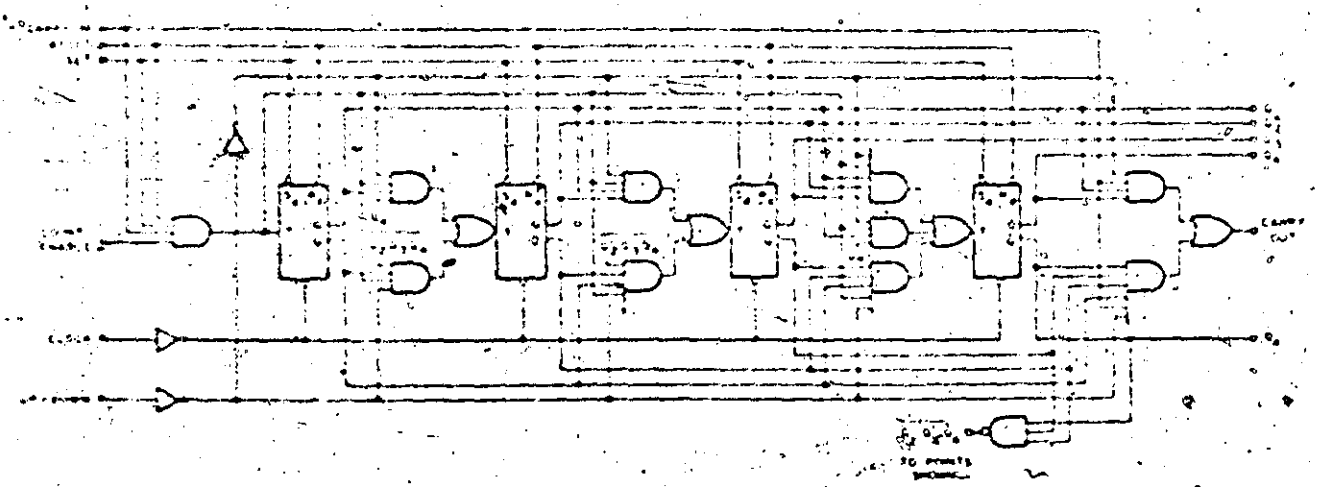


Figure 4-8 BCD Synchronous Up/Down Counter Type: 8285

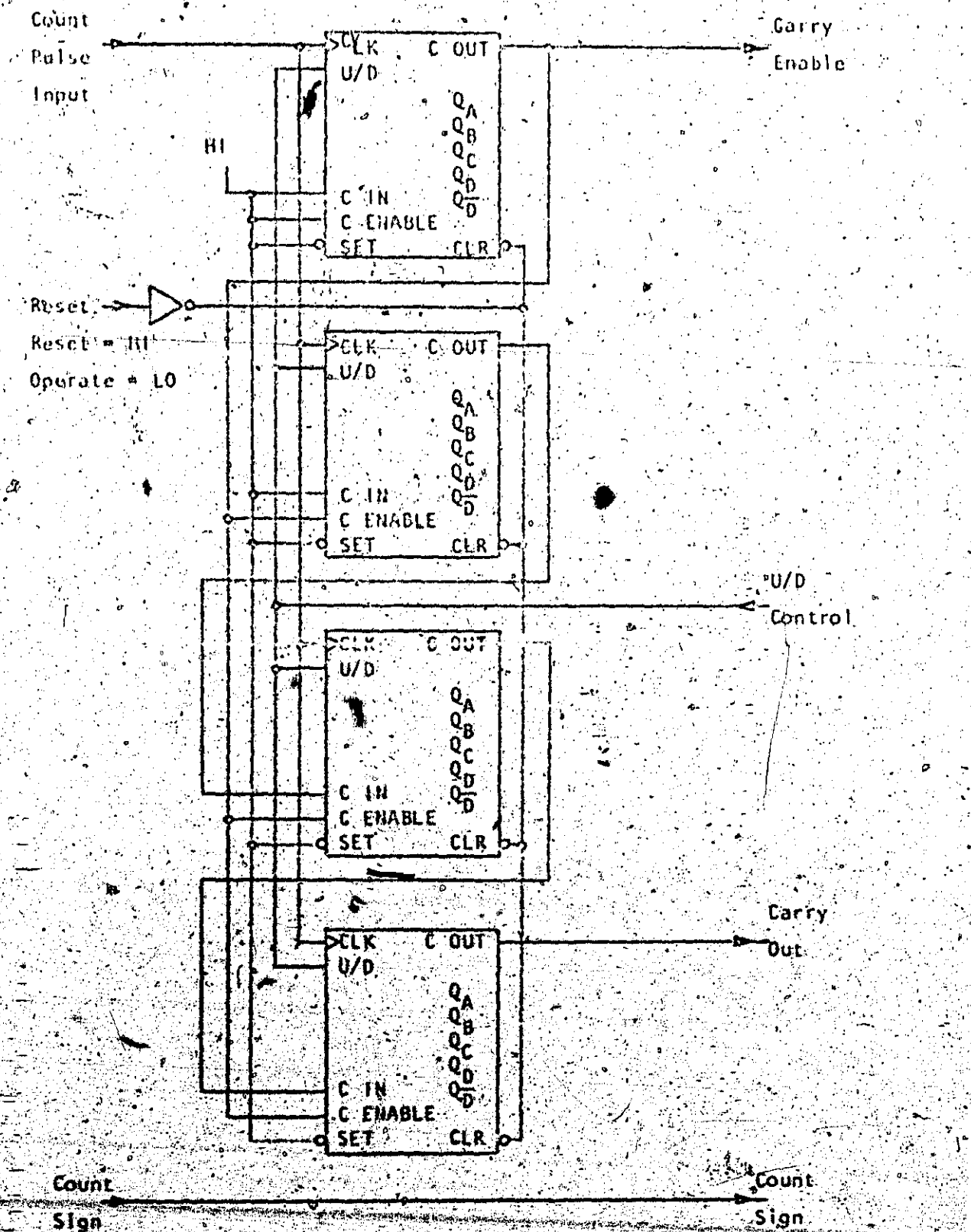


Figure 4-9 Four-Decade BCD Up/Down Counter

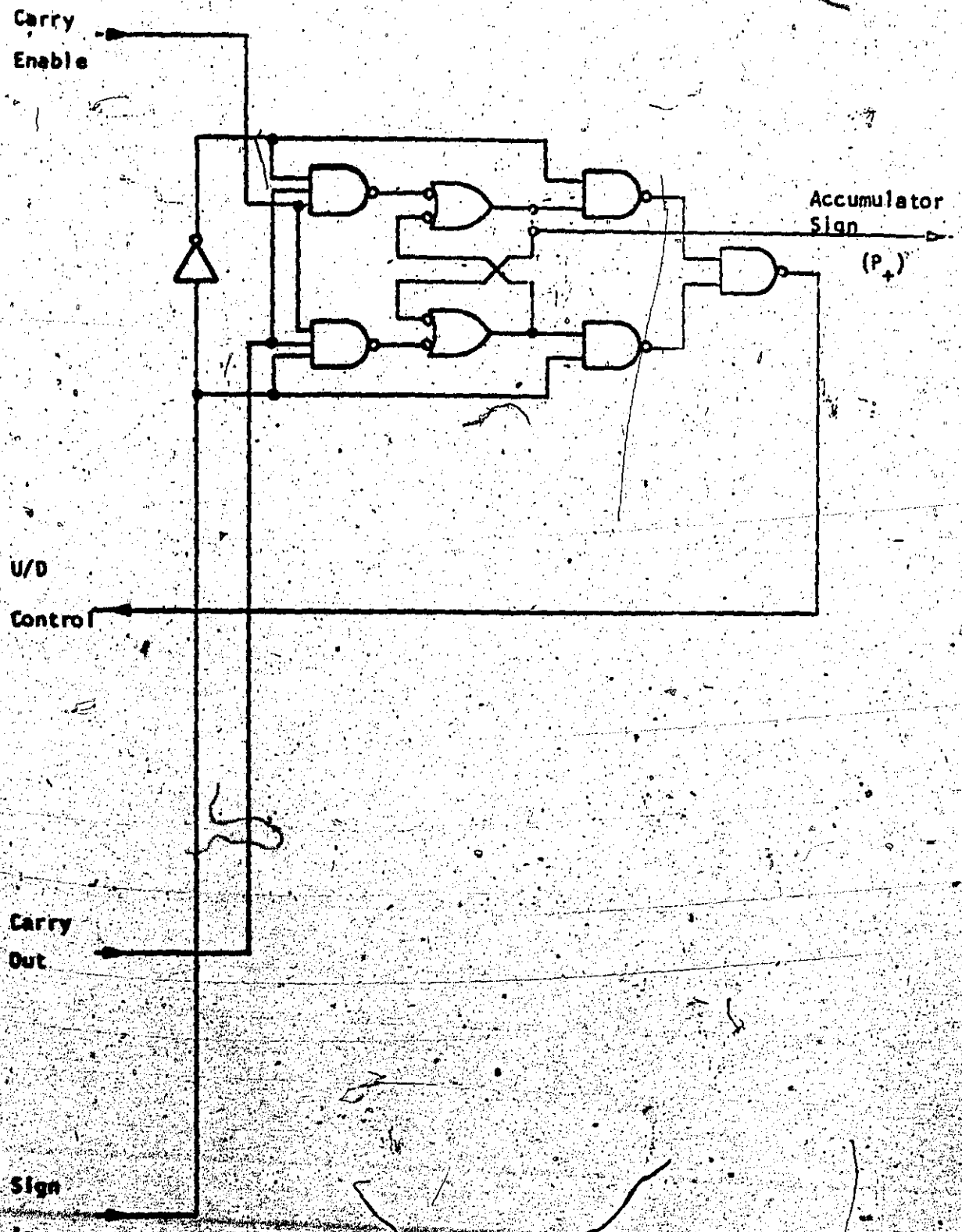


Figure 4-10 Accumulator Sign Generator

SGN	Carry Out $C_c \cdot C_i$	P_+	$U/\overline{D}$	Clock Pulse	N_2 (BCD)	Decimal
0	0	1	0	0	0 0 1 1	+3
0	0	1	0	1	0 0 1 0	+2
0	0	1	0	2	0 0 0 1	+1
0	0	1	0	3	0 0 0 0	+0
0	1/0	0	1	4	0 0 0 1	-1
0	0	0	1	5	0 0 1 0	-2
0	0	0	1	6	0 0 1 1	-3
1	0	0	0	7	0 0 1 0	-2
1	0	0	0	8	0 0 0 1	-1
1	0	0	0	9	0 0 0 0	+0
1	1/0	1	1	10	0 0 0 1	+1
1	0	1	1	11	0 0 1 0	+2
0	0	1	0	12	0 0 0 1	+1
0	0	1	0	13	0 0 0 0	-0
0	1/0	0	1	14	0 0 0 1	-1

SGN = "1" for positive input count
SGN = "0" for negative input count

Table 4-1 Signed Accumulator Count Sequence

Because of the high speed capability of the 8285, the accumulator will accept input clocking pulses at a 25 megahertz rate, typically.

4.4.2 Programmable Overflow Division

The 4-stage decade counter described in the previous section can be viewed as a modulo 10,000 counter [12]. This means that the count states from 0000 to 9999 represent 10,000 distinguishable states. If more than 10,000 pulses are fed to the counter it will overflow after state 9999, return to 0000 and continue counting. This effectively accomplishes division by 10,000. The 8285 HSI decade counter stages contain the logic required to detect the overflow state and this is available as the CARRY OUT signal. Proper interconnection of the stages will yield an overflow indication for any number of decade stages. It will be shown in this section that the addition of comparator logic and pulse shaping circuits to the basic signed accumulator makes it possible to preset the count-state at which an overflow output will occur. This programmable division function provides division by H, the number of samples taken during the cycle, for any H. The term H is made available by the sample counter.

The Walsh analyzer's decade ranging system maintains H between 200 and 2000, inclusive, requiring 4 decade counters. Figure 4-11 contains an illustration of programmable overflow divider operation. Because the accumulator may overflow as a result of negative counts numbering more than H, there must be a negative region to the accumulator count-states. The accumulator sign thus becomes the overflow sign, which

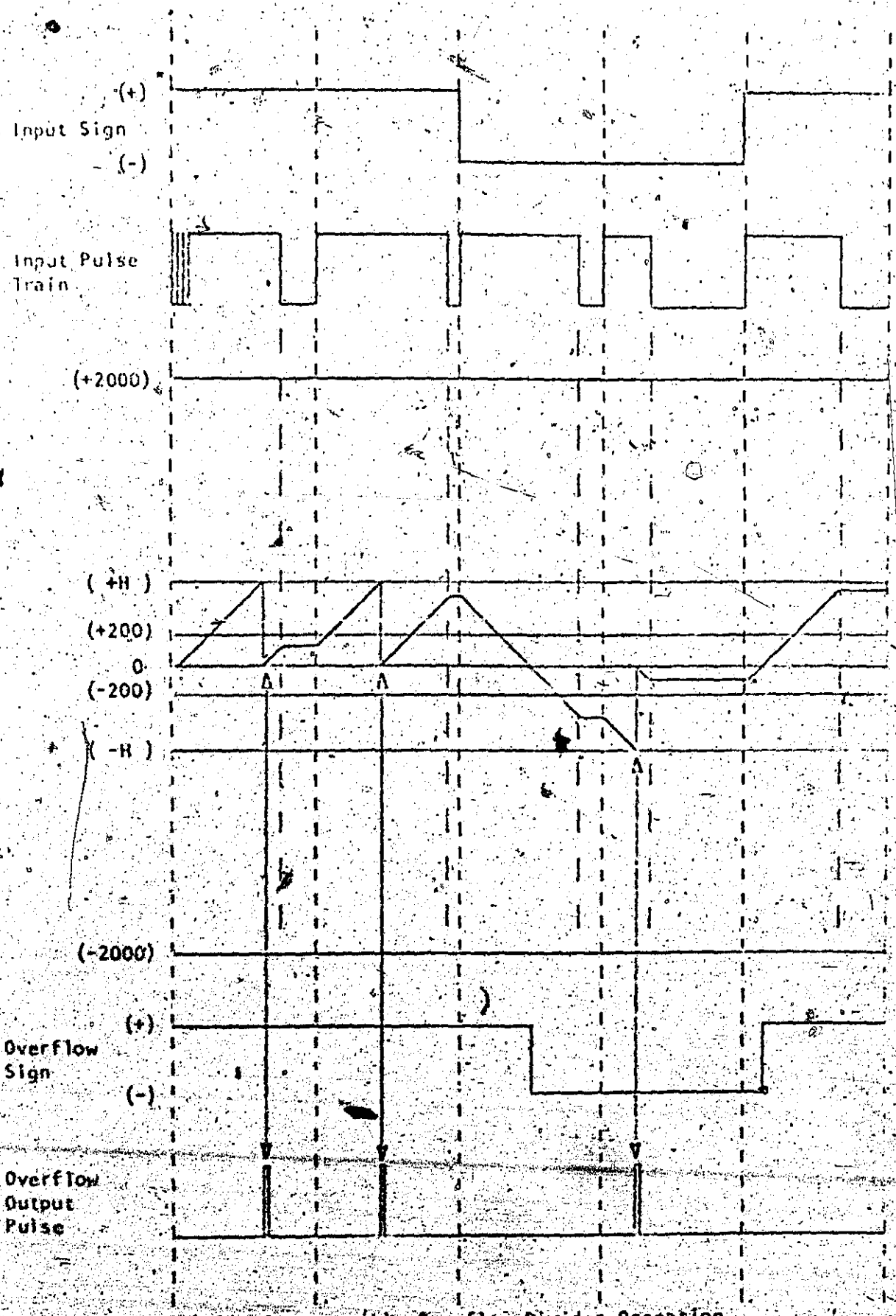


Figure 4-11 Programmable Overflow Divider Operation

is presented to the coefficient output accumulator along with the overflow pulses.

Special attention must be given to the reset-to-zero operation. Assuming H equal to 500 and the counters at 0000, an input pulse train of 500 pulses must produce one overflow pulse and return the counters to 0000. Positive input pulses will produce a positive overflow output. The last input pulse, number 500, produces a count-state of 500 in the 4 decade stages. The comparator detects equivalence between this counter-state and H and initiates operations which produce the overflow output pulse and reset the counters to zero. These operations must be completed with minimum delay to allow for the case of additional input pulses. The pulse number 501 would then advance the counters to 0001 and the system must be ready to accept this input pulse.

Equivalence between H and the counter state is detected by 16 EXCLUSIVE-NOR or comparator gates as illustrated in Figure 4-12. The comparator gates feature the open-collector output structure which is used to implement the wired-AND configuration. Thus the comparator output goes HI when equivalence occurs. The wired-AND connection is followed by an inverting buffer gate. The comparator gates are Schottky diode clamped, type 82S42.

Figure 4-13 illustrates the pulse shaping and latch circuitry which is required in addition to the sign generator discussed previously. A special monostable multivibrator is employed which features very short delay between the initiating transition provided by the comparator circuit and the output pulse. The diode and resistors provide reference voltages

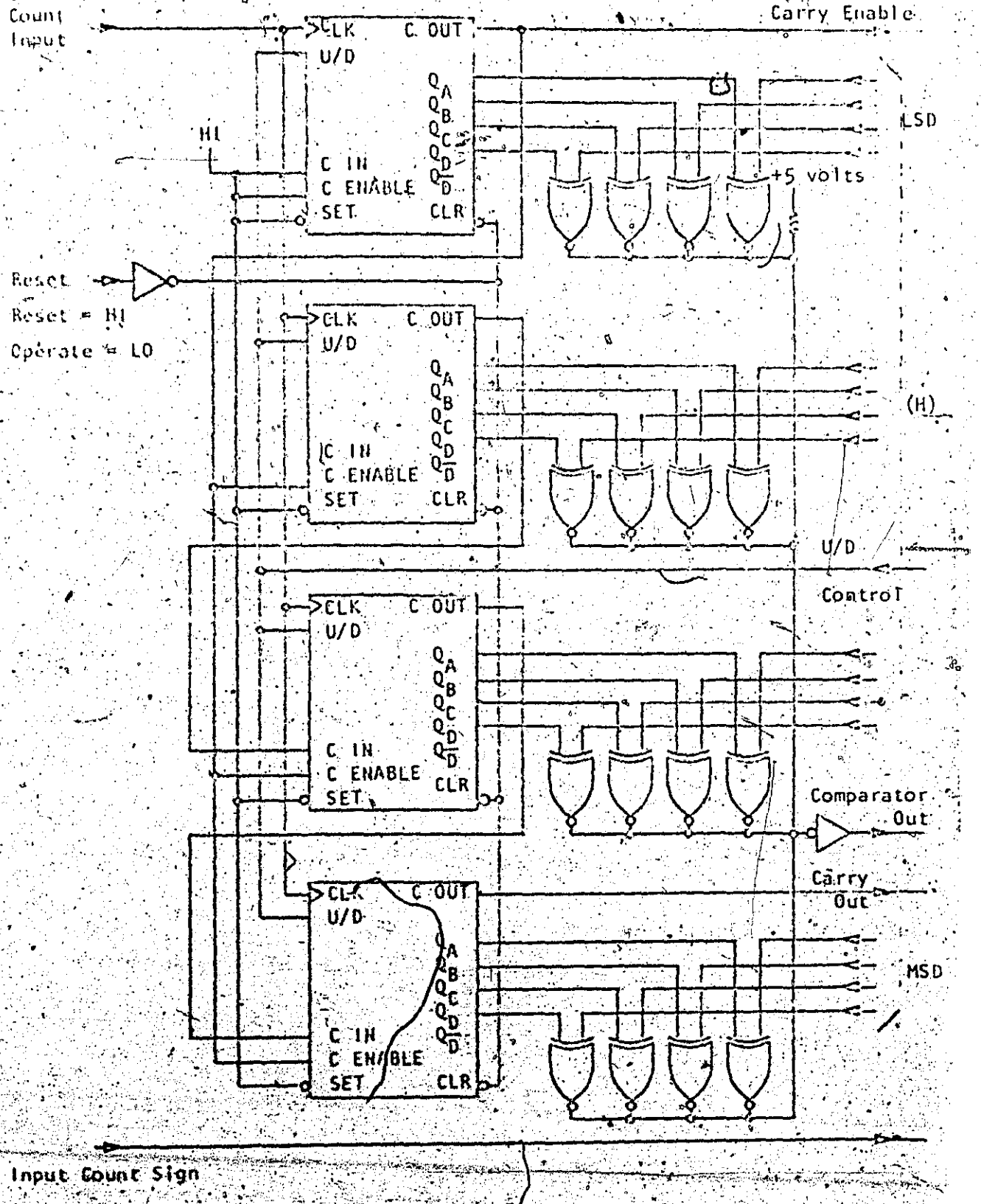


Figure 4-12. Four-Decade BCD Up/Down Counter with Comparator

which assure stable operation over normal temperature ranges. The monostable's delay is merely the propagation delay of the 3-input OR gate and the following inverter. R and C are adjusted for an output pulse of 40 nanoseconds.

The 8285 counter module provides a CARRY OUT signal according to the following expression:

$$\text{CARRY OUT} = \text{CARRY IN}\ (Q_1Q_4UP + \overline{Q}_1\overline{Q}_2\overline{Q}_3\overline{Q}_4\overline{UP})$$

When the 8285 is used in the programmable division accumulator, this signal is no longer sufficient to provide input to the sign generator. Therefore, the overflow output pulse also sets a latch whose output is OR'ed into the sign generator, as shown in Figure 4-13. Thus the sign generator latch is enabled at the programmed overflow count and can accept a change in input sign. The overflow latch is then reset at the first pulse in the next pulse train.

Also shown in Figure 4-13 is the D-type flip-flop originally used by Siemens [10] to store the product of the sample sign and Walsh function at the time the sample is taken. An EXCLUSIVE-NOR gate provides the product of the Walsh function and the sample sign. The sample convert command clocks the flip-flop. The following D-type flip-flop synchronizes the Programmable Overflow Divider input sign with the Sample Pulse Generator output. The Sample Pulse Generator's internal "load" or counter preset pulse (see Figure 4-3) is used to clock the second flip-flop.

The maximum speed at which the programmable overflow divider can operate is determined by the time the comparison and reset operations require. The delays involved are listed in Table 4-2. The total delay shown in the table indicates that the counters will be reset 78 nanoseconds

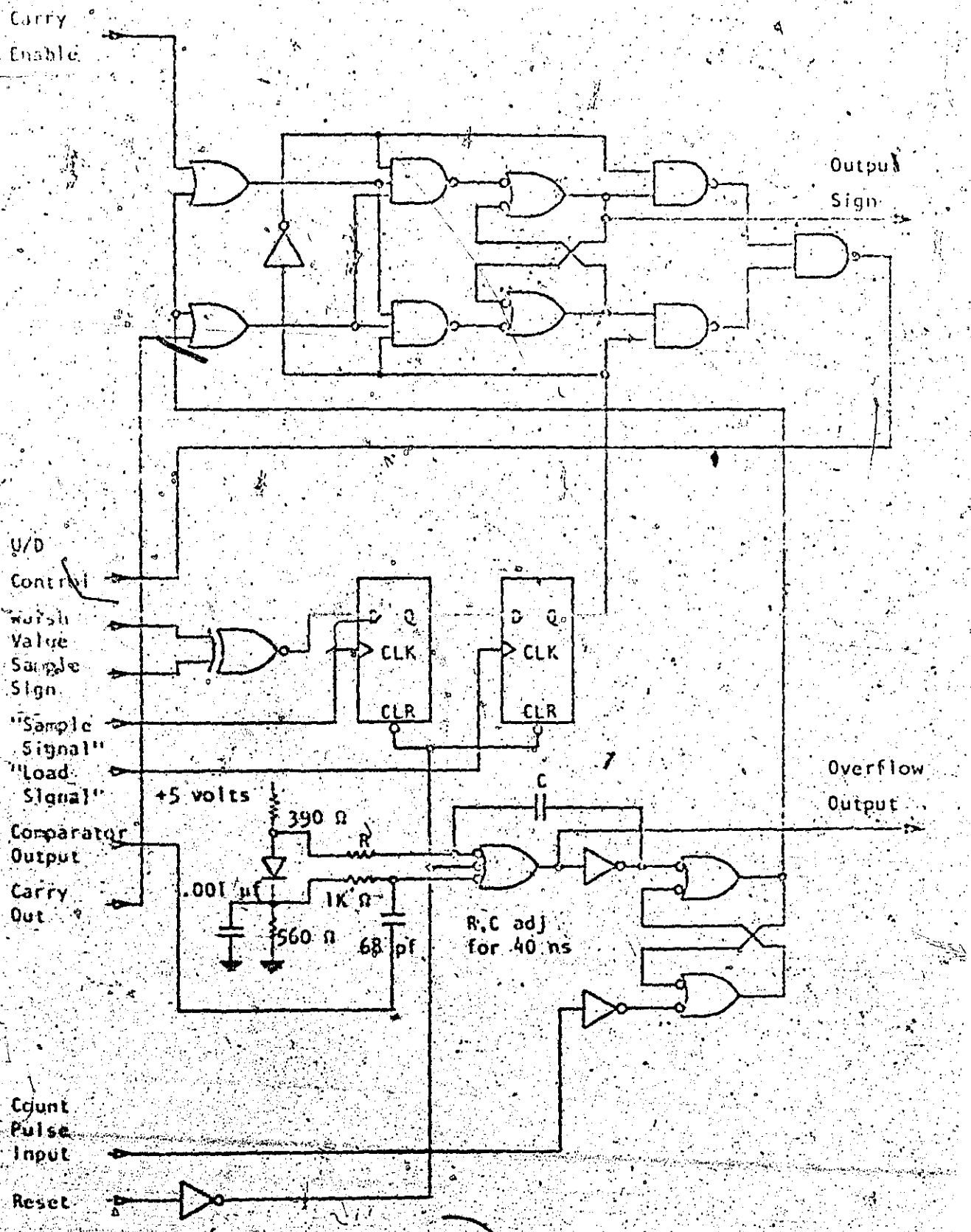


Figure 4-13 Programmable Divider Sign and Output Pulse Generator

Device	Type	Delay or Transition	Time
Counter	8285	clock to output	32 nanoseconds
EX-NOR	82S42	output (LO to HI)	9
Inverter	74S04	output (HI to LO)	5
3-Input NAND	74S10	output (LO to HI)	3
Inverter	74S04	output (HI to LO)	5
Counter	8285	reset to output	24
		+	
			78 nanoseconds

Table 4-2 Programmable Division Propagation Delays

after the count pulse transition which initiated the equivalent count state. The monostable's pulse width is 40 nanoseconds and will therefore last 14 nanoseconds after the counter is reset, bringing the total to 94 nanoseconds. This is consistent with an input pulse train repetition rate of 100 nanoseconds which corresponds to the system clock of 10 megahertz.

4.4.3 Coefficient Output Stage.

The Coefficient Output Stage consists of the signed accumulator illustrated in Figures 4-9 and 4-10, with the exception that only 3 decade counter modules are required. It accepts as its pulse input the overflow output of the preceding programmable overflow divider accumulator discussed in the previous section. The sign input also comes from the previous stage. The digital output format of the A/D converter used in the Walsh analyzer is a decimal fraction of 3 places. Because the programmable overflow divider stage divides the number of pulses by H for all H, this format is maintained in the output stage. It is sufficient to consider the case of a constant full-scale input to the A/D converter for the duration of a cycle. The input signal may be assumed positive. The total number of pulses produced by the Sample Pulse Generator will be HX999. Since this quantity of pulses will be divided by H, the coefficient output stages, namely the 3 decade stages of the final accumulator, will contain +999 at the end of the calculate cycle. Since the fractional format is maintained, the normalized coefficient value is actually +.999. A constant negative full scale input would yield -.999. Any time-varying input signal would

result in a coefficient value between these two boundary values.

4.5 Summary

The Dual Arithmetic Processor described in this chapter provides the Walsh analyzer with a calculation facility compatible with the resolution and speed requirements of its measurement input. Signed, normalized outputs representing both sal and cal coefficients are available immediately at the termination of the analyzer's calculation cycle for all decade ranges covering the input frequencies from 50 Hertz to .005 Hertz. The processor assembly needs only to be cleared at the beginning of the time period measurement cycle and to be given a single mode change signal at the beginning of the calculate cycle. The coefficient outputs are available for readout via visual display or for transfer to a memory for coefficient array storage. The number of samples taken during the calculate cycle is also available.

If the Walsh coefficient output is desired in the binary fraction format, it is necessary only to connect the output of a straight binary A/D converter to the processor's Sample Pulse Generator and to use hexadecimal up/down counter modules in the generator and coefficient output stages. No other modifications are necessary; the programmable overflow division stages may retain their BCD format so that H may be easily decoded for readout, if desired.

It has been shown that standard TTL devices may be used for most of the circuit functions employed in the Dual Arithmetic Processor. Schottky-clamped TTL devices are used only in the critical functions of

comparison and overflow/reset pulse generation. When Schottky devices become available to replace the presettable BCD or hexadecimal up/down counters, the maximum operating speed and/or resolution of the Dual Arithmetic Processor and hence the Walsh analyzer can be increased at least 2-3 times.

CHAPTER 5

PROGRAMMABLE WALSH FUNCTION GENERATOR

5.1 Introduction

Walsh function generators resulting from various design approaches have appeared over the past 10 years. An excellent overview of these designs is provided by Kitai and Yuen [13], in which both the theoretical basis and the practical implementation of representative designs are considered. Although any one of a number of the existing Walsh function generators could have been adapted for use in the Walsh Spectral Analyzer, additional design effort has produced a generator particularly suited to the analyzer's requirements. These requirements are listed as follows:

- serial programmable format
- dual orthogonal output
- low orthogonality error
- high speed operation
- simple initialization
- reset capability
- economical integrated circuit implementation

The serial programmable format means that the values of wal (s, t) are produced sequentially over the range of 0 to 1 of normalized t. The sequency order, s, is provided to the generator as an external input. The generator is further required to produce a dual orthogonal output, i.e., to produce the sal and cal functions for all s. There should be a minimum of orthogonality error between the sal and cal outputs and

minimum delay from the generator's input clock pulse to the output [illegible] state. The generator should operate well into the megahertz region and its control requirements should be straightforward and compatible with other analyzer circuitry.

The serial programmable format requirement can be satisfied by an array generator if means are provided to select the Walsh function desired. This approach was taken by Siemens [14]. Significantly fewer integrated circuits are required when the Walsh function generator provides the programmability feature itself, as will be shown here. It will also be seen that the present design, while easily meeting the delay and speed requirements of the analyzer system, is inherently flexible and can be adapted to a variety of generator configurations.

The sequency or Walsh ordering of Walsh functions, as illustrated in Figure 5-1, is not the only ordering possible. Sequency ordering is more easily programmable than Paley or Hadamard ordering [15] and is therefore used in the Spectral Analyzer system.

5.2 Sequential Logic-Output Generators

A Walsh function generator may be constructed by using a binary counter and a combinational logic network to decode the counter states and produce the Walsh function outputs. An example of this type of generator is from Harmuth [16], and is illustrated in Figure 5-2. An array of Walsh functions are produced with the binary counter outputs providing the Walsh subset of Rademacher functions directly. The remaining Walsh functions are produced by the EXCLUSIVE-OR gates (modulo-2 adders) which implement the multiplicative property of the

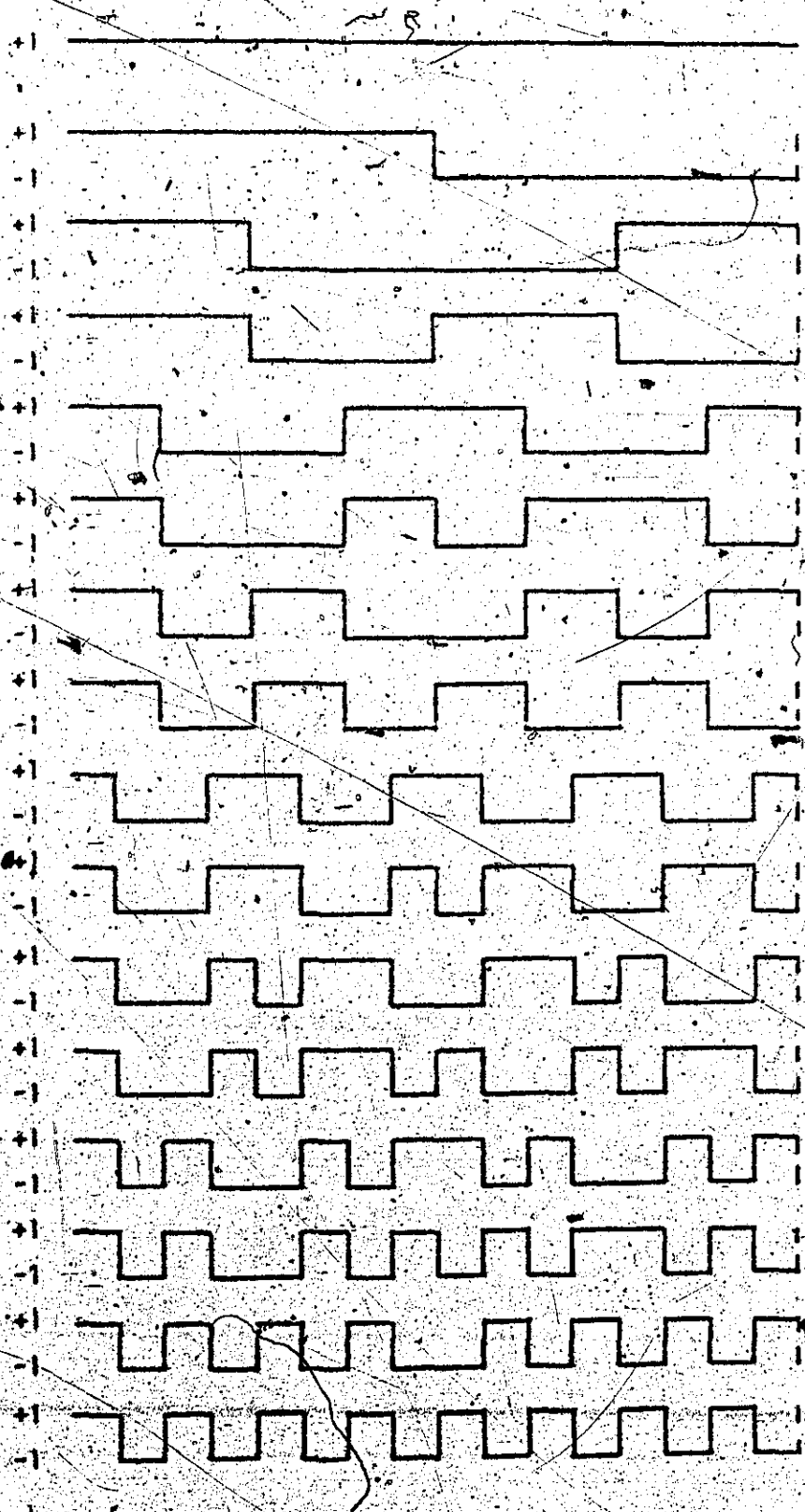


Figure 5-1 Sequency Ordered Walsh Waves to s = 7

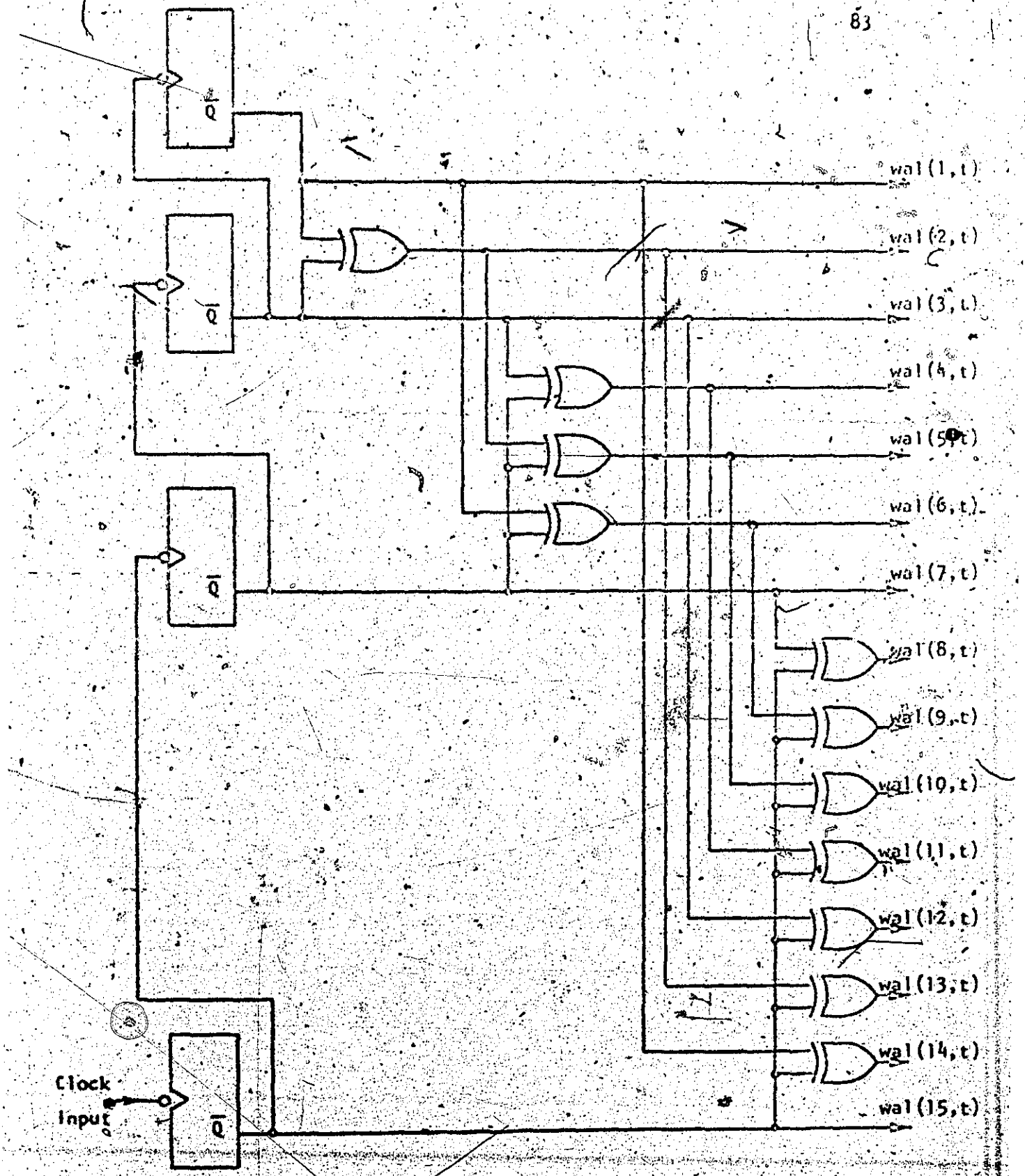


Figure 5-2 Harmuth's Early Walsh Array Generator

Walsh functions:

$$wal(s_1,t)\,wal(s_2,t) = wal(s_1 \oplus s_2, t) \qquad (5\text{-}1)$$

Figure 5-2 indicates the connection pattern which can be extended for larger array generators.

Inspection of the diagram shows that a change in logic state at the counter's output will propagate through one, two, or three EXCLUSIVE-OR elements before reaching the Walsh output. These separate paths of variable delay contribute to large orthogonality error. Further, the problem of output hazards can be aggravated if the binary counter used is the asynchronous or ripple type. The transient logic conditions between counter states add to the hazards or spurious pulses at the function generator's output. The hazard problem is eliminated only when a synchronous Gray code counter that is hazard-free itself is used in place of the binary counter [17]. In order to decrease the orthogonality error, clocked latches or D-type flip-flops (not illustrated) could be added to the Walsh output lines of Figure 5-2. The latches would be clocked after the data at their inputs had settled. However, the latch clock pulse could occur only after the longest expected delay of the combinational network. This seriously limits the operating speed of the generator. Thus it is desireable to have a minimum of combinational logic between the state-counter and the output flip-flops. This approach is realized by using the toggle or T-type flip-flop in the generator design.

5.2.1. Toggle Flip-Flop Implementation

The Walsh function generator reported by Besslich [18] demonstrated

that toggle or T-type flip-flops are particularly suited to Walsh array generators. By concentrating on the toggle input functions required by the T flip-flops, Besslich was able to minimize the necessary combinational logic and to merge the state-counter, or rather the Rademacher function generator, and the Walsh output stages. Thus all flip-flop outputs become Walsh outputs, thereby eliminating hazards and maximizing the generator's operating speed.

The Walsh function generator design used in this analyzer, reported by Gaubatz and Kitai [19], also makes use of toggle flip-flops, but adds the programmability feature to the toggle functions resulting in a dual orthogonal output generator in which the sequency of the Walsh pair is determined by binary inputs. The binary programming input s is fully decoded and requires no special translation; an input of binary 3 (011) produces sal(3,t) and cal(3,t) at the generator's output.

To demonstrate the dual programmed toggle function derivation it is sufficient to consider the set of Walsh functions to s=7. These functions are illustrated in Table 5-1(a), where they are separated into pairs of equal sequency. The Walsh values are tabulated as a function of the sixteen intervals L in one cycle. The logic convention used is that a Walsh value of +1 is represented by a 1 and a Walsh value of -1 is represented by a 0. Immediately following, in Table 5-1(b), are the toggle input functions necessary to produce the Walsh outputs using T-type flip-flops. Inspection of the toggle table for the sal toggle reveals that there are four sets of sequencies that have a logic 1 state in their respective intervals. The sequencies are labeled A, B, C and D. It is further noted that D is the special case of all states equal to 1.

SEQUENCY S

	a b c	sal																cal													
0	0 0 0																														
1	0 0 1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1
2	0 1 0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
3	0 1 1	1	1	0	0	0	0	1	1	0	0	1	1	1	1	0	0	1	1	0	0	1	1	0	0	0	0	1	1	0	0	1	1
4	1 0 0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
5	1 0 1	1	0	0	1	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1
6	1 1 0	1	0	0	1	0	1	1	0	1	0	0	1	0	1	1	0	1	0	1	0	0	1	0	1	1	0	1	0	0	1	0	1
7	1 1 1	1	0	1	0	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	1	0	1
8		1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Interval L																Interval L															

a. Sal and cal Values to S = 7.

SEQUENCY S

	a b c	sal Toggle																cal Toggle															
0	0 0 0																																
1	0 0 1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	
2	0 1 0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	
3	0 1 1	0	1	0	0	0	1	0	1	0	1	0	0	0	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	0	0		
4	1 0 0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0		
5	1 0 1	1	0	1	0	1	0	1	1	1	0	1	0	1	0	1	1	1	0	1	0	1	0	1	1	1	0	1	0				
6	1 1 0	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	0				
7	1 1 1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0			
8		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1																
		A	B	A	C	A	B	A	D	A	B	A	C	A	B	A	D	P	Q	P	R	P	Q	P	V	P	Q	P	R	P	Q	P	V
		Set																Set															

b. Sal and cal Toggle Functions.

	z	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
	y	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	x	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1

c. State-Counter Output Values.

Table 5-1 Walsh Function Generator States

A similar situation exists in the cal toggle table where the sequency sets are labeled P, Q, R and V. Set V represents another special case with all values equal to log 2 0. A characteristic of both toggle tables is that the toggle functions progress through two identical subcycles over the sixteen intervals of L. Returning to the sal and cal tables, it is noticed that all Walsh functions start at the 1 state for all sequencies. Practically, this results in simpler generator reset or initialization requirements.

Table 5-2 lists the sal and cal toggle function sets along with the sequencies in which they occur. It is noticed that the sal sets ABCD occur in the same intervals of L as the cal sets PQRV. The table also shows that sequencies in cal set P have corresponding sequencies 1 in sal set A. An identical relationship holds for sets B and Q, C and R.

A requirement of the generator is to program the dual Walsh output with a binary sequency input s. Therefore, a sequency of 7 requires 3 bits, a b c, c being the lsb. Using standard reduction methods, or simply by inspection of the cal toggle table, the expression for cal sets P, Q, R in terms of a, b, c are:

$$P(a,b,c) = a \tag{5-2}$$

$$Q(a,b,c) = b \tag{5-3}$$

$$R(a,b,c) = c \tag{5-4}$$

For the sal sets A, B, C, the expressions are more complicated:

$$A(a,b,c) = a(b + c) \tag{5-5}$$

$$B(a,b,c) = a\,\overline{bc} + bc \tag{5-6}$$

$$C(a,b,c) = \overline{c}(a\overline{b} + b) \tag{5-7}$$

sal Set	S
A	5,6,7,8
B	3,4,7,8
C	2,4,6,8
D	1 - 8

cal Set	S
P	4,5,6,7
Q	2,3,6,7
R	1,3,5,7

Table 5-2 Sal and cal Toggle Function Sets vs. Sequency

is more feasible practically to perform a subtraction of 1 from sequency s. This gives $s - 1 = \alpha\beta\gamma$ in binary. Replacing a,b,c with the new binary variables again gives the reduced expressions:

$$A(a,\beta,\gamma) = a \qquad (5\text{-}8)$$

$$B(a,\beta,\gamma) = \beta \qquad (5\text{-}9)$$

$$C(a,\beta,\gamma) = \gamma \qquad (5\text{-}10)$$

The logic circuitry required to implement the full adder which is needed to perform the s - 1 operation is admittedly more complex than that required by equations (5-5), (5-6) and (5-7). But it must be noted that the programming sequency s remains unchanged for the duration of the cycle, and even from cycle to cycle when continuous Walsh waves are desired. Therefore, propagation delays within the adder do not effect the generator's operating speed. Also parallel full adders are available complete in one integrated circuit package for input words of either two or four bits. The adders may be cascaded to accomodate a sequency s of any number of bits. The output s - 1 equal to $\alpha\beta\gamma$ is formed by connecting the inputs of the second word to logical 1. Ignoring any carry out bit from the adder, the sum is s - 1.

Since the toggle functions cycle over 8 intervals, the state-counter used requires only 3 flip-flops. The output states of these flip-flops are shown in Table 5-1(c) as a function of the intervals of L. The flip-flop outputs are labeled x,y,z, z being the lsb, the flip-flop which changes most often. Complement outputs are available as $\overline{x},\overline{y},\overline{z}$, respectively. The reduced counter states which produce the sal toggle set functions are as follows:

$$P : \overline{z} \qquad (5\text{-}11)$$

$$Q : \bar{y}z \qquad (5\text{-}12)$$

$$R : \bar{x}yz \qquad (5\text{-}13)$$

The programmability feature requires that each of these reduced functions be further gated by the sequency inputs. The complete cal toggle function thus appears:

$$T_{cal} = a\bar{z} + b\bar{y}z + c\bar{x}yz \qquad (5\text{-}14)$$

The sal toggle function is in the same form, but substitutes the s = 1 programming bits a,b,c and includes the D set, xyz:

$$T_{sal} = a\bar{z} + b\bar{y}z + c\bar{x}yz + xyz \qquad (5\text{-}15)$$

Figure 5-3 illustrates the circuitry required to implement the programmable Walsh function generator. Examination of the circuitry reveals several important aspects of the generator which will be retained even when the size (sequency) of the generator is increased.

The binary counter or Rademacher function generator used as the generator's state-counter is synchronously clocked. This increases the counter's operating speed and reduces the time required for the connecting combinational logic to settle.

All gating functions, including the inverters, are implemented with essentially the same type of TTL gate. The negative logic 3-input OR gate is actually a positive logic 3-input NAND gate. Also, the propagation delay exhibited by the inverter is equal to the NAND gate delay, regardless of the number of NAND inputs. It is a further advantage that the NAND gate propagation delay is the shortest of any combinational gate in the TTL family [20].

Figure 5-4 indicates some typical values for the important timing delays in the circuit. Starting with an active (1 to 0) clock transition,

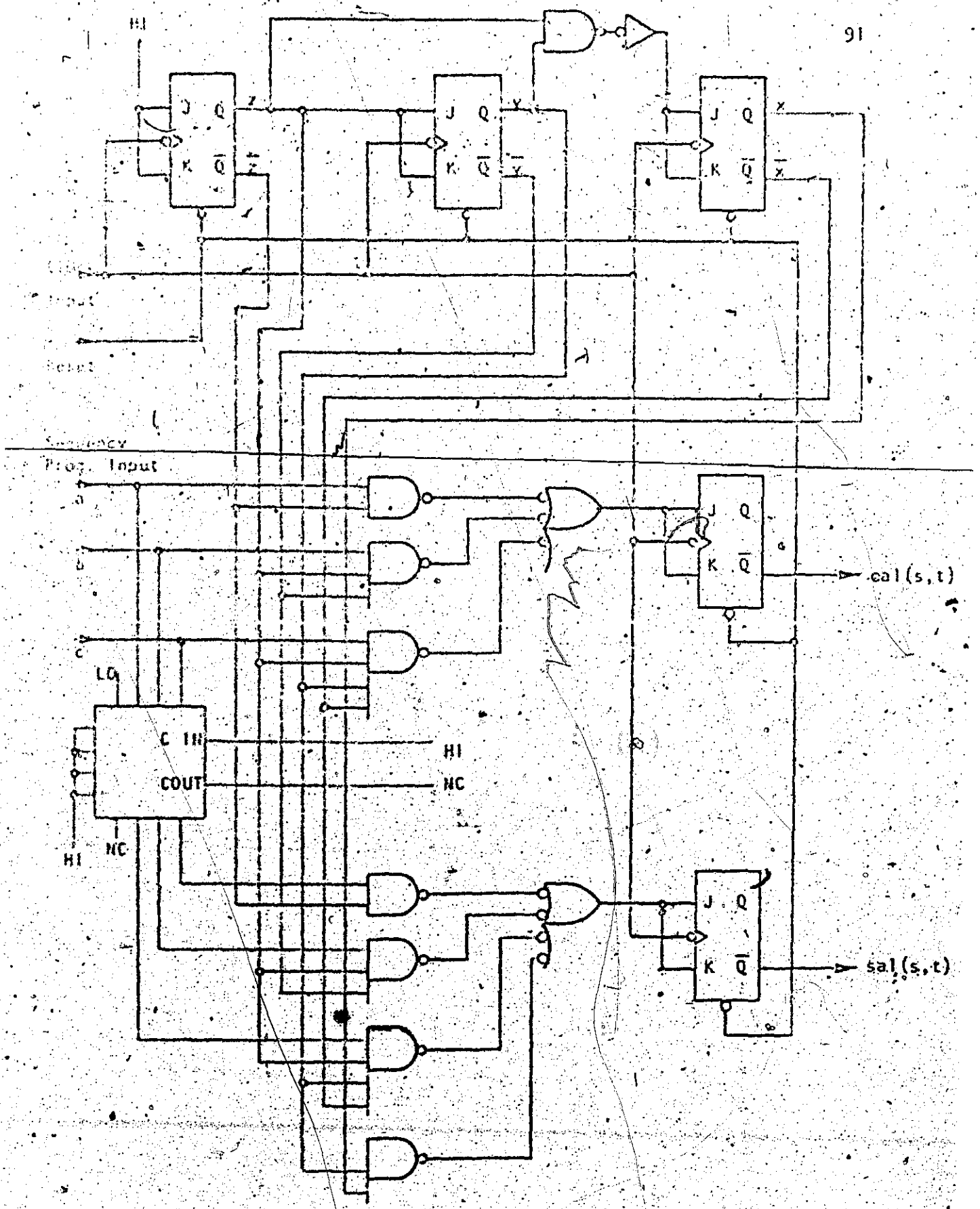
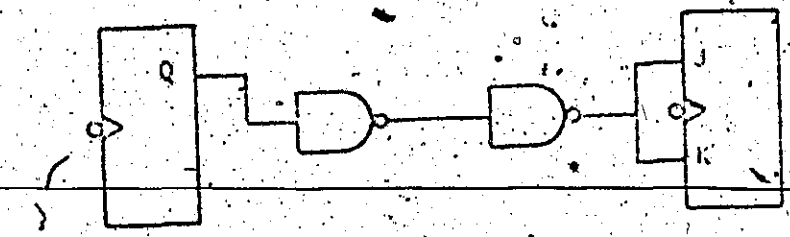
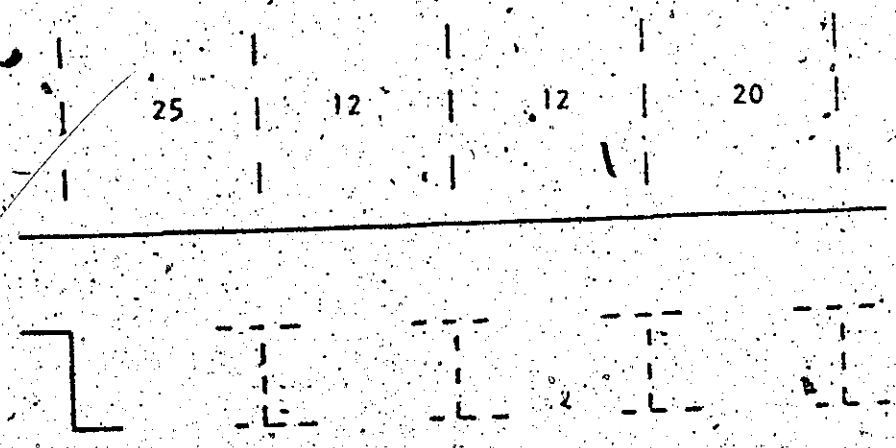


Figure 5-3 Sequency Programmable Walsh Function Generator for Walsh Pairs to s = 7





Note: all delay values are in nanoseconds

Figure 5-4 Critical Generator Timing Delays

25 nanoseconds are required for the flip-flop output to settle. Following this are two NAND-type gate propagation delays of about 12 nanoseconds each. The next delay is due to the required input setup time of the J-K-wired JK flip-flop (SN7473). This is the time that the flip-flop input data must remain unchanged before the clocking transition occurs, and it is typically 20 nanoseconds or greater than or equal to the clock pulse width. Therefore, the minimum time between active clock transitions is 69 nanoseconds, which is consistent with a clock pulse width of 20 nanoseconds. This converts to a clock frequency of about 15 megahertz, attainable with standard TTL devices. The 25 nanoseconds listed as the flip-flop output settling time can, in the extreme, vary up to plus or minus 15 nanoseconds. The worst-case output settling time would therefore be 40 nanoseconds, with the typical value much less than this. Flip-flops exhibiting the longer delay times in the state-counter locations would, of course, jeopardize the generator's maximum operating speed. However, operation to above 10 megahertz is in all cases almost assured.

The toggle input to the x flip-flop is delayed by two gate propagation delays, which is seen as a determining factor in the maximum operating speed of the counter. Two gate propagation delays also constitute the maximum delay required to produce a sal or cal toggle function. Therefore, the programmable Walsh output flip-flops do not place any additional limits on the generator's operating speed.

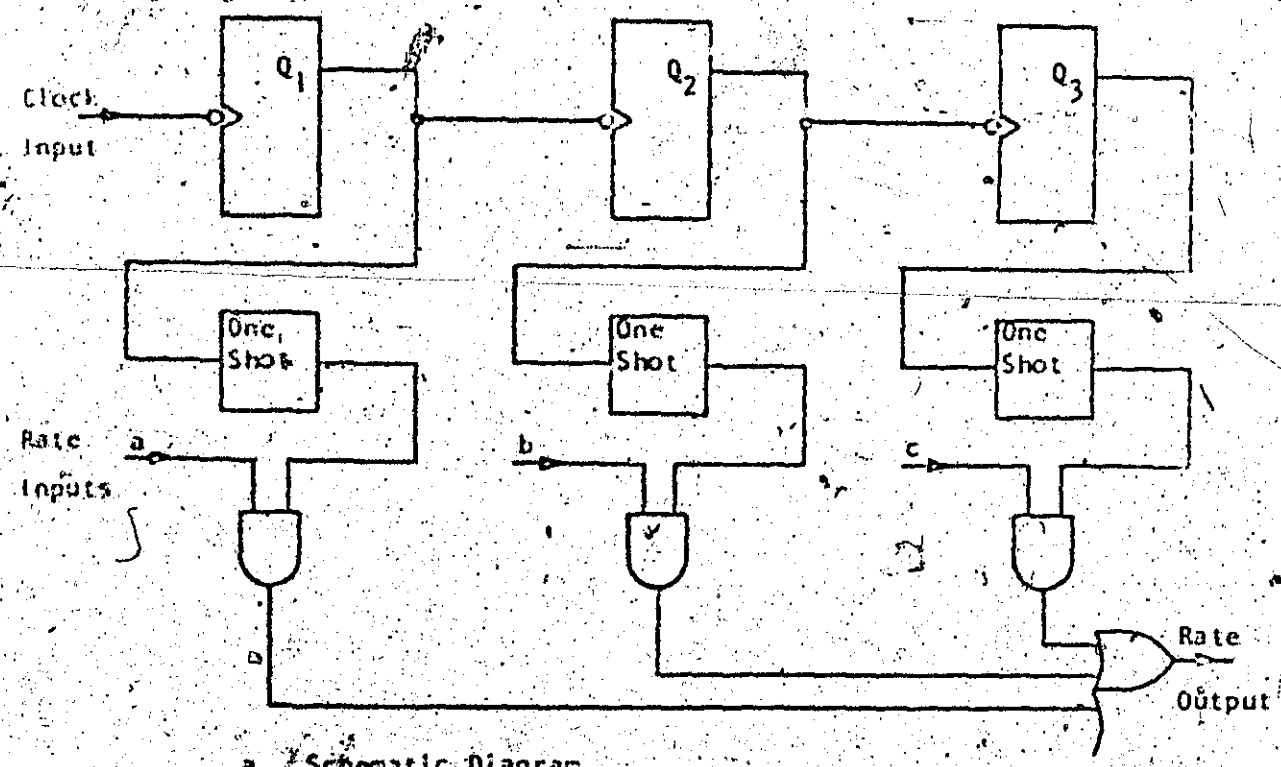
The flip-flops in the counter and the output flip-flops all start the cycle in the 0 or reset state. All Walsh outputs begin with logic 1, so the false, complement, or "$\bar{Q}$" flip-flop output is chosen for all outputs. Thus, resetting all the flip-flops effectively initializes the

Walsh function generator completely. Since synchronous clocking is also used with the output flip-flops, the intervals of the Rademacher outputs and the programmed Walsh outputs are the same. This would be especially useful if wal(15,t) or sal(8,t) is to be used for synchronization purposes in the total analyzer system.

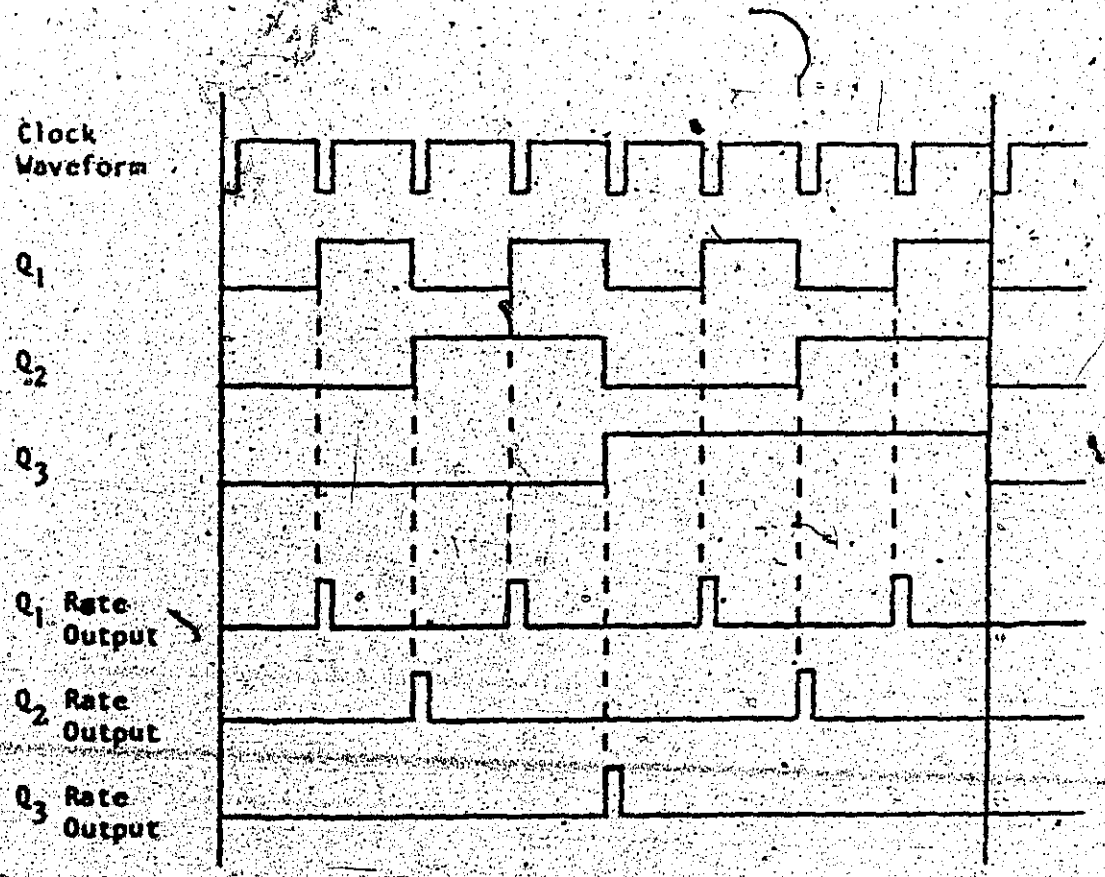
It might be desireable to add an extra stage, w, to the binary counter (not illustrated). This makes it possible to form the function wxyz. This output gives the end-of-cycle indication for a 1b interval cycle.

5.3 The Binary Rate Multiplier as a Toggle Function Generator

The binary rate multiplier emerged as a digital subsystem useful in performing serial arithmetic computations [21]. Basically it consists of a multi-stage binary counter and means provided to produce output pulses at a rate determined by the counter clock rate and a parallel programming input. Figure 5-5 illustrates the basic binary rate multiplier circuit [22], along with the characteristic timing details. The output of each counter stage is connected to a differentiator which produces a positive pulse in response to a logical 0 to logical 1 transition at its input. As can be seen in the timing diagram, the rate of the differentiator's output pulses are a fraction (1/2, 1/4, 1/8) of the binary counter's input clock rate. Starting from the reset condition of all flip-flops equal to 0, the counter states will repeat every 8 input clock pulses. During this 8 clock pulse cycle, one, two, or four pulses will be produced by the various differentiators. Since the differentiator output pulses are never coincident, an OR gate can be



a. Schematic Diagram



b. Timing Details

Figure 5-5 Basic Binary Rate Multiplier

used to provide a common output for the differentiator pulses. It is at this output that the "rate multiplication" function appears. For a differentiator's pulse to be included at the common output, the following AND gate must have a logical 1 at its other input. These three AND gates thus implement the rate programmability function and their external inputs appear as variables in the rate multiplier expression:

$$\text{output rate} = \text{input rate}(a/2 + b/4 + c/8) \qquad (5\text{-}16)$$

Rewriting the expression gives:

$$\text{output rate} = \text{input rate}/8(a4 + b2 + c) \qquad (5\text{-}17)$$

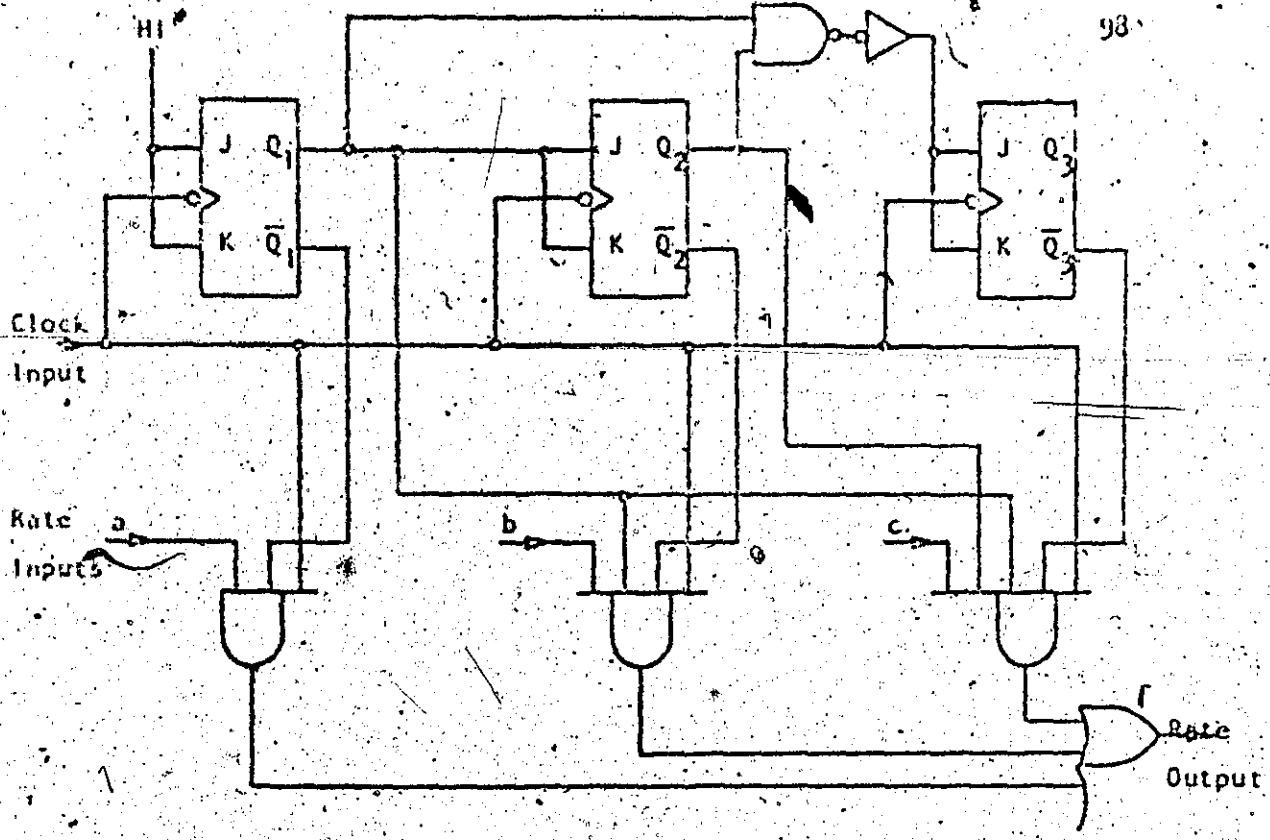
Equation (5-17) shows that a 3-bit parallel programming input can produce between zero and seven output pulses per 8 clock pulse input cycle. The input clock rate, divided by the number of counter states, is multiplied by the binary-weighted input programming bits. At this point it is possible to make the association of rate multiplier output with toggle flip-flop input. The toggle functions are more often HI (logical 1) with increasing sequency, which corresponds to higher pulse rate output with increasing binary programming input. It remains to be shown, however, that the pulse rates supplied are exactly those required by the T-type flip-flops, and further, that the positions of the pulses within the cycle are suitable. It will be seen that certain modifications of the simple binary rate multiplier circuit of Figure 5-5 are necessary to implement it practically and that these changes effectively satisfy the above requirements.

The binary counter shown in Figure 5-5 is a ripple counter which is changed for a synchronously clocked counter. To be acceptable, the pulse differentiators would have to exhibit uniform characteristics

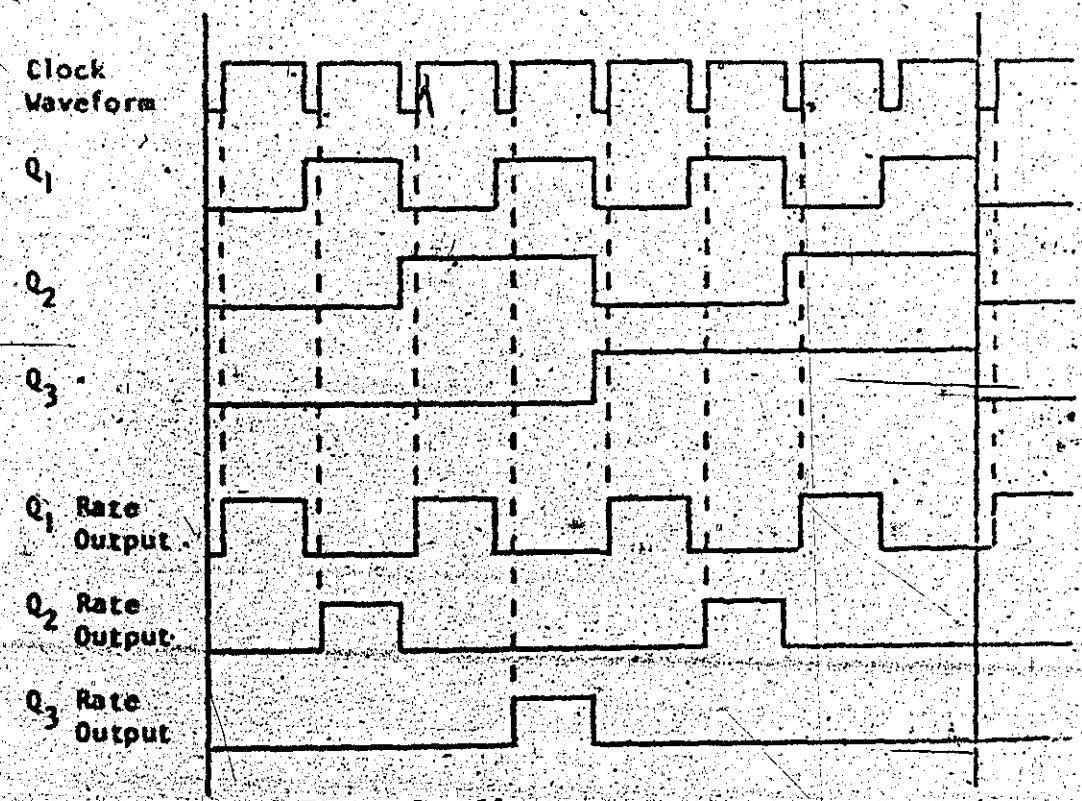
such as propagation delay and output pulse width, and such circuits are difficult to realize. It is preferable to replace the differentiators with extra gating circuitry, as shown in Figure 5-6. Each differentiator is replaced with an AND gate which decodes the counter state immediately preceding the logical 0 to logical 1 transition that was previously used as the differentiator's initiating input. An additional input on the AND gates is connected to the counter clock. Since the flip-flops change state on the negative-going transition, the changing flip-flop states will not effect the AND gate outputs until the clock has returned to logical 1, and the inverted clock to logical 1. The AND gate outputs, and thus the binary rate multiplier output, will remain constant until the next clock pulse occurs. This method of conditioning the output pulses is much more compatible with the wide range of input clock frequencies with which the binary rate multiplier will be used than would an output pulse of fixed duration.

Figure 5-7 illustrates a programmable Walsh function generator for the cal function implemented with a binary rate multiplier as the toggle function generator. It is noticed that there is very little difference between this circuit and the cal generator circuit shown in Figure 5-3. The counter clock is fed to all the programming AND gates, but the gates still provide the correct toggle functions.

To produce the sal output, the additional reduced counter state, XYZ, would have to be provided and fed to the OR gate, thus supplying



a. Schematic Diagram



b. Timing Details

Figure 5-6 Modified Binary Rate Multiplier

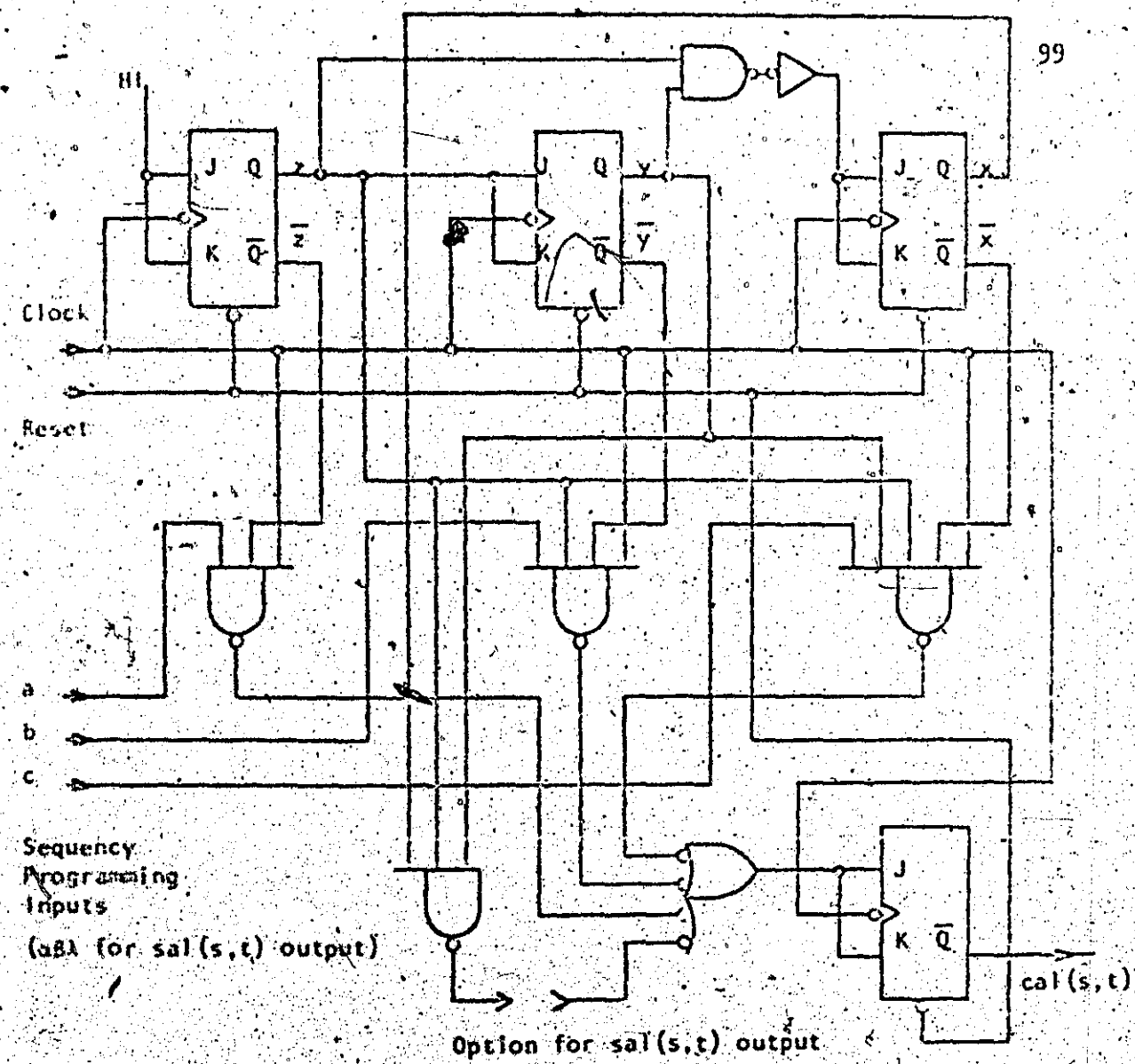


Figure 5-7 Cal Function Generator via Binary Rate Multiplier

the constant term in equation (5-15). This gate is indicated as an option in Figure 5-7. Also the input programming bits, s, would be changed to s - 1 = any.

5.3.1 Sequency Input: 6-bit, $S_{max} = 63$

The Texas Instruments Binary Rate Multiplier type SN7497 is an MSI circuit which provides pulse rate programming for a 6-bit input word. Because the circuit is essentially an extension of the diagram of Figure 5-6, it may be used to directly implement the sequency programmability feature of a Walsh function generator. The internal circuitry of the SN7497 is shown in Figure 5-8. The binary counter is synchronously clocked and the CLOCK input is buffered. The rate programming gates are coupled to the CLOCK input as before. A common, buffered CLEAR resets the binary counter. There are several extra connections to the circuitry which do not appear in the simple version of Figure 5-6. The STROBE input provides additional control of the rate programming gates. The other extra connections are means for cascading a number of 7497's to obtain binary rate multipliers of more than 6 programming bits. These connections are used in adapting the 7497 to use in the Walsh function generator.

The complete schematic for a sequency programmable Walsh function generator with dual orthogonal output is shown in Figure 5-9. Two 7497's are required; one for the cal and one for the sal toggle functions. Since the 7497's Z OUTPUT is derived from a NOR rather than an OR gate, the connecting NOR gate is used as the necessary inverter. The Z OUTPUT is left open and the UNITY/CASCADE INPUT is wired HI. The Y

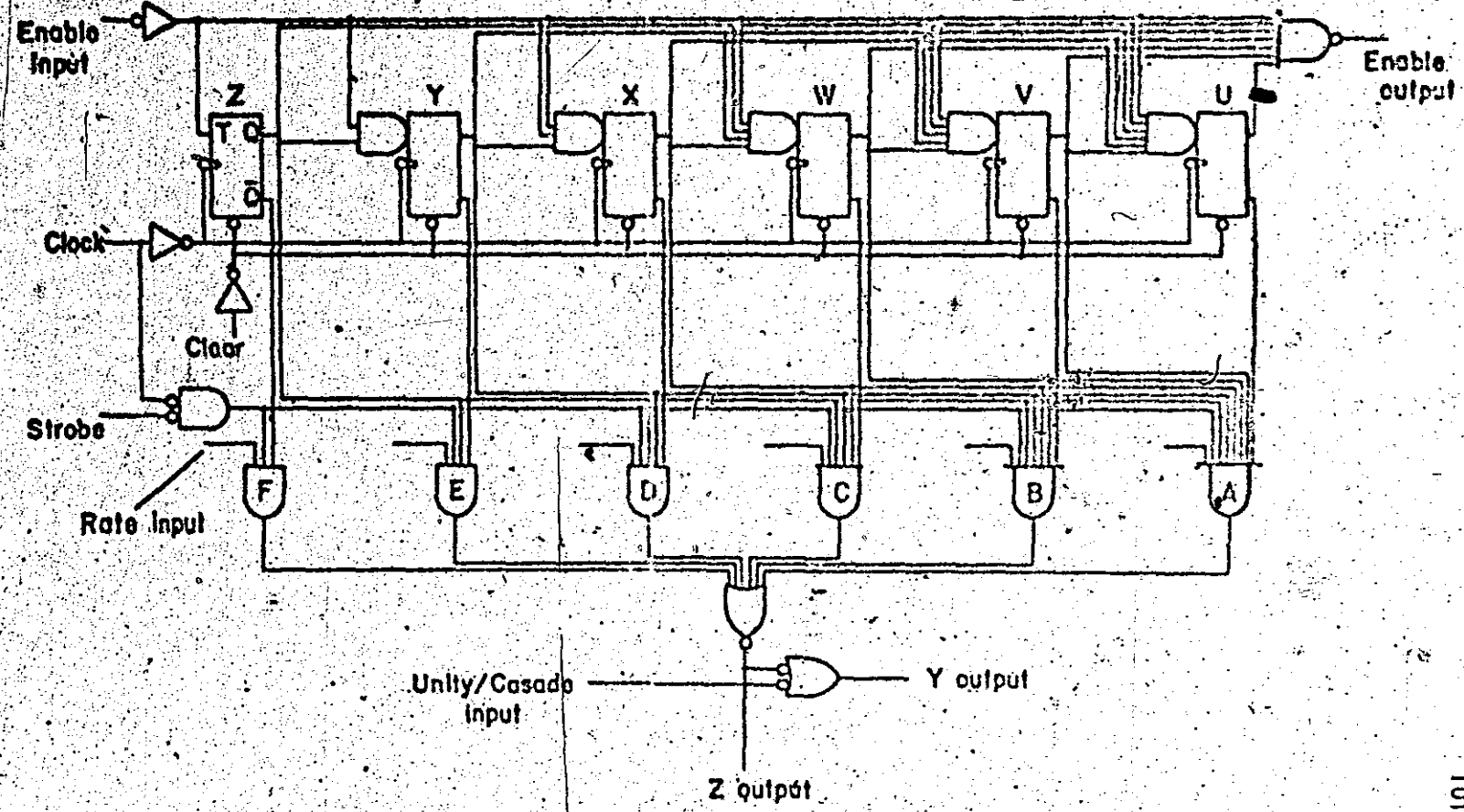


Figure 5-8 Integrated Binary Rate Multiplier Type SN7497 Internal Circuitry

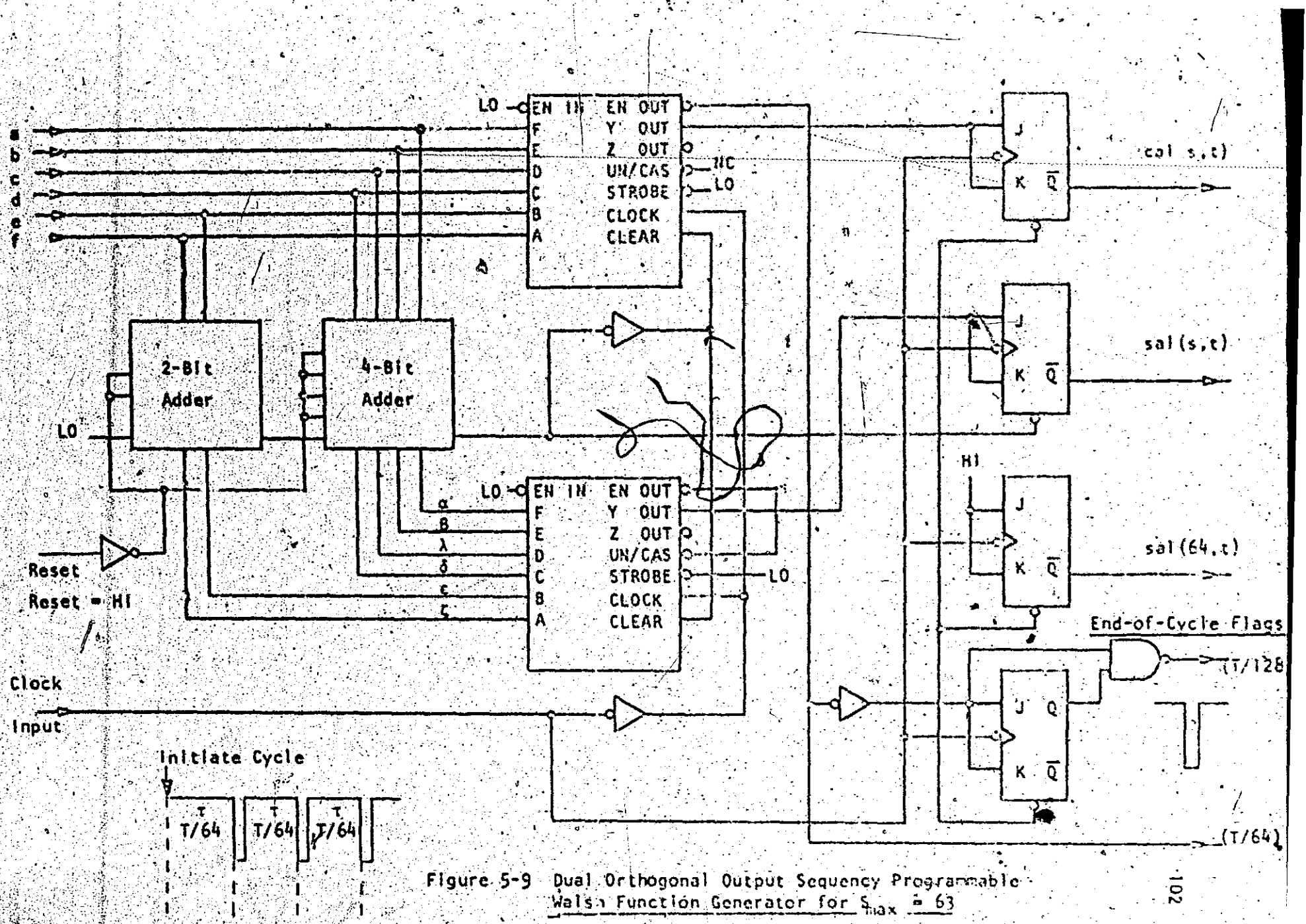


Figure 5-9 Dual Orthogonal Output Sequency Programmable Walsh Function Generator for $S_{max} = 63$

OUTPUT then connects directly to the T-wired JK Walsh output flip-flop. This provides the cal output, and the 6 sequency input or sequency address bits abcdef are applied directly to the rate programming inputs. The msb a is applied to RATE INPUT F, b to E, and so on. The ENABLE INPUT is wired LO and the ENABLE OUTPUT is unused in the cal toggle function.

The sal toggle function makes use of the ENABLE OUTPUT to provide the final, constant term in the toggle function equation of the form used in equation (5-15). For the 6-bit binary counter used in the 7497, this term would be uvwxyz. Since the ENABLE OUTPUT is negative (inverted) logic, it can connect directly to the negative logic pin of the UNITY/ CASCADE INPUT. Thus the internal gating circuitry of the 7497 completely implements all counting and gating functions dictated by the cal and sal toggle function expressions (5-14) and (5-15). The Y OUTPUT is connected to another T-wired JK flip-flop to form the sal output. The programming inputs in the sal toggle function, however, are derived from the s - 1 operation provided by the 6-bit full adder. The resulting $\bar{s}$ is connected to RATE INPUT F, B to E, and so on. The 6-bit full adder is implemented by cascading a 2-bit and a 4-bit parallel adder, which are also MSI circuits.

The combined 6-bit adder's other input word is normally HI, making the adder's output equal to s - 1 or sal programming bits αβλδεζ. Since the second input word of the adder is normally all 1's, any non-zero sequency address abcdef will produce a CARRY OUT equal to logic 1 or HI. The adder CARRY OUT is connected to the RESET pins of all output flip-flops and also to the binary rate multipliers. For a

sequency address of all zeros, the adder CARRY OUT will disappear, and the resulting LO will reset the complete generator. Thus all output flip-flops will be forced HI, which corresponds to a zero sequency programming input. The reset capability is also provided by the external connection to the other adder input word. Taking this connection to the LO state will force the adder's CARRY OUT LO, thus resetting the generator without returning the sequency address input to zero.

The number of clock intervals corresponding to one generator cycle is 128. The active clocking transition is negative going and the first clock pulse of the cycle occurs at the termination of the first interval, 1, of the cycle. The relationship of clock timing to the start of the Walsh cycle is also shown in Figure 5-9.

Two flip-flops are provided in addition to those used for the sal and cal outputs. One is connected directly to the clock input and supplies the sal 64 output. The other flip-flop has an associated gate which decodes the last interval in the cycle. These two outputs are useful for system synchronization.

The input clock pulse feeds the output flip-flops directly to minimize the delay between active clock transition and final Walsh output. Thus the only orthogonality error which can occur is due to differences in switching times between the devices used for output flip-flops. The input clock pulse is inverted to accomodate the positive active transition of the binary rate multiplier's CLOCK INPUT. Therefore, the next toggle state will arrive at the output flip-flop after one inverter propagation delay (12 nanoseconds) and one CLOCK to Y OUTPUT delay of the binary rate multiplier. The latter delay is listed as 20 nano-

seconds, typically, which gives a total delay of 32 nanoseconds. This corresponds to the 49 nanosecond delay (counter flip-flop plus 2 gate delays) illustrated in Figure 5-4. Thus the MSI implementation of the programmable Walsh function generator offers a speed improvement as well as a reduction in package count over previous designs. The 32 nanosecond delay assures generator operation well above 10 megahertz input clock frequencies.

5.3.2 Sequency Inputs: general, $S_{max} = 2^n - 1$

The use of the integrated binary rate multiplier is not restricted to programmable Walsh function generators for which the sequency address is exactly a 6-bit binary word. The sequency programming capability may be increased by cascading several binary rate multipliers, or decreased by shifting the sequency address with respect to the generator's programming inputs.

Cascading several binary rate multipliers is readily accomplished with the connections provided by the integrated circuit. By referring to Figure 5-8, the 7497 internal circuitry, it is seen that connecting the ENABLE OUTPUT of the first 7497 to the ENABLE INPUT of the following one will yield a 12-bit synchronous binary counter. The Z OUTPUT of the second 7497 is brought back to the UNITY/CASCADE INPUT of the first 7497, whose Y OUTPUT then provides a rate multiplier output for a 12-bit input. If more than two circuits are to be cascaded, a multi-input negative logic OR gate will have to be provided external to the 7497's. This is easily supplied by a NAND gate. The external gate's output then provides the toggle output directly. Additional parallel

full adders may be used to perform the s - 1 operation on the 12 or more input address bits.

The number of integrated circuits required to accomodate a 12-bit sequency input is still small; 4 binary rate multipliers, 3 4-bit adders, 2 dual flip-flops, and a few gates. This generator would provide an $S_{max} = 2^{12} - 1 = 4095$.

In some instances the number of programming bits available may be less than 6. A 5-bit sequency programming word, for example, would yield an $S_{max} = 31$. Such cases are accomodated by this generator design and no circuit modifications are required. It is only necessary to recognize that, for example, a sal 8 Walsh wave in a 128 interval cycle is exactly the same as two consecutive sal 4 Walsh waves of 64 interval cycles. This relationship can be observed in Figure 5-1 for cycles of 16, 8, 4... intervals. In the case of a 5-bit sequency address; the 5 input bits should be connected to the 5 most significant bits of the generator's address input. The unused input should be wired LO. This will produce correct sequency programming over a 64 interval cycle. The only difference in the generator operation is that the end-of-cycle flag will still occur at the end of 128 clock pulses or two 64 interval cycles. For a 4-bit input word, the 4 most significant input connections are used and the end-of-cycle flag at the end of each fourth cycle. The sal 64 output is equivalent to sal 32 in the 5-bit case, and to sal 16 in the 4-bit case. No circuit modifications are required.

The procedure described above can be used to adapt this generator design to any number of sequency programming bits. Only two pairs of

cascaded binary rate multipliers are needed to provide an S_{max} of 4095, and a shifted sequency address will provide any closed set of Walsh functions terminating in lower maximum sequencies (2047, 1023, ...).

5.3.3 Array Generators

Although the SN7497 binary rate multiplier integrated circuit is particularly suited to sequency programmable Walsh function generators, it may also be used where a complete Walsh array is required. It is necessary only to provide a separate 7497 to supply the toggle function for each Walsh output desired. The rate programming inputs are simply hard-wired in the appropriate logic state, derived in accordance with the rules outlined above. Since all the Walsh output flip-flops would be clocked simultaneously, there would be no degradation in the orthogonality characteristic from that described previously. An additional advantage of this method of array generation is that all the Walsh outputs are in near-perfect orthogonality, but are derived from completely independent circuits. A failure or an erroneous count in the state-counter of the design shown in Figure 5-2, for example, would jeopardize all the Walsh outputs, whereas the present design does not allow an individual circuit failure to effect the entire array.

5.4 Alternate Logic Families

The discussion thus far has been in terms of the standard TTL or Transistor-Transistor Logic family for implementation of the generator design. It has been shown that TTL devices offer generator operating speeds upwards of 10 megahertz and maximum orthogonality errors of a few

tens of nanoseconds. The following two sections discuss the contribution to Walsh function generator design that can be made by Schottky Clamped TTL and Low Power CHOS.

5.4.1 High Speed Schottky Clamped TTL

Many circuit designs can be implemented directly in Schottky TTL (the 74S__ series) and can expect a five-fold decrease in flip-flop clocking frequency, from 20 megahertz to 100 hegahertz, and a three- to five-fold reduction in gate propagation delay. While many 74__ series circuits have become available in Schottky clamped versions, the Schottky clamped binary rate multiplier, SN74S97, has not yet appeared. Thus there are presently two options for improving the generator design via Schottky devices.

The first option is to build up the complete binary rate multiplier circuit out of Schottky circuits. Then the diagram of Figure 5-7 could be followed more closely, eliminating the clock pulse inverter necessary with the integrated binary rate multiplier. The typical time delay between consecutive active clock transitions is 5 nanoseconds (flip-flop clock to output) plus 2 times 3 nanoseconds (gate delay) plus 3 nanoseconds (flip-flop setup time) giving a total of 14 nanoseconds [23]. Thus the use of Schottky clamped integrated circuits offers a generator which operates at speeds in the 50 megahertz region.

The second option is to retain the TTL integrated binary rate multiplier to supply the sequency programming in one package and to use Schottky clamped devices for the Walsh output flip-flops. An example of a dual JK Schottky clamped flip-flop is the 74S112, which offers

a typical delay from clocking input to output of only 5 nanoseconds. Thus the difference in switching times between various devices of the same flip-flop are significantly less than this, on the order of 1 or 2 nanoseconds. A Walsh function generator thus implemented features operation above 10 megahertz, an extremely low orthogonality error of a few nanoseconds and the economical parts compliment of 7 circuit packages.

It is interesting to note that Boeswetter [24] also recognized the advantage of toggle-programmed (Vorbereitungsfunktionen) flip-flops for Walsh function array generation. He chose to implement his design for an array generator in Motorola ECL (Emitter Coupled Logic). The ECL family was a valid choice for the fastest logic elements available at that time (1968), but Boeswetter recommended hand-selection of the output flip-flops to reduce the orthogonality error to less than plus or minus 10 nanoseconds.

5.4.2 Low Power CMOS

Low Power CMOS is not to be considered where minimum orthogonality error is a requirement. Typical flip-flop switching times run to 200 nanoseconds and a correspondingly high orthogonality error can be expected. The advantage of CMOS, however, is its extremely low power supply requirement of about 50 nanowatts per dual JK flip-flop. This corresponds to the 50 milliwatt requirement of a TTL dual JK flip-flop, a factor of 10^6. The binary rate multiplier will be available shortly in CMOS as the new CD4089A, manufactured by RCA [25]. Only preliminary data is presently available, but it is known that the circuit will have

only 4 rate programming inputs, as well as cascading connections. Therefore, the design procedures described in Section 5.3.2 will be useful to expand a generator's sequency programming capacity. The total generator circuit would require only about a microwatt of power at 5 volts.

5.5 Summary

The Walsh function generator design presented in this chapter is compatible with the requirements of the Walsh Spectral Analyzer. It provides dual output of orthogonal Walsh pairs and the sequency of the pair is determined by external parallel input. The generator design is easily adapted to other configurations, to increase sequency capacity or to provide array generation. The configuration used in the analyzer requires only 7 integrated circuit packages, two of which are MSI binary rate multipliers.

The generator also features excellent timing characteristics; the delay from clock input to Walsh output is one flip-flop switching time, and the orthogonality error is due only to differences in switching times between flip-flops. When the generator is implemented with standard TTL circuits, operating speeds well above 10 megahertz are possible, with orthogonality errors of a few tens of nanoseconds. By using Schottky clamped TTL circuits, the operating speed is increased to 50 megahertz, and orthogonality err is reduced to a few nanoseconds.

CHAPTER 6

SPECTRAL ANALYZER SYSTEM OPERATION

6.1 Introduction

The four major subsystems of the Walsh Spectral Analyzer have been presented in detail in the preceding chapters. These subsystems are the Time Period Generator-Divider, Input Sampling System, Walsh Function Generator and Dual Arithmetic Processor. A fifth subsystem is presented in this chapter which combines the system clock and sample rate generator circuitry. This circuitry is now removed from the other subsystems, thus simplifying system control and eliminating duplicated functions. The subsystem diagrams, where simplified, are presented here.

The various analyzer operational modes are discussed, and the relevant control and clocking conditions are presented in a table. Means for analyzer system control may be implemented by special-purpose hardwired logic circuits or by interfacing to a minicomputer.

6.2 System Clock, Sampling Rate Generator, Decade Range Selection Circuits

The analyzer system components are designed to use a 10 megahertz system clock when operating in the highest input range (50 Hz - 5.0 Hz). A sampling rate generator is also required to provide the sample-convert commands at the 10 kilohertz rate for the highest input range. The 10 kilohertz signal is derived from the 10 megahertz system clock by three cascaded divide-by-10 circuits. To provide both system clock and sampling rate signals over all four decades of analyzer operation,

additional counter-divider and gating circuitry is required. The combined diagram is illustrated in Figure 6-1. This diagram is very similar to that shown in Figure 4-1 as the Sampling Rate Generator. Extra outputs and control gating allow the circuit to serve the entire analyzer system.

Inspection of Figure 6-1 shows that undivided 10 megahertz system clock is available at the designated output when the proper range selection input is presented with a logical 1. This particular gate also has another input which is connected to the reset line. This inhibits the 10 megahertz system clock output, whereas divided system clock is inhibited by forcing the counters into the reset mode.

The selected system clock is also fed to the fixed divide-by-1000 counter chain which supplies the sampling rate output. Pulse-shaping circuits provide a 100 nanosecond pulse for each 1000 system clock pulses and a first pulse when the divider circuits are taken out of reset.

Output gating feeds the sample rate signals to either the Sample Counter in the Dual Arithmetic Processor or to the Input Sampling System, depending upon the control input. If calculate cycles are to follow in immediate succession, all the counter-dividers can be quickly reset at the end of the input waveform period.

6.3 Input Sampling System

The Input Sampling System to be used in the spectral analyzer is illustrated in Figure 6-2. Figure 6-2 is a combination of Figures 3-3 and 3-8. The decade dividers are omitted, however, because the

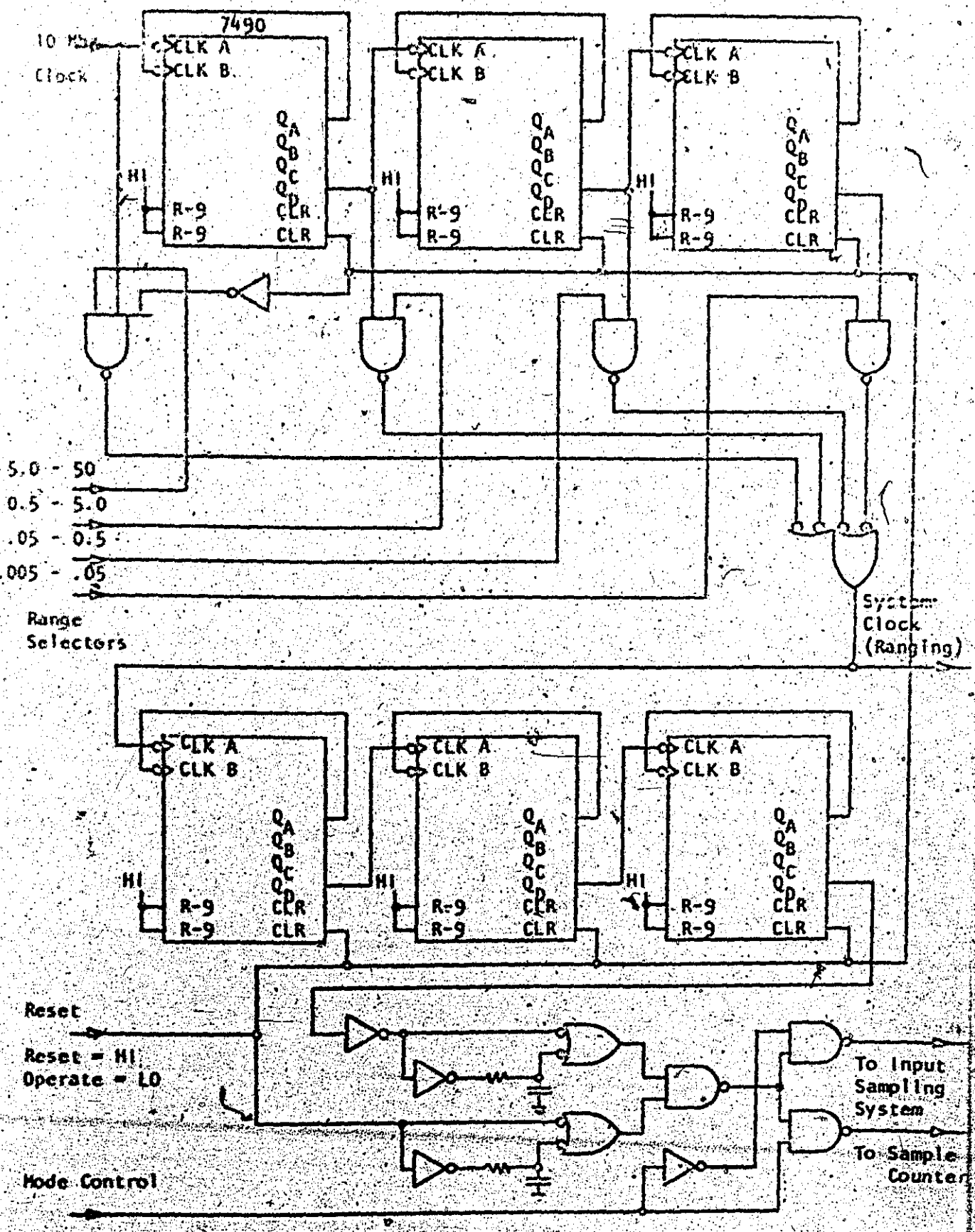


Figure 6-1 Combined System Clock and Sampling Rate Generator for Four Decade Ranges

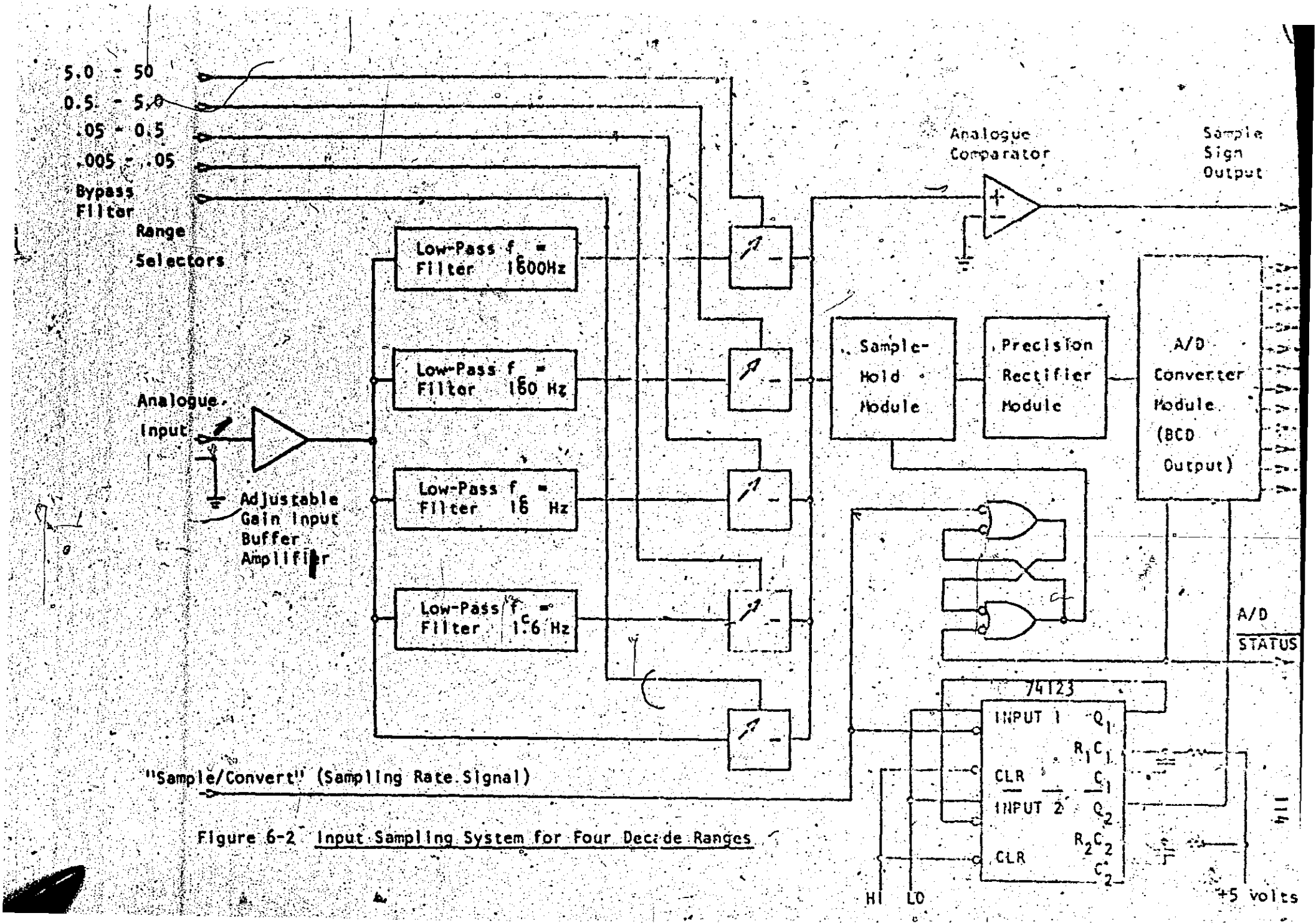


Figure 6-2 Input Sampling System for Four Decade Ranges

sampling rate signal is supplied by the generator described in the previous section.

The analogue input buffer amplifier is gain-adjustable so that the absolute magnitude of the input waveform may be normalized with respect to the digitized coefficient output. The buffer amplifier is fed to the four low-pass filters, and digitally-controlled analogue switches select the output to be measured. A fifth analogue switch permits the low-pass filters to be bypassed when analyzing an input waveform of sufficiently band-limited spectral content. The analogue switches are driven by the same control lines which select the analyzer system clock and sampling rate. Only one analogue switch is in the "ON" state at a given time, and the switch outputs feed the sample-hold module.

Connected in parallel with the sample-hold module is an analogue comparator. The comparator makes the polarity of the input waveform available when the sample command occurs. A precision rectifier circuit follows the sample-hold module which converts the input waveform samples to unipolar voltages. The rectifier may be omitted if the following A/D converter can accept bipolar voltages.

The associated latch and timing circuitry accomodates the time delays required by the sampling and conversion operations.

The comparator output also provides the zero-crossing information required by the Time Period Generator-Divider and the analyzer control logic.

6.4 Time Period Generator-Divider

The Time Period Generator-Divider used in the analyzer system is the circuit illustrated in Figure 2-8. This circuit comprises a subsystem with only three inputs and three outputs. The system clock input is connected to the circuit described in Section 6.2. The mode control input selects either the period measurement mode or the interval generate mode. The reset input resets the counters to zero prior to a measurement cycle.

The overrange and underrange outputs give indication of either a too high or too low system clock frequency, respectively. When either indication is registered, the analyzer range selection control is readjusted for in-range operation. The T/64 or interval output provides the interval clocking pulses required by the Walsh Function Generator.

If the mode control is held in the generate position, resetting the counters will not destroy the data stored in the latches. Thus, resetting the counters at the end of each calculate cycle allows the interval clock pulses to be repeated exactly in each successive calculate cycle for periodic input waveforms.

6.5 Walsh Function Generator

The sal and cal Walsh values used in the spectral analyzer are supplied by the programmable Walsh Function Generator circuit illustrated in Figure 5-9. Since this Walsh Function Generator will produce Walsh pairs up to and including a sequency of 63, the sequency programming address is applied to the 5 most significant bits of the sequency programming input. This provides sequency programming for an S_{max} of 31,

corresponding to a Walsh cycle of 64 intervals. The end-of-cycle flag is taken from the alternate position as illustrated in Figure 5-9, which gives indication after the 64 intervals have elapsed.

The sal and cal outputs are fed directly to the Dual Arithmetic Processor.

6.6 Dual Arithmetic Processor

All of the arithmetic operations required by the spectral analyzer are performed by a dual processor which consists of the subsystem elements described in Chapter 4. These subsystems are the Sample Counter, Sample Pulse Generator, Programmable Division- or Signed-Accumulators, and they are interconnected as shown in Figure 6-3.

The Dual Arithmetic Processor operates in two modes which correspond to the time period measurement cycle and the calculate cycle. Prior to the first cycle, the counters and accumulators are set to zero. During the period measurement cycle, only the Sample Counter is in operation, being clocked by pulses from the Sampling Rate Generator described in Section 6.1. At the end of the measurement cycle, the sampling rate signal is switched to the Input Sampling System, and the number of samples (H) taken during the cycle then resides in the Sample Counter. The Sample Counter is not reset until a new time period measurement cycle is to be started.

During the calculate cycle, the Dual Arithmetic Processor receives the sal and cal values from the Walsh Function Generator. The sampling rate pulses are used to synchronize the latch which stores the product of the Walsh function and the sample sign. When the

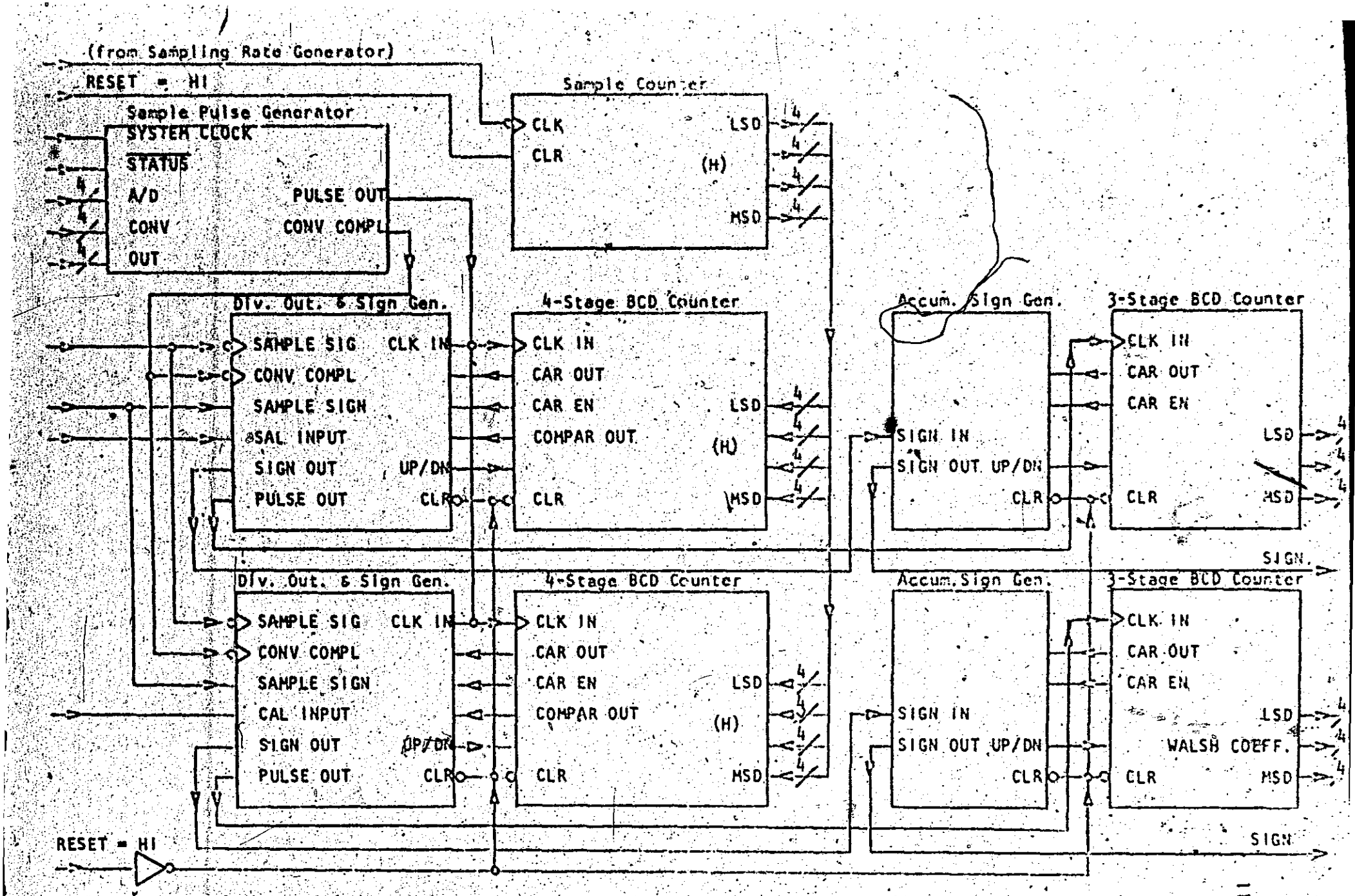


Figure 6-3 Dual Arithmetic Processor Interconnections

sampling and conversion is complete, the accompanying level shift of the $\overline{\text{STATUS}}$ output of the A/D converter (HI to LO) is used to shift the calculated product to the Programmable Divider. The actual latch clocking pulse is the Sample Pulse Generator "LOAD" pulse (see Figure 4-3). This sign data, together with the sample's digitized magnitude comprises the input data for one phase of the processor's operation. An identical sequence is followed for each sample taken during the calculate cycle. At the end of the calculate cycle, the signed Walsh coefficients A_s and B_s are available at the coefficient output accumulators.

The Dual Arithmetic Processor requires no connection to the sequency address inputs; the sequency order of the Walsh coefficients is determined by the sal and cal functions fed from the Walsh Function Generator.

6.7 Analyzer System Interconnections And Control

The complete diagram of the Walsh Spectral Analyzer is illustrated in Figure 6-4. The only component not indicated is the power supply which provides +5 volts for the TTL digital integrated circuits and +15 and -15 volts for the analogue modules: input buffer amplifier, low pass filters, sample-hold and A/D converter.

All necessary control functions are provided by two 2-state mode controls and five reset controls. Table 6-1 indicates the control states for the different phases of analyzer operation including reset, pause, period measure, and calculate. Any normal analyzer operation will be composed of a series of these states. Where "LO or HI" is entered in the table, the control point is free to assume either state. Where

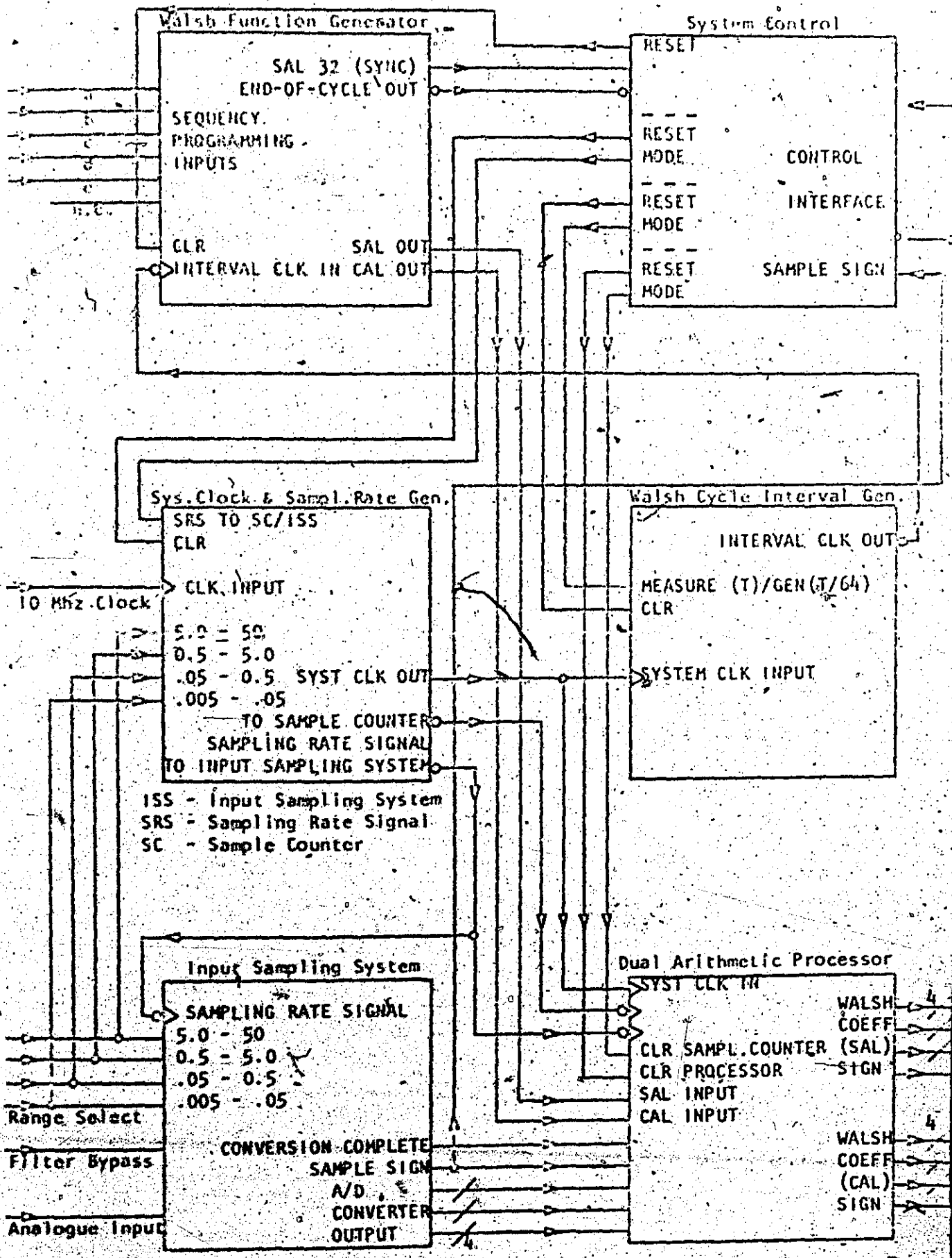


Figure 6-4 Walsh Spectral Analyzer System Diagram

	System Clock, Sampling Rate Generator Mode = HI, SRS to SC Mode = LO, STS to ISS		Input Sampling System	Time Period Generator-Divider Mode = HI, Measure Period Mode = LO, Calculate	Walsh Function Generator	Dual Arithmetic Processor	
	SRG	SYSC				SC	PRO
Reset	R	HI	-	HI	HI	HI	HI
	M	HI	-	HI	-	-	-
	CLI	Internal	(HI)	(LO)	(HI)	(HI)	(LO)
	CLO (HI)	(LO)	(HI)	(HI)	-	-	-
Pause	R	HI	-	LO	LO	LO	LO
	M	LO or HI	-	LO or HI	-	-	-
	CLI	Internal	(HI)	LO	(HI)	(HI)	LO
	CLO (HI)	(LO)	(HI)	(HI)	-	-	-
Measure Period	R	LO	-	LO	LO	LO	LO
	M	HI	-	HI	-	-	-
	CLI	Internal	(HI)	SYSC	(HI)	SRS	SYSC
	CLO SRS	SYSC	(HI)	(HI)	-	-	-
Calculate	R	LO	-	LO	LO	LO	LO
	M	LO	-	LO	-	-	-
	CLI	Internal	SRS	SYSC	T/64	(HI)	SYSC
	CLO SRS	SYSC	SRS (delayed)	T/64	-	-	-

ISS - Input Sampling System
PRO - Processor
SC - Sample Counter
SRS - Sampling Rate Signal
SYSC - System Clock
R - Reset
M - Mode
CLI - Clocking Input
CLO - Clocking Output
SRG - Sampling Rate Generator

All Reset Inputs
RESET = HI
OPERATE = LO

Table 6-1 Analyzer Control and Clocking Conditions

a clocking input (CLI) or clocking output (CLO) shows "(LO)" or "(HI)", the term in the parentheses denotes the logic level of the inactive clock line.

The time period measurement cycle derives its "start" and "stop" control from the LO to HI transition of analogue comparator. This transition indicates a positive-going zero-crossing of the waveform under analysis. After T has been determined, the same signal is used to initiate the calculate cycle. The calculate signal may follow immediately, if desired. The end of the calculate cycle is indicated by the Walsh Function Generator's end-of-cycle flag output.

Analyzer control can be implemented by special-purpose hardware consisting of a state-counter and gating circuitry or by interfacing to a minicomputer. In the latter case, the Walsh Spectral Analyzer would operate under software control, thus providing on-line Walsh spectral analysis for periodic waveforms.

If the low-pass filters in the Input Sampling System are to be bypassed, the low-pass filter range selector lines must be disconnected from the System Clock range selection inputs.

6.8 Summary

The modular approach to analyzer system organization yields an instrument with five basic subsystems: Decade Range Switching System Clock and Sampling Rate Generator, Time Period Generator-Divider, Input Sampling System, Walsh Function Generator and Dual Arithmetic Processor. System control for period measurement and calculate cycles is via five reset controls and two mode controls. Four control lines are required

to adjust the system's internal clocking frequencies as a one-of-four selection. The sequency order of the output Walsh coefficients is selected by applying binary coded logic inputs to the Walsh Function Generator sequency address input. The output Walsh coefficients retain the BCD format of the A/D converter output. The Sample Counter stages also employ the BCD format, and a readout of their values will provide a time measurement of the period of the analogue input waveform.

A laboratory model of the Digital Walsh Analyzer was constructed and all relevant parameters of operating speed, timing accuracy and timing delay were verified to fall within the boundaries which have been derived here. The sal and cal coefficients produced in response to known sine wave inputs agreed with the calculated values. Owing to the compactness of the circuitry, the practical problems which normally accompany the fabrication and testing of a digital logic system were greatly minimized.

CHAPTER 7

CONCLUSION

The Digital Walsh Spectral Analyzer achieves its level of performance by making extensive use of Medium Scale Integration TTL integrated circuits which have recently become available. Walsh coefficients of programmed sequency are produced after one cycle of the input signal, once the period is known, over a four-decade range of 0.005 Hz to 50 Hz. The range limits refer to the fundamental frequency component of the input signal. There is no theoretical or practical low frequency limit to the analyzer's operation. Practical limitations imposed by analogue filters, sampling and conversion modules limit the analyzer's sampling rate to 10 kilohertz. For input signals of known bandwidth no greater than 32 times the fundamental frequency, the maximum fundamental may be increased to 150 Hz, while still measuring the full 32 Walsh coefficients or sequency harmonics. In the case of unknown signal bandwidth, the maximum fundamental frequency is reduced to 50 Hz, and frequency bandlimiting is provided by a low-pass filter.

The 10 kilohertz sampling rate allows 100 microseconds in which to process the digitized value of each sample. A dual processor simultaneously calculates both the sal and cal coefficients, which are normalized with respect to the input signal fundamental frequency. The coefficients are also presented in the BCD fractional format used by the A/D converter output, which simplifies normalization with respect to the input signal

voltage. The 100 microsecond sampling and processing period is readily compatible with the serial arithmetic techniques employed in the analyzer. A significantly shorter processing period would necessitate faster logic speeds than are available in standard TTL digital integrated circuits and/or parallel arithmetic techniques. An increase in sampling rate would also pose difficulties for the Input Sampling System: a possible compromise is to decrease the A/D converter resolution to relax the acquisition time constraint. A trade-off therefore exists between analyzer speed and the resolution of the measured coefficients.

The analyzer design as described requires 70 digital integrated circuit packages and several analogue and conversion modules. All of this circuitry can easily fit on a 12" by 12" printed circuit board, possibly with space available for the 10 megahertz system clock and power supplies. Other wiring configurations are possible, depending on whether the analyzer is used as an independent instrument or is interfaced to a computer system.

Since low-pass filters with fixed cutoff frequencies have been assumed, the use of tunable low-pass filters should be investigated when suitable designs become available. Depending on the range over which the cutoff frequency may be adjusted, an octave- as opposed to decade-ranging internal clock system might be desireable. Additional space would be saved if a single tunable filter could replace the existing four fixed filters.

Additional attention should be given to analyzer design alternatives employing low power circuitry. Many of the digital logic functions now used in the analyzer are presently becoming available in low power CMOS devices, and the circuit modifications to accomodate detail differences

would be minor. The expectation is that even more gates and counters will be combined in the standard integrated circuit package. A parallel development is the availability of linear circuit functions in CMOS devices. Further investigation will reveal whether all of the linear functions (filtering, sampling, A/D converting) are available in process-compatible CMOS fabrication. One could then weigh the feasibility of a totally integrated Walsh analyzer. Such an instrument would have a very low power requirement and would be suitable for battery operation or remote telemetry. A refinement would be the use of a current-saving "stand-by" mode for all circuitry not needed between sampling or processing operations. This would further reduce power consumption when analyzing very low frequency signals.

Much of the analyzer's efficient use of digital hardware is due to the sequency programmability feature of the Walsh Function Generator. However, the maximum rate at which the generator is clocked is 9.6 kilohertz, which corresponds to a bandwidth limited input signal having a fundamental frequency of 150 Hz. The generator can also be constructed with CMOS devices, but applications requiring its high speed capability should also be investigated. Standard TTL implementation offers clock rates above 10 megahertz with an orthogonality error of a few tens of nanoseconds, while Schottky-Clamped TTL implementation increases clock rates to well above 50 megahertz and reduces orthogonality error to a few nanoseconds. The combination of sequency programmability, high speed and low orthogonality error invites use of the Walsh Function Generator in signal multiplexers and waveform synthesizers operating well into the megahertz region.

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