MOS
LSI

TMS 0117 NC
10 DIGIT DECIMAL ARITHMETIC PROCESSOR

- 10 Digits, 3 Registers
- BCD Input and Output
- Direct Add, Subtract, Multiply, Divide
- Implied Constant in 4 Basic Modes
- Add to Overflow, Subtract to Zero
- Shift Left, Shift Right
- Exchange Registers
- Busy/Ready Interlocks
- On-Chip Digit Clock
- 100 ms Maximum Operation Time
- TTL Compatibility

description

The TMS 0117 NC is an MOS/LSI digital building block designed to process numerical data in BCD format. The device performs the most commonly required arithmetic operations, and numbers of up to ten digits can be processed in under 100 milliseconds.

Even when only partially utilized, the TMS 0117 provides a considerable cost saving when compared with more conventional arithmetic techniques. Its applications include automatic control systems, on-line data analysis, digital correlators, weighing machines, and computing counters/frequency meters. The device requires a minimal amount of external control logic, and complex problems may be solved by using it as a 'mini' central processor unit (CPU) in conjunction with SN74188 bipolar integrated circuit Programmable Read Only Memories (PROMs) as the microprogram store.

In addition to the four basic processes (Add, Subtract, Multiply, Divide), the TMS 0117 performs operations such as Increment, Decrement, Shift Left, Shift Right, Exchange Operands, Add to Overflow, and Subtract to Zero.

A BUSY/READY signal generated on the chip discriminates between the BUSY condition (output data invalid, no data can be entered) and the READY condition (output data valid, data can be entered).

Data input and output are in serial form.

An output clock generated on the chip can be used to off load the output data into a memory.

operation

Functions that the processor will perform may be classified into three types – arithmetic, register, and internal control ('housekeeping'). Register and simple arithmetic operations, such as data interchange and add/subtract 1, require a minimal amount of internal microprograms and are rapidly executed. More complex arithmetic operations, such as multiplication and division, use a considerable portion of the program space and take proportionately longer to execute. The time taken to carry out housekeeping instructions, e.g. reset after error flag, is variable, being dependent on the state of the internal program.

The operations are defined as follows:

- Multiply

  Multiply the contents of the output register (multiplicand) by the last data entry (multiplier) and transfer the product to the output register.

– continued

operation (continued)

- Divide
  Divide the contents of the output register (dividend) by the last data entry (divisor) and transfer the quotient to the output register.
- Add
  Add the last data entry to the contents of the output register.
- Subtract
  Subtract the last data entry from the contents of the output register.
- Increment
  Add 1 to the contents of the output register. (Decimal point and sign are ignored in this operation.)
- Decrement
  Subtract 1 from the contents of the output register. (Decimal point and sign are ignored.)
- Add to Overflow
  Continuously increment at the rate of 1 per D scan, the contents of the output register until overflow is reached.
- Subtract to Zero
  Continuously subtract 1 at the rate of 1 per D scan from the contents of the output register until zero is reached.
- Equal
  Execute instruction. Causes the processor to carry out the last stored instruction. Equal also sets up implied constant (last data entry and last function).
- Right Shift
  Move the contents of the output register one place toward the least significant digit (LSD).
- Left Shift
  Move the contents of the output register one place toward the most significant digit (MSD).
- Exchange Operands
  Interchange the last pair of numeric entries, e.g. a ÷ b becomes b ÷ a.
- Clear
  Clear all stored instructions and data registers.
- Reset
  Reset is a master clear and will operate under all conditions. It is used when the processor has entered a locked state, i.e. error flag, and it resets the internal programs.

timing

The basis for the timing is an external clock applied to the device. Nominal frequency of the clock is 250 kHz. An internal state time is equivalent to 3 external clock cycles. A digit time is equivalent to 13 internal state times or 39 clock cycles or nominally 156 microseconds. A digit time (D-time) corresponds to the time during which each digit is displayed. A blanking of one state time is on the leading and trailing edge of each D output signal. Eleven digit terminals are used to scan the data entry logic and to multiplex a display. Only one digit time is high at any given point.

Digits are displayed in scanning mode, thus any digit is displayed for one D-time and displayed again one D-cycle later. (A D-cycle is equivalent to 11 D-times – i.e. 1.72 milliseconds.)

A digit clock is brought out on SP (pin 24) to be used for clocking data to be stored from the TMS 0117 to a memory. The clock pulse is two state times wide (S_4 and S_5 out of 13 state times) and the data is valid on either edge of the clock as shown below. The period of the clock is one digit time (13 state times).

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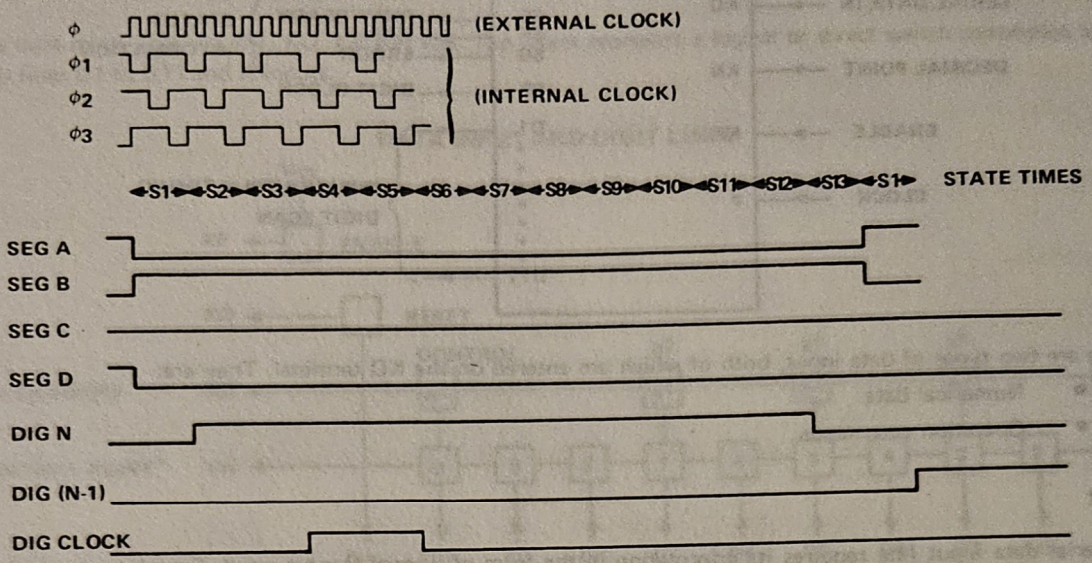
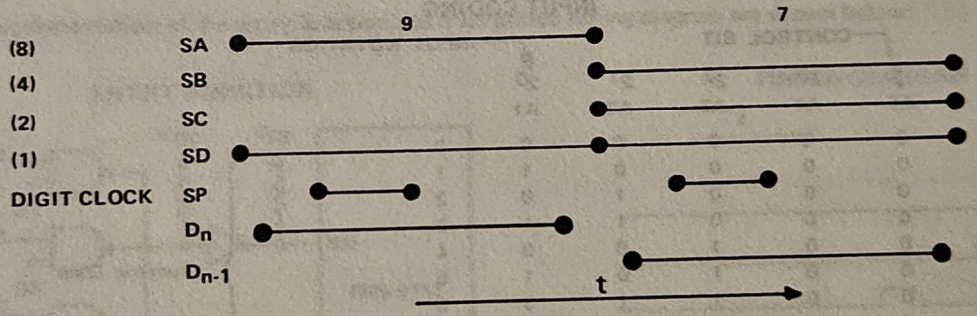
timing (continued)

TIMING DIAGRAM
One Digit Time



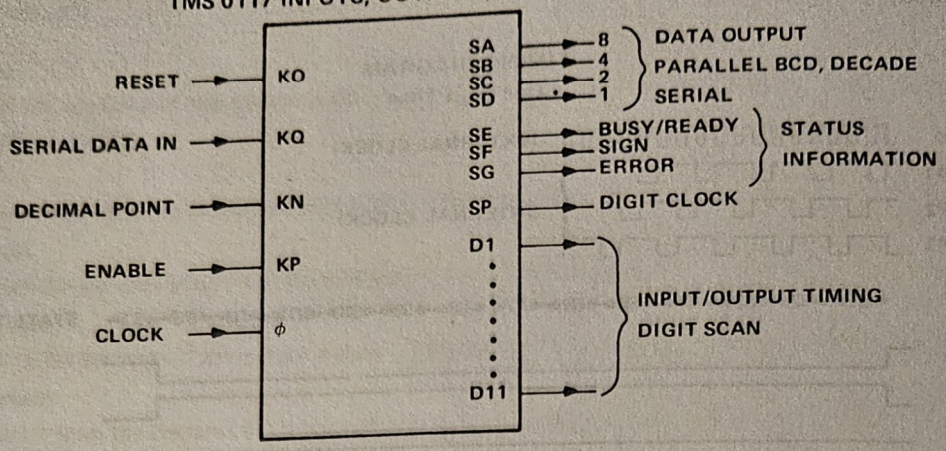
Two Digit Times, Displaying Number 97



The table below shows the time required to complete the functions indicated for a nominal 250-kHz clock rate.

FUNCTION	TIME
Numer entry, single digit	5.2 ms maximum
Operation instruction entry	6.9 ms maximum
Shift left or right	1.72 ms
Increment or decrement	3.4 ms
Exchange operands	5.2 ms
Add, subtract	8.6 ms
Multiplication	70 ms (worst-case numeric inputs)
Division	80 ms (worst-case numeric inputs)
Digit cycle time	1.72 ms
Digit time	156 μs

TMS 0117 INPUTS, OUTPUTS, CONTROL TERMINALS



There are two types of data input, both of which are entered on the KQ terminal. They are:

- Numerical data
- Operation commands

data input

The serial data input line requires its information in the form of a serial five-bit word. Four bits are used as a data/instruction code and the fifth bit as a control. The control determines whether the four-bit code is interpreted as data or as an instruction.

INPUT CODING

CONTROL BIT				INPUT NOTATION		
2^3	2^2	2^1	2^0			
A5	A4	A3	A2	A1		
0	0	0	0	0	0	Numeric Data
0	0	0	0	1	1	
0	0	0	1	0	2	
0	0	0	1	1	3	
0	0	1	0	0	4	
0	0	1	0	1	5	
0	0	1	1	0	6	
0	0	1	1	1	7	
0	1	0	0	0	8	
0	1	0	0	1	9	
1	0	0	0	0	Clear	Instruction Codes
1	0	0	0	1	Equals	
1	0	0	1	0	Multiply	
1	0	0	1	1	Divide	
1	0	1	0	0	Add	
1	0	1	0	1	Add 1	
1	0	1	1	0	Subtract	
1	0	1	1	1	Subtract 1	
1	1	0	0	0	Add 1 to overflow	
1	1	0	0	1	Subtract 1 to zero	
1	1	0	1	0	Shift right	
1	1	0	1	1	Shift left	
1	1	1	0	0	Exchange operands	
1	1	1	0	1	No operation	Not Used
1	1	1	1	0	No operation	
1	1	1	1	1	No operation	

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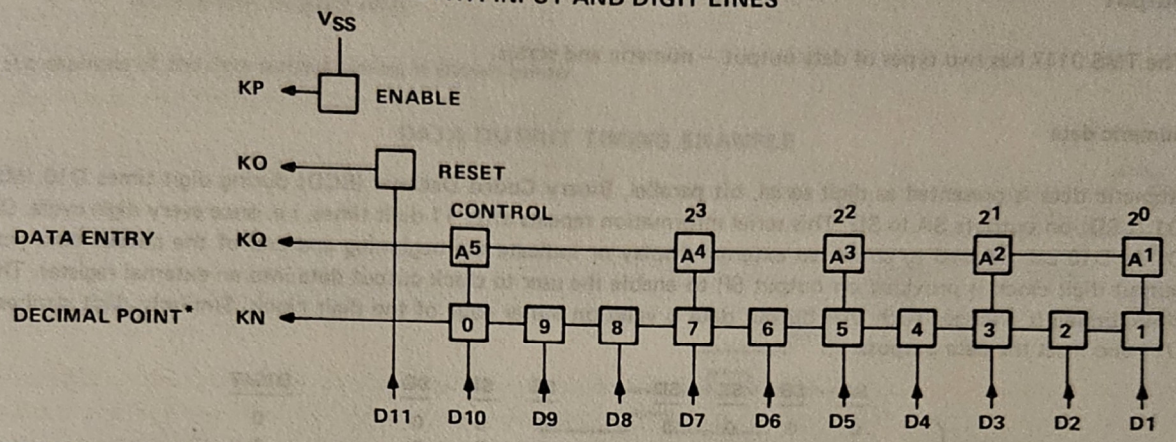
data input (continued)

In order to reduce the number of package pins required for data entry, the five-bit code is serialized. The processor generates sequential digit strobes, D1 to D11, that enable the input data to be serialized.

The data input lines are KN, KO, KP and KQ. The boxes represent a logical or direct switch connection between the digit lines D1 to D11 and K inputs.

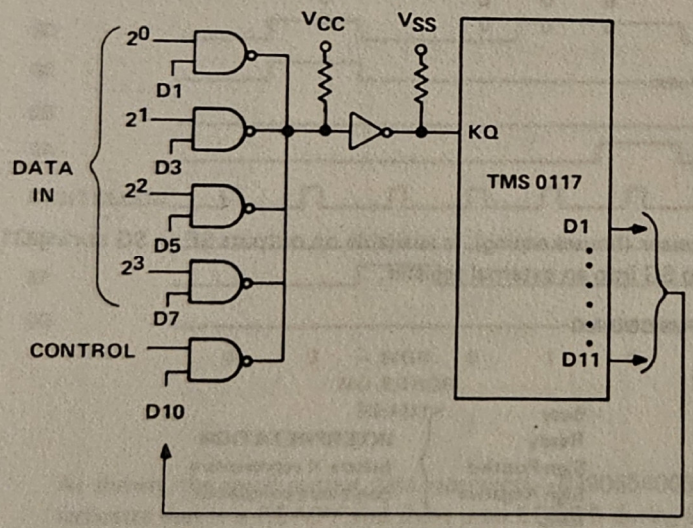
DATA INPUT AND DIGIT LINES



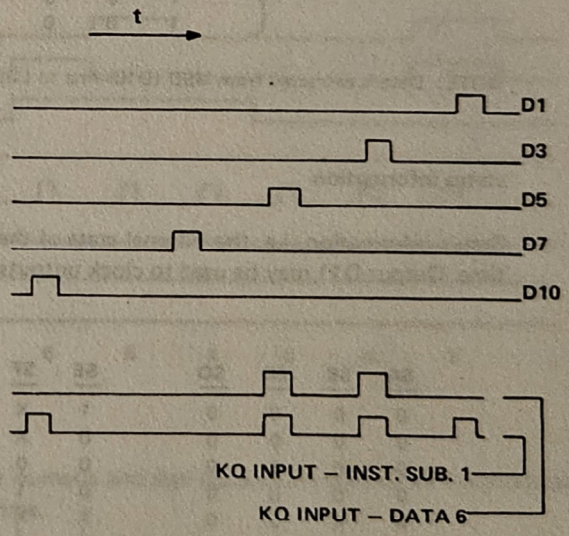
*Decimal point — one switch and only one switch permanently closed.

A gate implementation of the entry function and a simplified timing diagram are shown below.

ENTRY FUNCTION



TIMING DIAGRAM



The data entries are controlled by the enable input, as described under Input Coding. Numeric entries are limited to ten digits. Any zeros that are required to fill the unused most-significant-digit positions preceding number entry (leading zeros) need not be entered; but if, from a systems point of view, it is necessary to enter them, they will be ignored by the processor. Data are entered most-significant-digit first.

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data input (continued)

The RESET terminal is an interrupt signal. It will clear all registers and status information under any conditions. This is the only key operational after the machine enters a locked state. The CLEAR opcode clears in the same manner but cannot be used once in the locked state (overflow). RESET operates independently and does not need to be followed by an ENABLE.

data output

The TMS 0117 has two types of data output – numeric and status.

numeric data

Numeric data is presented as digit serial, bit parallel, Binary Coded Decimal (BCD) during digit times D10 (MSD) to D1 (LSD) on outputs SA to SD. This serial information repeats after 11 digit times, i.e. once every digit cycle. Outputs D1 to D10 can be used to strobe an external display or indicate the beginning and end of the output data word. An output digit clock is provided on output SP to enable the user to clock output data into an external register. The digit clock timing is arranged such that output data is valid on either edge of the digit clock. Similarly digit strobes D1 to D11 also inset the data outputs.

	SA	SB	SC	SD	SE	SF	SG	DIGIT
DATA	0	0	0	0	0	0	0	0
	0	0	0	1	0	0	0	1
	0	0	1	0	0	0	0	2
	0	0	1	1	0	0	0	3
	0	1	0	0	0	0	0	4
	0	1	0	1	0	0	0	5
	0	1	1	0	0	0	0	6
	0	1	1	1	0	0	0	7
	1	0	0	0	0	0	0	8
	1	0	0	1	0	0	0	9

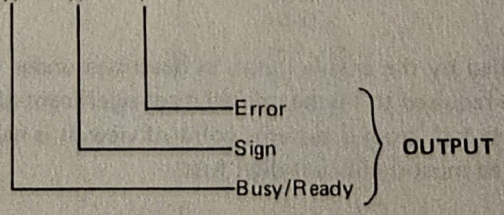
NOTE: Data is extracted from MSD (D10) first to LSD (D1) last.

status information

Status information, i.e. the internal state of the processor (housekeeping), is available on outputs SE to SG during D11 time. Output D11 may be used to clock outputs SE to SG into an external register.

STATUS CODING

SA	SB	SC	SD	SE	SF	SG		
0	0	0	0	1	X	0	Busy	INTERPRETATION (where X represents a don't-care condition)
0	0	0	0	0	X	0	Ready	
0	0	0	0	0	0	0	Sign Positive	
0	0	0	0	0	1	0	Sign Negative	
0	0	0	0	X	X	1	Error	



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data output (continued)

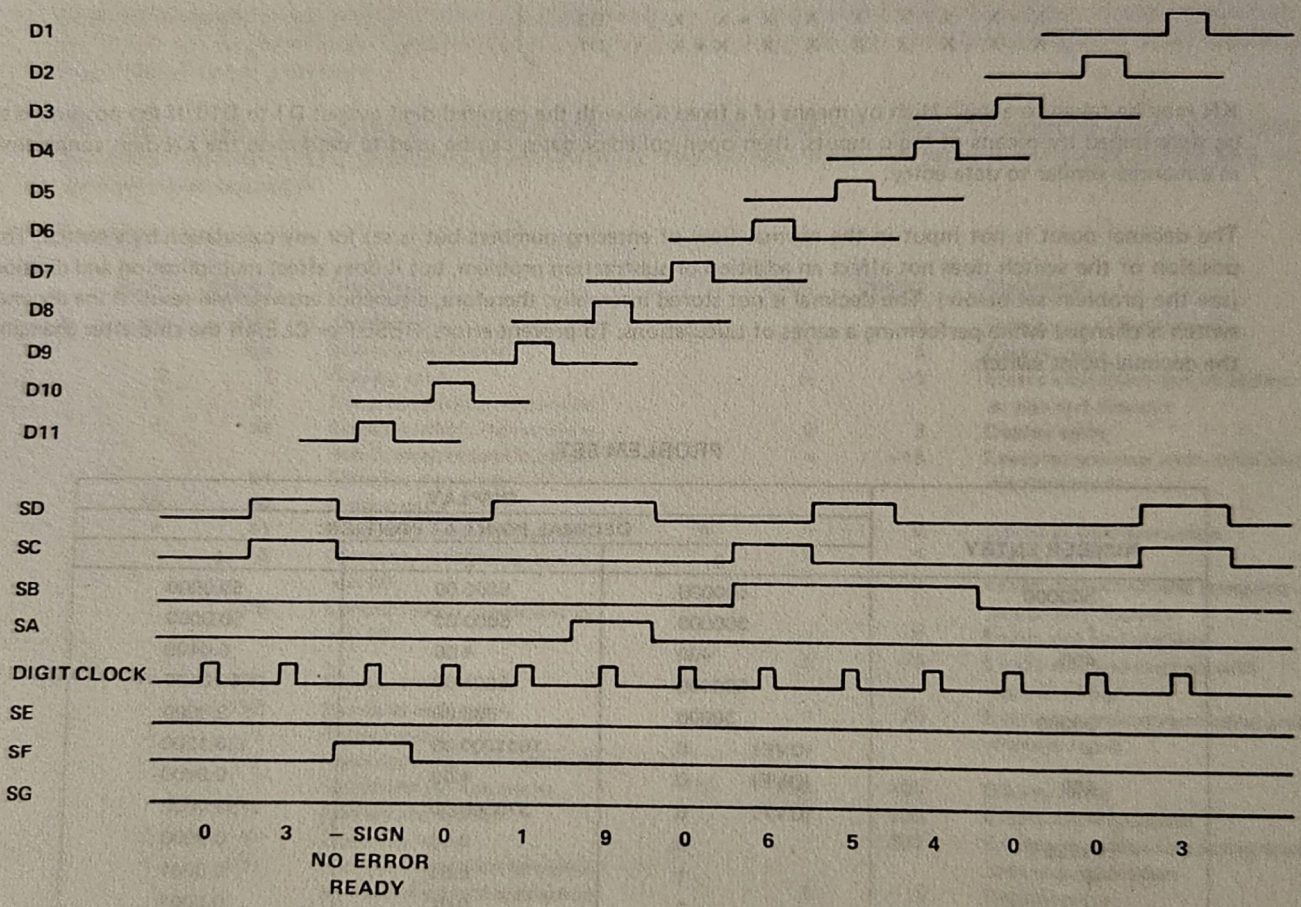
During D11 time, outputs SA to SD are zero. Output SG indicates an error, such as numeric overflow or an invalid operation. Status outputs have the following priorities:

1) Error output SG invalidates all other numeric and status outputs. If an error indication occurs, the processor enters a locked state and must be reset.

2) Busy/ready output SE invalidates numeric and sign data, unless it indicates that the processor is ready to accept new data or instructions, i.e. only when there is no error and the ready signal is present are the sign and numeric outputs valid.

An example of the data output timing is shown below.

DATA OUTPUT TIMING EXAMPLE



As shown, the serial output data represents –0190654003. The numeric and sign outputs are valid since the processor indicates that it is READY and there is no ERROR during D11 time.

decimal point (DP)

The processor operates in fixed-point mode on input and output. The point is not interposed between input digits, i.e., there is no input or output data code representing DP. DP is, in fact, implied by the digit time at which input KN is taken to a logic High. Decimal-point format is shown below.

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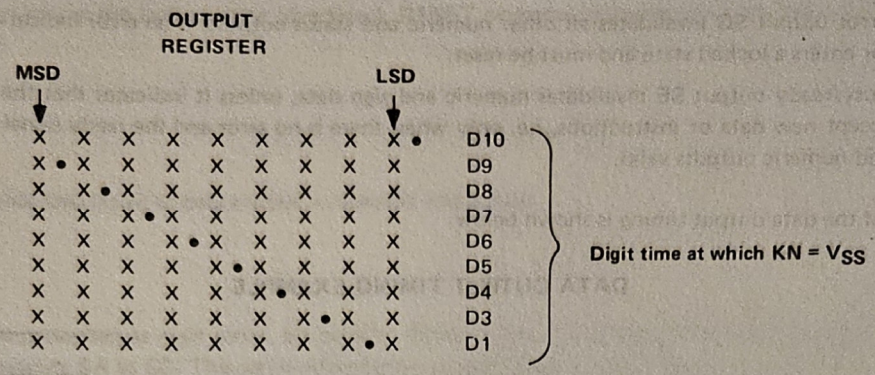
decimal point (DP) (continued)

DECIMAL POINT FORMAT



KN may be taken to a logic High by means of a fixed link with the required digit output D1 to D10. If the position is to be determined by means of logic inputs, then open collector gates can be used to determine the KN-digit connection in a manner similar to data entry.

The decimal point is not input in the normal flow of entering numbers but is set for any calculation by a switch. The position of the switch does not affect an addition or subtraction problem, but it does affect multiplication and division (see the problem set below). The decimal is not stored internally; therefore, erroneous answers will result if the decimal switch is changed while performing a series of calculations. To prevent errors, RESET or CLEAR the chip after changing the decimal-point switch.

PROBLEM SET

NUMBER ENTRY	DISPLAY		
	DECIMAL POINT AT POSITION:		
	0	2	4
500000	500000.	5000.00	50.0000
+	500000.	5000.00	50.0000
400	400.	4.00	0.0400
X	500400.	5004.00	50.0400
30000	30000.	300.00	3.0000
÷	(OVF) 0.	1501200.00	150.1200
400	(OVF) 0.	4.00	0.0400
=	(OVF) 0.	375300.00	3753.0000
RESET	0.	0.00	0.0000
1	1.	0.01	0.0001
÷	1.	0.01	0.0001
3	3.	0.03	0.0003
=	0.	0.33	0.3333
90	90.	0.90	0.0090
=	30.	30.00	30.0000
4	4.	0.04	0.0004
EXCH OP	3.	0.03	0.0003
=	0.	0.75	0.7500

NOTES: 1. Decimal point is external to chip.

2. For clarity, insignificant leading zeros are not shown.

overall operation

The timing of the data entry and control is determined by the enable input in conjunction with the status outputs. It is best expressed in 'digit times', i.e. the time between leading edges of successive digit pulses, and 'digit cycles', i.e. the time between leading edges of successive D1 pulses.

To initiate a data entry cycle, the enable input KP is taken to a logic High (V_{SS}). After a variable delay, the status outputs will indicate that the processor is in the BUSY mode. Data entry will be possible during the READY mode only. The TMS 0117 will ignore inputs when performing an operation. The entry cycle will last 14 to 23 D-times, depending on which digit is On when the enable connects to V_{SS}. Enable must be released within 5 D-times from BUSY signal unless a special mode of operation is desired. In the special mode the enable is kept High throughout the operation. Data inputs are changed each time the processor goes from the READY to the BUSY state until the entire sequence is completed. This speeds up data input since the processor may be ready internally to accept new data, but, because of the multiplexed output, the READY output cannot be given until D11 time. Since data entry and some operations, such as Add 1, Shift Right, etc., are short, the BUSY time will only be 1 to 3 digit cycles.

Data and instructions are entered in the same order as with a +, −, = type of keyboard. In addition to chain operations, e.g. z x b x c =, there is an implied constant. The processor retains the last operator and number entry before an Equal operation, as a constant.

The + and − code is interpreted as a sign after a Multiply or Divide operation, and as an operation at any other time. Successive Equal operations cause multiple executions of the previously stored instructions and the associated data, i.e. constant mode operation.

Examples:

	Entry	Display	Comments
1)	100	100	Display entry
	−	100	Stored as instruction
	3	3	Display entry
	=	97	Executes previous instruction
	=	94	Constant mode, instruction is sub 3, executes and displays
	−	94	Stored as instruction
	50	50	Display entry
	=	44	Executes previous instruction
	=	−6	Constant mode instruction is sub 50
	=	−56	Constant mode instruction is sub 50
2)	100	100	Display entry
	−	100	Stored as instruction
	3	3	Display entry
	+	97	Causes previous instruction to be carried out and stores current instruction.
	10	10	Display entry
	+	107	Previous instruction carried out and stores current instruction
	3	3	Display entry
	−	110	Executes previous instruction and stores current instruction
	99	99	Display entry
	−	11	Executes previous instruction and stores current instruction
	12	12	Display entry
	=	−1	Executes previous instruction and displays result

	Entry	Display	Comments
3)	−	0	Stored as sign/instruction
	5	5	Display entry
	X	−5	Enters instruction and interprets− as sign and displays
	3	3	Display entry
	=	−15	Executes previous instruction and displays result
4)	−	0	Stored as sign/instruction
	5	5	Display entry
	X	−5	Enters instruction and interprets− as sign and displays
	−	−0	Enters sign and displays
	5	−5	Enters data and displays with associated sign
	=	25	Executes previous instruction and displays result
5)	100	100	Display entry
	+	100	Enters add instruction
	−	200	Enters sub instruction and executes previous instruction
	3	3	Display entry
	=	197	Executes previous instruction and displays result
6)	100	100	Display entry
	−	100	Enters sub instruction
	−	0	Enters sub instruction and executes previous instruction
	5	5	Display entry
	=	−5	Executes previous instruction and displays result

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −20 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −20 V to 0.3 V
Clock input voltage range (See Note 1) . . . . . −20 V to 0.3 V
Data input voltage range (See Note 1) . . . . . −20 V to 0.3 V
Applied output voltage range (See Note 1) . . . . . −20 V to 0.3 V
Operating free-air temperature range . . . . . 0°C to +70°C
Storage temperature range . . . . . −55°C to +150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

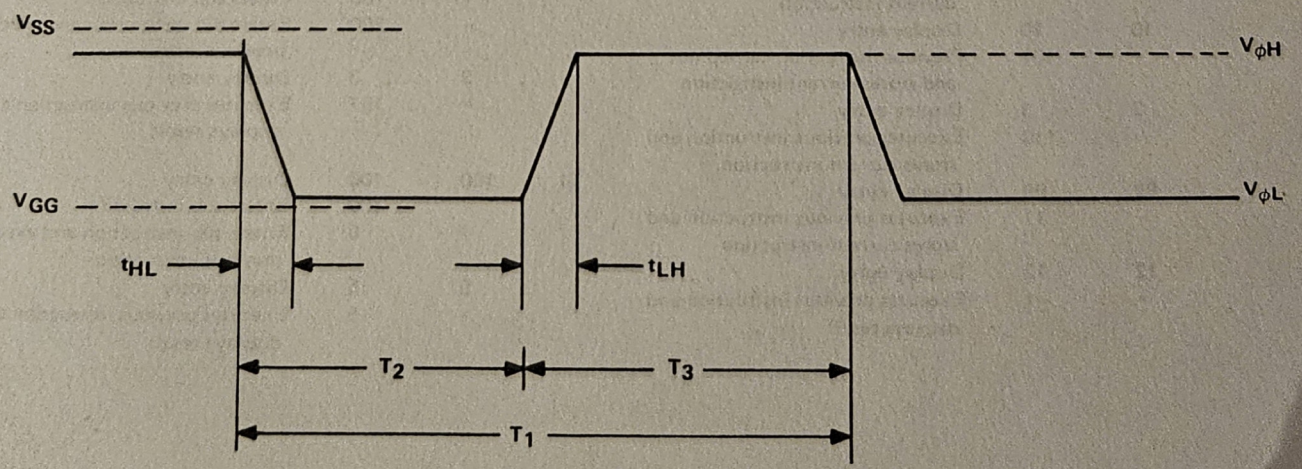
recommended operating conditions

CHARACTERISTICS	CONDITIONS	MIN	NOM	MAX	UNIT
Operating Voltages (See Note 2)					
Drain supply V_{DD} (See Note 3)		0	0	0	V
Substrate supply V_{SS}		6.6	7.2	8.1	V
Gate supply V_{GG}		−8.1	−7.2	−6.6	V
Clock Levels					
Clock high level $V_{\phi H}$		V_{SS} −1.5	V_{SS} −0.5	V_{SS}	V
Clock low level $V_{\phi L}$		V_{GG} −1	V_{GG}	V_{GG} +1	V
Applied Output Voltage		−0.3		18	V
Clock Timing (See Clock Timing Diagram)					
Frequency		100	250	400	kHz
Period T_1		2.5	4	10	µs
Half-period T_2		1.25	2	5	µs
Half-period T_3		1.25	2	5	µs
Clock T_r and T_f	f clock = 100 kHz	30		1000	ns
Clock T_r and T_f	f clock = 250 kHz	30		650	ns
Clock T_r and T_f	f clock = 400 kHz	30		300	ns
Input Level K Lines					
Low		V_{GG}	V_{DD}	V_{SS} −6	V
High		V_{SS} −1.5	V_{SS} −0.5	V_{SS}	V

NOTES: 2. Effective zero suppression depends on a transient free rise of V_{SS} and V_{GG} during power-up. With certain supply systems it may be necessary to capacitively damp the supplies to ensure zero suppression.

3. V_{DD} is voltage reference.

CLOCK TIMING DIAGRAM



electrical characteristics at nominal conditions over 0°C to 70°C temperature range

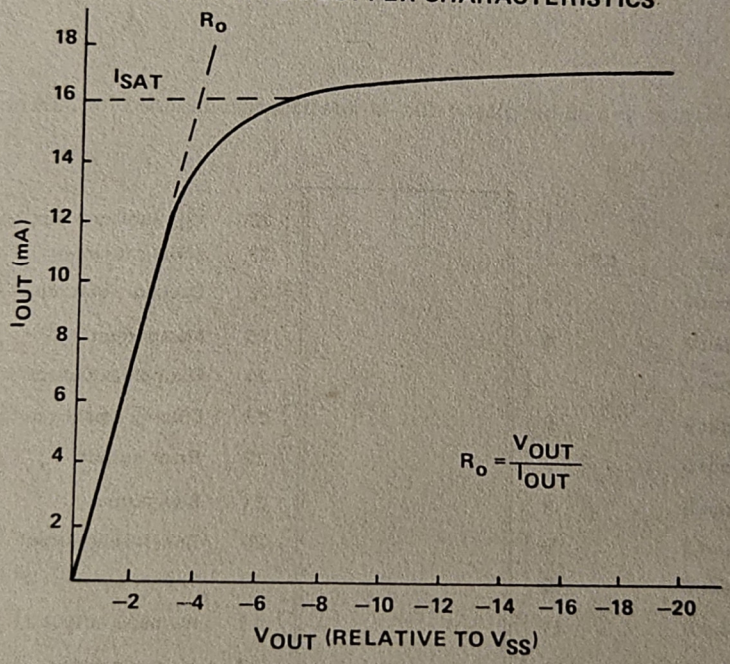
CONDITION	MIN	TYP†	MAX	UNIT
Input current on K lines (K input low) (All other pins GND)		0.1	10	μA
Input pull-up resistance		30		kΩ
Output leakage (off state with $V_{OUT} = V_{SS} - 10$ V) (See Note 4)		0.1	100	μA
Output resistance R_O (on state with $V_{OUT} = V_{SS} - 0.5$ V) (See Typical Output Buffer Characteristics)		250	500	Ω
Output saturation current I_{SAT}		15		mA
Clock leakage (Low Level)		0.1	100	μA
K line input capacitance ($V_K = V_{SS}$, f = 100 kHz)		2.5	5	pF
Output capacitance (f = 100 kHz)		2.0	5	pF
Clock capacitance (f = 100 kHz)		10	20	pF
Average supply current I_{GG} (See Note 4)		10	15	mA
Average supply current I_{DD} (See Note 4)		17	25	mA
Power dissipation (See Notes 4 and 5)		265	400	mW

NOTES: 4. At 25°C. Output leakage cannot be measured with a curve tracer because capacitive coupling will turn on the output.

5. Power saving techniques, including pulsing of power supplies and reduction of clocking cycle may reduce power to 100 mW. These techniques involve special screening of the device.

†All typical values are at $T_A = 25°C$.

TYPICAL OUTPUT BUFFER CHARACTERISTICS



computation times (see timing section)

TTL interface

The K inputs will interpret as a logic High a voltage that lies between the substrate supply voltage V_{SS} and $V_{SS} - 1.5$ V, and as logic Low a voltage between the gate supply voltage V_{GG} and drain supply voltage $V_{DD} + 1.2$ V. The simplest input interface may be a TTL open-collector gate with a pull-up resistor to V_{SS}.

All data and control inputs have an internal pull-up resistor to V_{DD}. The load presented to an external driver is the internal resistor (30 kΩ) and the capacitance of the gate clamp protection diode.

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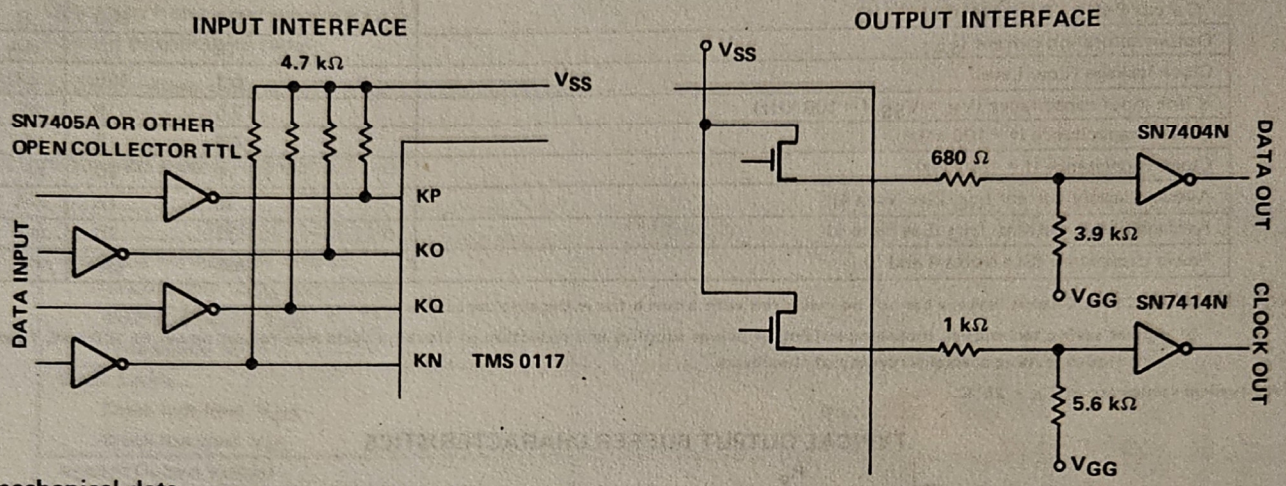
TTL interface (continued)

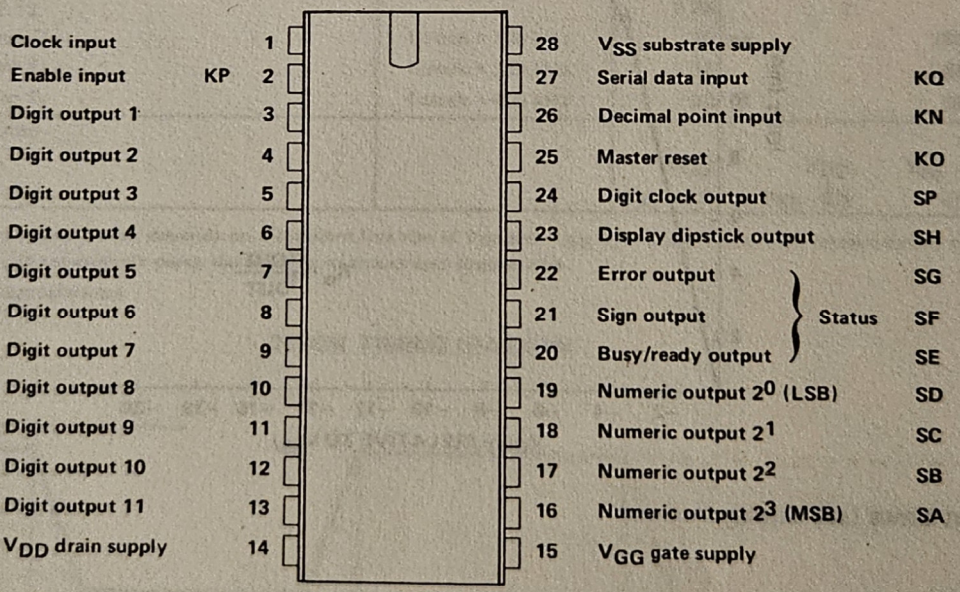
All outputs, D1 to D11 (data and status) are open-drain buffers. The output buffers have a typical channel resistance $r_{DS(on)}$ of 250 Ω and can supply in excess of 5 mA to V_{SS}. An economical output interface compatible with TTL is shown below.

Any output, e.g. digit clock, that is required to drive a TTL clock input should be interfaced with a Schmitt trigger, such as the SN7414N integrated circuit. The Schmitt trigger is required because the fall time of the open-drain output is of the order of 150 nanoseconds and is not directly compatible with edge-triggered TTL inputs.



mechanical data

The TMS 0117 NC is mounted in a 28-pin plastic dual-in-line package, designed for insertion in mounting-hole rows on 0.600-inch centers.



NOTES:
1. Digit outputs D1, D3, D5, D7 and D10 are used to serialize input data.
2. Digit outputs D1 — D10 are used as digit enable for numeric display.
3. Status outputs are valid during D11 time.
4. K input and S output notation per TMS 0100 NC specifications.
5. Display dipstick SH indicates the number of digits displayed in the output register by being at logic High for the relevant portion of the digit cycle. It acts as a zero suppress latch.

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Printed by Newnorth Associates Bedford England