MULTIPLIERS/DIVIDERS PROM ROM HMSI PAL HAL FIFO $7.00

MULTIPLIERS/DIVIDERS PROM ROM HMSI PAL HAL FIFO HI-REL
MULTIPLIERS/DIVIDERS PROM ROM HMSI PAL HAL FIFO HI-REL
MULTIPLIERS/DIVIDERS PROM ROM HMSI PAL HAL FIFO HI-REL
MULTIPLIERS/DIVIDERS PROM ROM HMSI PAL HAL FIFO HI-REL
MULTIPLIERS/DIVIDERS PROM ROM HMSI PAL HAL FIFO HI-REL
MULTIPLIERS/DIVIDERS PROM ROM HMSI PAL HAL FIFO HI-REL
MULTIPLIERS/DIVIDERS PROM ROM HMSI PAL HAL FIFO HI-REL

MULTIPLIERS/DIVIDERS • PROM • ROM • HMSI • PAL • HAL • FIFO • HI-REL

ARITHMETIC ELEMENTS • INTERFACE • CHARACTER GENERATORS

ARITHMETIC ELEMENTS INTERFACE CHARACTER GENERATORS
ARITHMETIC ELEMENTS INTERFACE CHARACTER GENERATORS
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ARITHMETIC ELEMENTS INTERFACE CHARACTER GENERATORS

BIPOLAR LSI

1982 DATABOOK

FOURTH EDITION

Monolithic Memories

BIPOLAR LSI

DATABOOK
FOURTH EDITION

Monolithic Memories MMI

 • 1165 East Arques Avenue • Sunnyvale • CA 94086-9960 • (408) 739-353[illegible] TWX 910-339-9229

Introduction

This book has been prepared to give the user a concise list of all Bipolar LSI Products offered by Monolithic Memories. It is divided by products into sections on HI REL, PROMs, ROMs, Character Generators, PAL, HAL, HMSI, FIFO, Arithmetic Elements Multiplier/Divider, Octal Interface, Leadless and Die. Each section has been designed to allow the user the most useable format for the products described. The PROM, ROM, and Character Generator sections give data in the "generic" form allowing a quick review of the trade-off between devices. Cross references and selection guides are given where applicable. FIFO, PAL, HMSI, Arithmetic Elements, Multipliers/Dividers and Octal Interface data sheets are shown in detail for each product. This LSI data book was formatted with you, the user, in mind. For more information, contact the local Monolithic Memories sales representative or franchised distributor.

Prices

All prices are in U.S. dollars and are subject to change without notice. Distributor costs are sufficed by ▲ (price increase) ▼ (price decrease), an N (new product).

Minimum Order Requirements

For all orders placed on the factory there is a minimum order requirement of $1000 ($250 per line item) except for the following:

ROMS/HAL — For masked programmable read-only memories and hard array logic there is a minimum order requirement of $2500 and 500 units, plus a one time (per bit pattern) mask charge of $750.

Terms

Net 30 days from date of invoice, FOB Sunnyvale, California.

Commercial/Military Limits

The letter codes "C" and "M" are used to denote commercial and military level device limits as follows.

Commercial — TA = 0°C to +75°C
VCC = 5V to ±5%

Military — TA = −55°C to 125°C
VCC = 5V ±10%

Package Codes

All devices ordered must include a package code as a suffix to the part number. The package code definitions are as shown below.

PACKAGE CODE	DESCRIPTION
J	Ceramic dual-in-line
JS	Ceramic SKINNYDIP™
N	Plastic dual-in-line
D	Side brazed ceramic dual-in-line
F	Flat pack
W	Cerpak
L	Leadless

See "Part Numbering Systems" for complete part descriptions.

Screening Options

PROCESS LEVEL	PART MARKING
MIL-STD-883 Method 5004 and 5005 Level B	883B (Suffix)
MIL-STD-883 Method 5004 and 5005 Level C	883C (Suffix)
MIL-STD-883 Method 5004 Modified	B (Suffix)

SKINNYDIP is a registered trademark of Monolithic Memories

Part Numbering Systems

PAL/HAL

PAL 14 L 4 M J 883B

- PAL = PROGRAMMABLE ARRAY LOGIC FAMILY
  HAL = HARD ARRAY LOGIC
- NUMBER OF ARRAY INPUTS
- OUTPUT TYPE
  H = ACTIVE HIGH
  L = ACTIVE LOW
  C = COMPLEMENTARY
  R = REGISTERED
  A = ARITHMETIC REGISTERED
  X = EXCLUSIVE OR REGISTERED
- NUMBER OF OUTPUTS
- TEMPERATURE CODE
  C = COMMERCIAL
  M = MILITARY
- PACKAGE TYPE SEE "PACKAGE CODES"
- HI-REL SCREENING LEVEL SEE "SCREENING OPTIONS"

Octal Interface

SN 54 LS 373 J 883B

- STANDARD PREFIX
- TEMPERATURE CODE
  74 = COMMERCIAL
  54 = MILITARY
- FAMILY
  S = SCHOTTKY
  LS = LOW POWER SCHOTTKY
- UNIQUE 3 DIGIT PART NUMBER
- PACKAGE TYPE "SEE PACKAGE CODES"
- HI-REL SCREENING LEVEL SEE "SCREENING OPTIONS"

NiCR PROMS ROMS Character Generator-Logic

5 3 41-1 J 883B

- TEMPERATURE CODE
  6 = COMMERCIAL
  5 = MILITARY
- PRODUCT
  0 = CHARACTER GENERATOR O.C.
  1 = CHARACTER GENERATOR T.S.
  2 = READ ONLY MEMORY (ROM)
  3 = PROGRAMMABLE READ ONLY MEMORY (PROM)
  7 = LSI LOGIC PRODUCT
- UNIQUE 2 DIGIT PART NUMBER
- –1 = SCHOTTKY PROCESS (ROMS/PROMS)
  –2 = IMPROVED PERFORMANCE OVER-1
- PACKAGE TYPE SEE "PACKAGE CODES"
- HI-REL SCREENING LEVEL SEE "SCREENING OPTIONS"

High Performance Ti-W PROMs

5 3 S 2 4 0 A J 883B

- TEMPERATURE
  6 = COMMERCIAL
  5 = MILITARY
- PRODUCT
  3 = PROGRAMMABLE READ ONLY MEMORY (PROM)
- FAMILY
  S = SCHOTTKY
  LS = LOW POWER SCHOTTKY
  RX = REGISTERED
- MEMORY SIZE
  1 = 1024 BIT
  2 = 2048 BIT
  4 = 4096 BIT
  8 = 8192 BIT
  16 = 16384 BIT
- NUMBER OF OUTPUTS
  4 = 4 BIT
  8 = 8 BIT
- OUTPUT/PIN OUT DESIGNATOR
  0 = OPEN COLLECTOR
  1 = THREE STATE
- PERFORMANCE
  NONE = STANDARD
  A = ENHANCED
- PACKAGE TYPE "SEE PACKAGE CODES"
- HI-REL SCREENING LEVEL SEE "SCREENING OPTIONS"

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Quality System

The quality system at Monolithic Memories is based on MIL-Q-9858, "Quality Program Requirements," MIL-I-45208, "Inspection System Requirements," and MIL-M-38510, Appendix A, "Product Assurance Program." MIL-M-38510 plays a significant role in structuring Monolithic Memories' quality program.

Monolithic Memories' facilities in Sunnyvale were certified in June of 1977 by DESC, Defense Electronics Supply Center, to manufacture and qualify to Class B and Class C Schottky Bipolar PROMs, ROMs and RAMs in accordance with the requirements of MIL-M-38510. This certification included a successful audit of our quality system to the stringent requirements of Appendix A of MIL-M-38510 which defines a Product Assurance Program tailored for integrated circuit manufacturers by DESC. This same quality system has also met the strict requirements of both "controlled" and "captive" line programs connected with our special Hi-Rel programs.

The quality accent at Monolithic Memories is on process control as reflected in the use of many monitors and audits rather than gate inspections. This philosophy is consistent with building in quality and reliability rather than attempting to screen for it.

Process Control

Monolithic Memories' advanced low-power Schottky TTL process uses such techniques as redundant masking to reduce random defects and self-aligning masking to reduce active chip area. Although more costly than the standard SSI or MSI Schottky TTL processes, these approaches yield better quality, increased reliability and lower overall cost due to higher net die per wafer. During the initial production stages of new designs and periodically thereafter, engineering characterizes the design-process compatibility by careful sample selection of lots reflecting process variable extremes.

Screening

Much of the assembly (packaging only) is performed offshore at our Penang, Malaysia facility. The facility has been qualified and is routinely monitored for conformance to MIL-STD-883 by Monolithic Memories' military customers as well as by Monolithic Memories' Quality Control Department. All standard military hermetic Monolithic Memories products are 100% screened to MIL-STD-883 Class C. This includes:

- Pre-cap inspection.*
- High-temperature storage at 150°C.
- Temperature cycling. –65°C to +150°C.
- Constant acceleration.
- Fine and gross leak.
- Final electrical test.
- Q.A. sample acceptance testing.

*Modified for LSI.

Standard commercial hermetic product receives the following screens and monitors to insure the highest possible product quality.

- Pre-cap inspection*
- High temperature storage
- Temperature cycle
- Constant acceleration
- Fine and gross leak
- Final electrical test

$\left.\begin{array}{l}\text{Temperature cycle}\\ \text{Constant acceleration}\\ \text{Fine and gross leak}\end{array}\right\}$ Daily monitors in lieu of 100% screening which insure the AQL levels before are met or exceeded.

*Modified MIL-STD-883 Pre cap.

The product assurance levels which Monolithic Memories guarantees are listed in the table on this page.

Reliability Engineering maintains product surveillance through routine sampling and submission to MIL-STD-883, method 5005, qualification testing. Additional step-stress and extended (limit) testing conditions are used when warranted. In general, failure rates have been found to be two orders of magnitude better than MIL-HDBK-217 estimates.

The quality organization is defined into three departments:

- Quality control
- Quality assurance
- Reliability assurance

Quality Assurance (AQL) Levels

TEST	LEVEL I COMMERCIAL (%)	LEVEL II MILITARY (%)
Hermeticity (includes fine and gross)	0.65	0.4
Electrical		
DC at 25°C	.40	.25
Functional at 25°C	.40	.25
AC at 25°C	.65	.40
DC at Temperature Extremes	.65	.65
Functional at Temperature Extremes	.65	.65
AC at Temperature Extremes	1.5	1.5

Military Programs

Monolithic Memories has participated in the Trident Missile program since 1975. This participation has involved two manufacturing concepts for the production of components of the highest reliability.

Controlled Line — This concept place Monolithic Memories manufacturing documentation and equipment under customer control and concurrence with any change.

Captive Line — This concept defines the equipment and controls supplies to be used. Monolithic Memories documents the systems and provides the semiconductor expertise. The customer controls the Process Documentation.

The Military Programs Department is involved in TRIDENT, DISCUSS, MX, F-18, MK500, and various NASA/SPACE PROGRAMS are trademarks of PAL and The Programmable Solution. Our products have the capability of meeting full radiation requirements of neutron, gamma dot and ionizing environments.

Our facility has DOD clearance and we have the capability to participate in customer analysis of our designs. These analyses may lead to design changes which enhance the product capability in hostile environments. Products which have been qualified for these advanced programs are:

5301 — 1K NiCR PROM
5300 — 1K Gold PROM
5341 — 4K NiCR PROM
5206 — 2K ROM (5306 NiCR PROM Equivalent)
5341 — 4K PROM
5381 — 8K PROM

By the very nature of demanding markets we serve, quality must be inherent in every Monolithic Memories product. It is our conviction that quality derives from a state of mind; that is, it is possible to product fine products only if the quality standards throughout the organization are uniformly high. At Monolithic Memories, we work at weaving quality into the entire company culture so that it shall not be necessary to try and add it on at the end of a manufacturing process by redundant testing or inspection procedures.

Military Products

Monolithic Memories' Hi-Reliability Program offers a broad line of industry standard Bipolar LSI components processed and tested to Military standards. All Hi-Reliability products can be purchased screened to Classes B or C of MIL-STD-883B, Method 5004.

Screening Options

PROCESS LEVEL	PART MARKING
MIL-STD-883 Method 5004 and 5005 Level B	883B (Suffix)
MIL-STD-883 Method 5004 and 5005 Level C	883C (Suffix)
MIL-STD-883 Method 5004 Modified	B (Suffix)

Monolithic Memories "883B"

This part receives full screening and quality conformance inspection to MIL-STD-883 per Method 5004 and 5005 Level B. It is a cost effective alternative to achieve "JAN" type product. Parts screened to this level are used industry wide and are established as very high reliability product.

Monolithic Memories "883C"

This part receives full screening and quality conformance inspection per MIL-STD-883 Method 5004 and 5005 Level C. It is a high quality military processed part to be used when there is no burn-in requirement. Or it can be upgraded to a full Level B processed product.

Monolithic Memories "B"

This part is processed to MIL-STD-883 Method 5004 Level B with modified final testing. It is a cost effective Level B product, which has passed Method 5005 Table I, statistical sampling over the full temperature range plus a self imposed PDA of less than 10%.

Other Hi-Rel Capability

In addition to the broad line of military components offered by Monolithic Memories, we have additional capability to process produce products to extreme reliability standards.

SEM to MIL-STD-883 Method 2018

Particle-induced noise testing to MIL-STD-883 Method 2020

X-ray to MIL-STD-883 Method 2012

Non-destructive bond-pull

Read and record and Delta computation

Statistical parameter plots, signals, mean and median distribution.

Fully documented custom flows to control baselines.

Currently, Monolithic Memories' Sunnyvale, California facility holds certification on both a "controlled" and "captive" facility for the TRIDENT Program. This is in addition to certification to MIL-M-38510 by DESC.

Screening

100% PROCESS FLOW	PROCESS PART MARKING		
	883B	883C	B
Wafer Test:			
Temperature Correlated Test @ 25° C	X	X	X
Internal Visual Inspection:			
2010B and MIL-M-38510	X	X	
Rebond Criteria 2010B Inspection Criteria	X	X	X
Quality Control Gate:			
At 100% Die Inspection	X	X	X
After Bond	X	X	X
After Seal	X	X	X
Stabilization Bake: Method 1008, Condition C, 24 hours	X	X	X
Constant Acceleration: Method 2001, Condition E	X	X	X
Gross Leak: Method 1014, Condition C	X	X	X
Temperature Cycle: Method 1010 Conditioning 10 cycles	X	X	X
Visual Inspection: For Assembly Related Failures	X	X	X
Interim Test:			
Temp Correlated Tests 25°C D.C.; A.C.* & Functional	X	X	X
Programming (when required)	X	X	X
Burn-In-Method 1015, T_A = +125° C, 160 hours			
Condition C, Unprogrammed PROM/PAL	X		X
Condition D, FIFO, Programmed PAL/HAL/ROM	X		X
Condition B, Octal Interface	X		X
Electrical Tests: D.C., A.C.* & Functional			
100% @ TA + 25°C	X	X	X
PDA 10%	X		X
100% Maximum Rated Temperature	X		
100% Minimum Rated Temperature	X		

Inspection

QUALITY CONFORMANCE INSPECTION MIL-STD-883 Method 5005	PROCESS PART MARKING		
	883B	883C	B
Group A: Performed on Every Lot & Sublot			
Subgroup 1, 2, 3, 7 and 9*	X	X	X
Subgroup 10* and 11* When Required	X	X	X
Group B:			
Each Inspection Lot — Condition for Shipment	X	X	
Summary Data Available			X
Group C:			
Performed Upon Request	X	X	X
Generic Data (within six months)	X	X	X
Group D:			
Performed Upon Request	X	X	X
Generic Data (within one year)	X	X	X

*A.C. (switching) tests do not apply to unprogrammed devices. Monolithic Memories Programmable Products are designed with special circuitry to verify A.C. specifications.

Controls

RELIABILITY SYSTEM CONTROLS	PROCESS PART MARKING		
	883B	883C	B
Monolithic Memories Quality System Based on MIL-M-38510 Appendix A Domestic and Offshore Build	X	X	X
MIL-M-38510 Structured Qualification Group A, B, C, and D Monolithic Memories Imposed for Product Approval	X	X	X
Tracebility-MIL-M-38510 Para. 3.1.3a	X	X	X

AMD

AMD	MMI
AM27S18	6330-1
AM27S19	6331-1
AM29S20	63S140 & 63LS140 6300-1
AM27S21	63S141 & 63LS141 6301-1
AM27S12	63S240 & 63LS240 6305-1
AM27S13	63S241 & 63LS241 6306-1
AM27S28	6348-1, -2
AM27S29	6349-1, -2
AM27S30	6340-1, -2
AM27S31	6341-1, -2
AM27S32	6352-1
AM27S33	6353-1
AM27S180	6380-1, -2
AM27S181	6381-1, -2
AM27S184	6388-1
AM27S185	6389-1, -2

FAIRCHILD

FAIRCHILD	MMI
93417	63S140 & 63LS140 6300-1
93427	63S141 & 63LS141 6300-1
93436	63S240 & 63LS240 6305-1
93446	63S241 & 63LS241 6306-1
93438	6340-1, -2
93448	6341-1, -2
93452	6352-1
93453	6353-1
93450	6380-1, -2
93451	6381-1, -2
93514	6388-1
93515	6389-1, -2

HARRIS

HARRIS	MMI
7602	6331-1
7603	6331-1
7610	6300-1, 63S140 & 63LS140
7611	6301-1, 63S141 & 63LS141
7620	6305-1, 63S240 & 63LS240
7621	6306-1, 63S241 & 63LS241
7648	6348-1, -2
7649	6349-1, -2
7640	6340-1, -2
7641	6341-1, -2
7642	6352-1
7643	6353-1
7680	6380-1, -2
7681	6381-1, -2
7684	6388-1
7685	6389-1, -2

INTEL

INTEL	MMI
3608	6380-1, -2
3628	6381-1, -2

INTERSIL

INTERSIL	MMI
5600	6330-1
5603A	6300-1, 63S140 & 63LS140
5604	6305-1, 63S240 & 63LS240
5610	6331-1
5623	6301-1, 63S141 & 63LS141
5624	6306-1, 63S241 & 63LS241

MOTOROLA

MOTOROLA	MMI
MCM 7620	6305-1, 63S240 & 63LS240
MCM 7621	6306-1, 63S241 & 63LS241
MCM 7640	6340-1, -2
MCM 7641	6341-1, -2
MCM 7642	6352-1
MCM 7643	6353-1
MCM 7680	6380-1, -2
MCM 7681	6381-1, -2
MCM 7684	6388-1
MCM 7685	6389-1, -2

NATIONAL

NATIONAL	MMI
DM74S188	6330-1
DM74S288	6331-1
DM74S287	6300-1, 63S140 & 63LS140
DM74S387	6301-1, 63S141 & 63LS141
DM74S470	6308-1
DM74S471	6309-1
DM74S472	6349-1, -2
DM74S473	6348-1, -2
DM74S570	6305-1, 63S240 & 63LS240
DM74S571	6306-1, 63S241 & 63LS241
DM74S572	6352-1
DM74S573	6353-1
DM87S180	6381-1, -2
DM87S181	6380-1, -2
DM74S475 DM87S295	6340-1, -2
DM74S474 DM87S296	6341-1, -2
DM87S184	6388-1
DM87S185	6389-1, -2

RAYTHEON

RAYTHEON	MMI
29600	6308-1
29601	6309-1
29610	6305-1, 63S240 & 63LS240
29611	6306-1, 63S241 & 63LS241
29620	6348-1, -2
29621	6349-1, -2
29624	6340-1, -2
29625	6341-1, -2
29602	6308-1
29603	6309-1
29612	6305-1, 63S240 & 63LS240
29613	6306-1, 63S241 & 63LS241
29622	6348-1, -2
29623	6349-1, -2
29626	6340-1, -2
29627	6341-1, -2
29640	6252-1

RAYTHEON

RAYTHEON	MMI
29641	6253-1
29630	6380-1, -2
29631	6381-1, -2
29660/62	6300-1, 63S140 & 63LS140
29661/63	6301-1, 63S141 & 63LS141
2950/52	6388-1
29651/53	6389-1, -2

SIGNETICS

SIGNETICS	MMI
N82S23	6330-1
N82S123	6331-1
N82S126	6300-1, 63S140 & 63LS140
N82S129	6301-1, 63S141 & 63LS141
N82S130	6305-1, 63S240 & 63LS240
N82S131	6306-1, 63S241 & 63LS241
N82S146	6348-1, -2
N82S147	6349-1, -2
N82S137	6353-1
N82S140	6340-1, -2
N82S141	6341-1, -2
N82S181	6381-1, -2
N82S185	6389-1, -2

TI

OLD NUMBERS

TI	MMI
SN74S188	6330-1
SN74S287	6301-1, 63S141 & 63LS141
SN74S288	6331-1
SN74S387	6300-1, 63S140 & 63LS140
SN74S470	6308-1
SN74S471	6309-1
SN74S472	6349-1, -2
SN74S473	6348-1, -2
SN74S474	6341-1, -2
SN74S475	6340-1, -2
SN74S477	6352-1
SN74S476	6353-1
SN74S478	6381-1, -2
SN74S479	6380-1, -2
SN74S455	6388-1
SN74S454	6389-1, -2

TI

NEW NUMBERS

TI	MMI
TBP18SA030	6330-1
TBP18S030	6331-1
TBP14S10	6301-1, 63S141 & 63LS141
TBP14SA10	6300-1, 63S140 & 63LS140
TBP18SA22	6308-1
TBP18S22	6309-1
TBP18S42	6349-1, -2
TBP18SA42	6348-1, -2
TBP18S46	6341-1, -2
TBP18SA46	6340-1, -2
TBP24SA41	6352-1
TBP24S41	6353-1
TBP28S86	6381-1, -2
TBP28SA86	6380-1, -2
TBP24SA81	6388-1
TBP24S81	6389-1, -2

Bipolar PROM Cross-Reference Guide

MEMORY DESCRIPTION				MMI	AMD	FAIR-CHILD	HARRIS	INTEL	INTERSIL	MOTOROLA	NATIONAL	RAYTHEON	SIGNETICS	TI
SIZE	ORGANIZATION	PINS	OUTPUT											
256	32x8	16	OC	**6330-1**	27S18 29750	—	7602	—	5600	—	74S188	—	82S23	18SA030 74S188
			TS	**6331-1**	27S19 29751	—	7603	—	5610	—	74S288	—	82S123	18S030 74S288
1024	256x4	16	OC	**6300-1 63S140 63LS140**	27S20 29760	93417	7610	—	5603A	—	74S287	29660/62	82S126	14SA10 74S387
			TS	**6301-1 63S141 63LS141**	27S21 29761	93427	7611	—	5623	—	74S387	29661/63	82S129	14S10 74S287
2048	256x8	20	OC	**6308-1**	—	—	—	—	—	—	74S470	29600/02	—	18SA22 74S470
			TS	**6309-1**	—	—	—	—	—	—	74S471	29601/03	—	18S22 74S471
		24	OC	**6335-1**	—	—	7629	—	—	—	—	—	82S114	—
			TS	**6336-1**	—	—	—	—	—	—	—	—	—	—
2048	512x4	16	OC	**6305-1 63S240 63LS240**	27S12 29770	93436	7620	—	5604	7620	74S570	29610/12	82S130	—
			TS	**6306-1 63S240 63LS240**	27S13 29771	93446	7621	—	5624	7621	74S571	29611/13	82S131	—
4096	512x8	20	OC	**6348-1, -2**	27S28	93438	7648	—	—	—	74S473	29620/22	82S146	18SA42 74S473
			TS	**6349-1, -2**	27S29	93448	7649	—	—	—	74S472	29621/23	82S147	18S42 74S472
4096	512x8	24	OC	**6340-1, -2**	27S30	—	7640	—	—	7640	74S475	2924/26	—	18SA46 74S475
			TS	**6341-1, -2**	27S31	—	7641	—	—	7641	74S474	29625/27	82S141	18S46 74S474
4096	1024x4	18	OC	**6352-1**	27S32	93452	7642	—	—	7642	74S572	29640	—	24SA41 74S477
			TS	**6353-1**	27S33	93453	7643	—	—	7643	74S573	29641	82S137	24S41 74S76
4096	1024x4	18	TS	**63RA441**	—	—	—	—	—	—	—	—	—	—
8192	1024x8	24	OC	**6380-1, -2**	27S180	93450	7680	3608	—	7680	87S180	29630	—	28SA86 74S479
			TS	**6381-1, -2**	27S181	93451	7681	3628	—	7681	87S181	29631	82S181	28S586 74S478
8192	2048x4	18	OC	**6388-1**	27S184	93514	7684	—	—	7684	87S184	29650/52	—	24SA81 74S455
			TS	**6389-1, -2**	27S185	93515	7685	—	—	7685	87S185	29651/53	82S185	24S81 74S454

Note: Only commercial specification part numbers are listed.

Generic NiCR PROM Family

53/63XX-1

Features/Benefits

- Standard Schottky processing
- Reliability proven nichrome fusible links (qualified for MIL-M-38510)
- PNP inputs for low input current
- Compatible pin configurations for upward expansion
- 4-bit-wide and 8-bit-wide for byte oriented applications

Application

- Microprogram store
- Microprocessor program store
- Look up table
- Character generator
- Random logic
- Code converter

Description

The 53/63XX-1-series generic PROM family offers the widest selection of sizes and organizations available in the industry. The 4-bit wide PROMs range from 256x4 to 2048x4 and feature upward/downward pin out compatibility in the space saving 16 and 18 pin packages. The 8-bit wide PROMs range from 32x8 to 1024x8 in a wide selection of package sizes including the space saving SKINNYDIP™ 24-pin .300 inch wide package. All PROMs have the same programming specifications allowing a single generic programmer.

The family features low input current PNP inputs, full Schottky clamping, three-state and open collector outputs. The nichrome fuses store a logical high and are programmed to the low state. Special on chip circuitry and extra fuses provide preprogramming tests which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

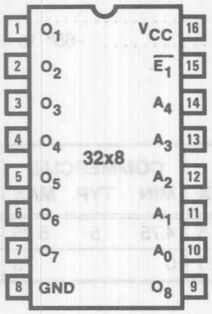
Generic PROM Selection Guide

MEMORY			PACKAGE	DEVICE TYPE		
SIZE	ORGANIZATION			COMMERCIAL	MILITARY	
1K	256x4	OC	J16, F16	6300-1	5300-1	4-bit-wide
		TS		6301-1	5301-1	
2K	512x4	OC	J16, F16	6305-1	5305-1	
		TS		6306-1	5306-1	
4K	1024x4	OC	J18, F18	6350-1	5350-1	
		TS		6351-1	5351-1	
		OC		6352-1	5352-1	
		TS		6353-1	5353-1	
8K	2048x4	OC	J18	6388-1	5388-1	
		TS		6389-1	5389-1	
1/4K	32x8	OC	J16, F16	6330-1	5330-1	8-bit-wide
		TS		6331-1	5331-1	
2K	256x8	OC	J20, F20	6308-1	5308-1	
		TS		6309-1	5309-1	
		OC	J24	6335-1		
		TS		6336-1		
4K	512x8	OC	J24, F24	6340-1	5340-1	
		TS		6341-1	5341-1	
		OC	J20, F20	6348-1	5348-1	
		TS		6349-1	5349-1	
8K	1024x8	OC	J24, JS24*	6380-1	5380-1	
		TS		6381-1	5381-1	

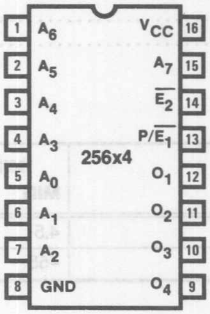
**JS is the .300 inch wide SKINNYDIP™ package.*

Pin Configurations

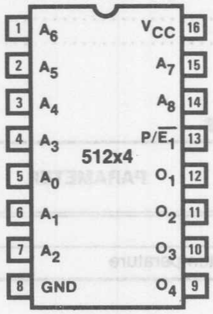
53/6330-1
53/6331-1



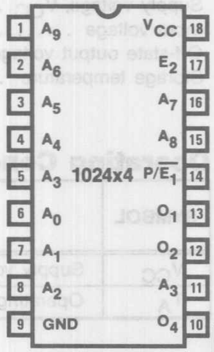
53/6300-1
53/6301-1



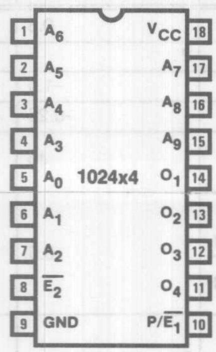
53/6305-1
53/6306-1



53/6350-1
53/6351-1



53/6352-1
53/6353-1



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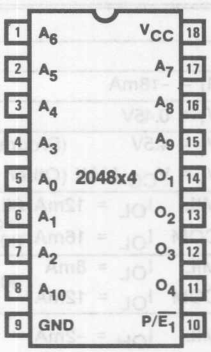
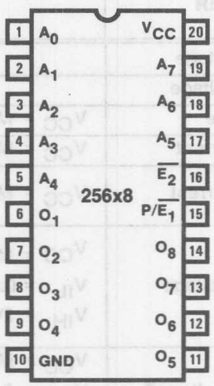
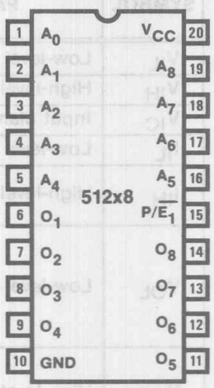


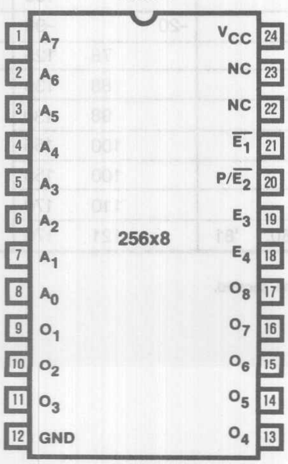
53/6308-1
53/6309-1



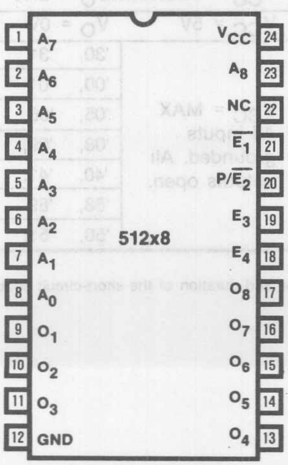
53/6348-1
53/6349-1



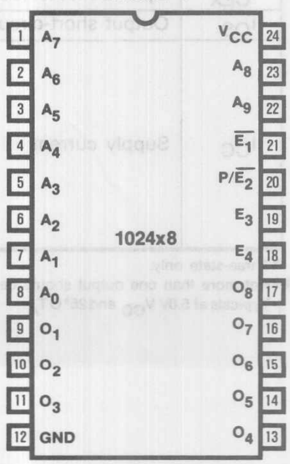
6335-1
6336-1



53/6340-1
53/6341-1



53/6380-1
53/6381-1



Supply voltage, V_{CC}	7V
Input voltage	7V
Off-state output voltage	5.5V
Storage temperature	-65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18mA				-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45V				-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 4.5V (Program pin) V_I = V_{CC} MAX (Other inputs)				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OL} = 12mA COM I_{OL} = 16mA	All PROMs except '30,'31,'80,'81			0.5	V
			MIL I_{OL} = 8mA COM I_{OL} = 12mA	'30,'31,'80,'81				
V_{OH}	High-level output voltage*	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = -2mA COM I_{OH} = -3.2mA		2.4			V
I_{OZL}	Off-state output current*	V_{CC} = MAX	V_O = 0.5V				-100	μA
I_{OZH}			V_O = 2.4V				100	μA
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4V				100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5V	V_O = 0V		-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX All inputs grounded. All outputs open.	'30, '31			78	125	mA
			'00, '01			88	130	
			'05, '06			98	130	
			'08, '09, '35, '36			100	155	
			'40, '41, '48, '49			100	155	
			'88, '89			110	170	
			'50, '51, '52, '53, '80, '81			121	175	

*Three-state only.

**Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0V V_{CC} and 25°C T_A.

Switching Characteristics

Over Commercial Operating Conditions

DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME		t_{EA} AND t_{ER} (ns) ENABLE ACCESS AND RECOVERY TIME		CONDITIONS (See standard test load)	
	TYP †	MAX	TYP †	MAX	R1(Ω)	R2(Ω)
6300-1, 6301-1	32	55	15	30	300	600
6305-1, 6306-1	44	60	17	30		
6308-1, 6309-1	39	70	14	30		
6335-1, 6336-1	52	70	17	30		
6340-1, 6341-1	52	70	17	30		
6348-1, 6349-1	52	70	17	30		
6350-1, 6351-1	43	60	15	30		
6352-1, 6353-1	43	60	15	30		
6388-1, 6389-1	49	70	19	30		
6330-1, 6331-1	37	50	21	30	375	750
6380-1, 6381-1	54	90	18	40		

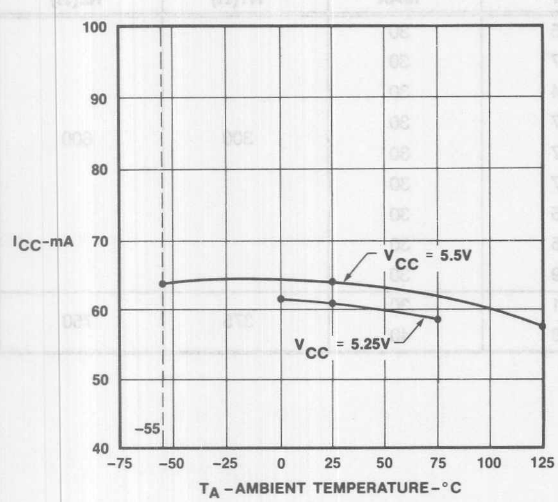
Over Military Operating Conditions

DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME		t_{EA} AND t_{ER} (ns) ENABLE ACCESS AND RECOVERY TIME		CONDITIONS (See standard test load)	
	TYP †	MAX	TYP †	MAX	R1(Ω)	R2(Ω)
5300-1, 5301-1	32	75	15	40	300	600
5305-1, 5306-1	44	75	17	40		
5308-1, 5309-1	39	80	14	40		
5335-1, 5336-1	52	80	17	40		
5340-1, 5341-1	52	80	17	40		
5348-1, 5349-1	52	80	17	40		
5350-1, 5351-1	43	75	15	40		
5352-1, 5353-1	43	75	15	40		
5388-1, 5389-1	49	100	19	40		
5330-1, 5331-1	37	60	21	40	375	750
5380-1, 5381-1	54	125	18	40		

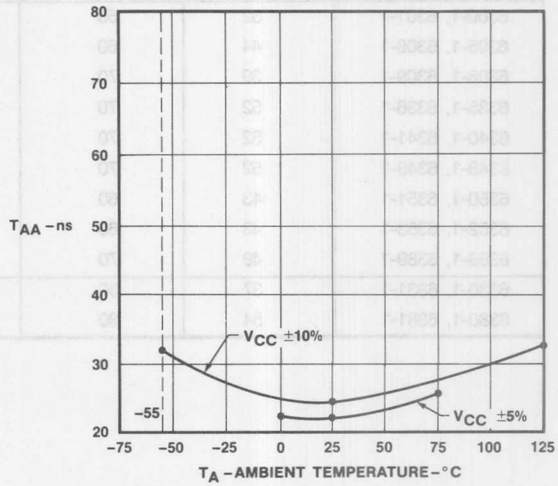
†Typicals at 5.0V V_{CC} and 25°C T_A

6331
5331

Typical I_{CC} vs Temperature

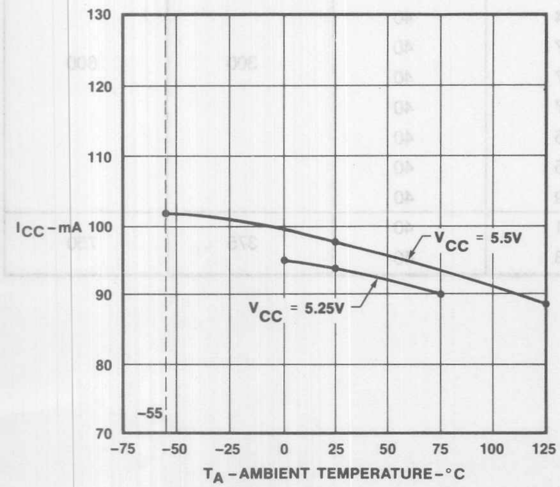


Typical T_{AA} vs Temperature

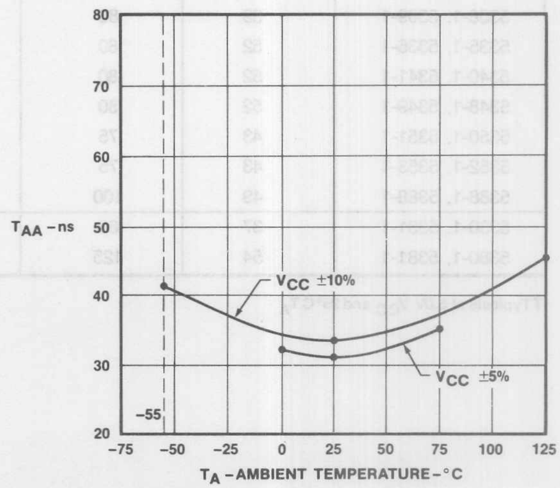


6301
5301

Typical I_{CC} vs Temperature

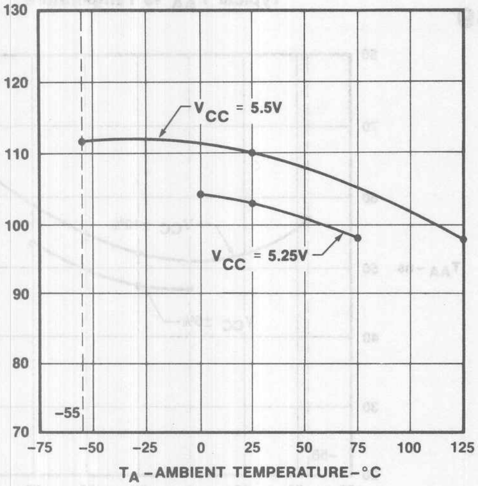


Typical T_{AA} vs Temperature

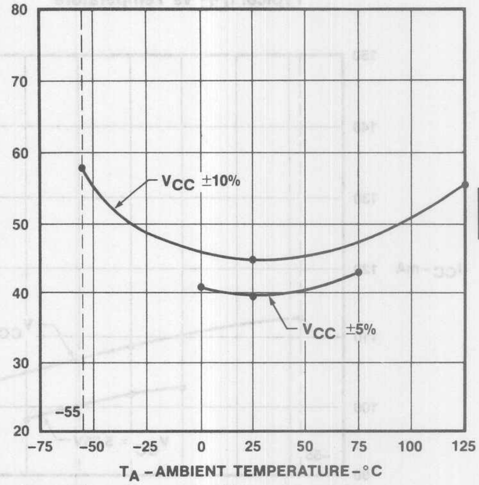


6306
5306

Typical I_{CC} vs Temperature

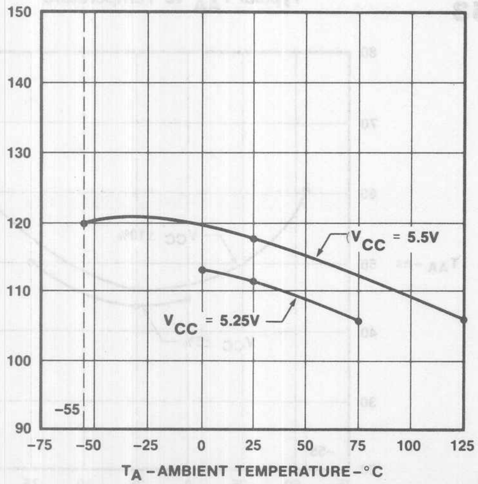


Typical T_{AA} vs Temperature

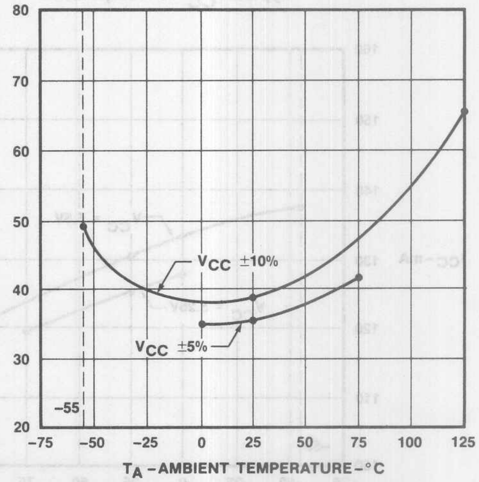


6309
5309

Typical I_{CC} vs Temperature



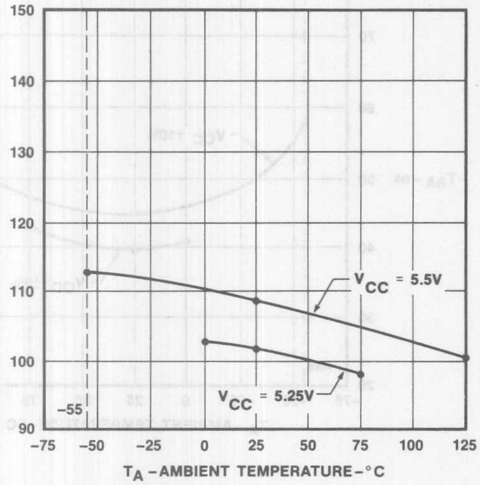
Typical T_{AA} vs Temperature



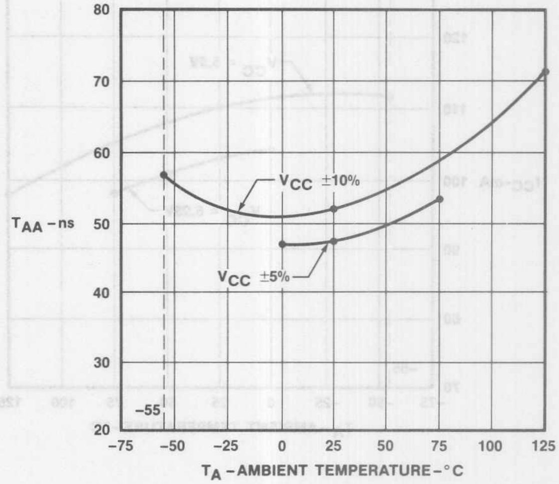
Typical Characteristics

6341
6349
5336
5341
5349

Typical I_{CC} vs Temperature

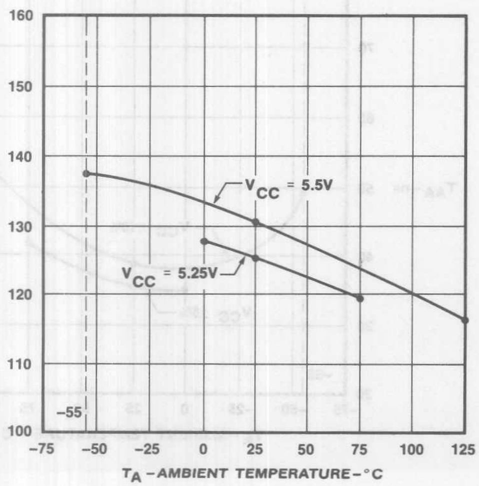


Typical T_{AA} vs Temperature

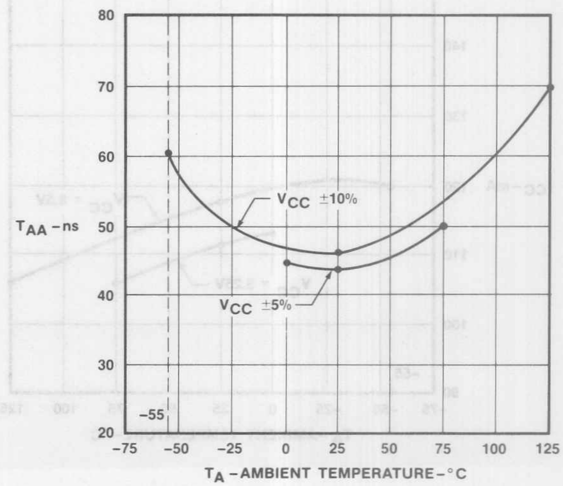


6351
6353
5351
5353

Typical I_{CC} vs Temperature

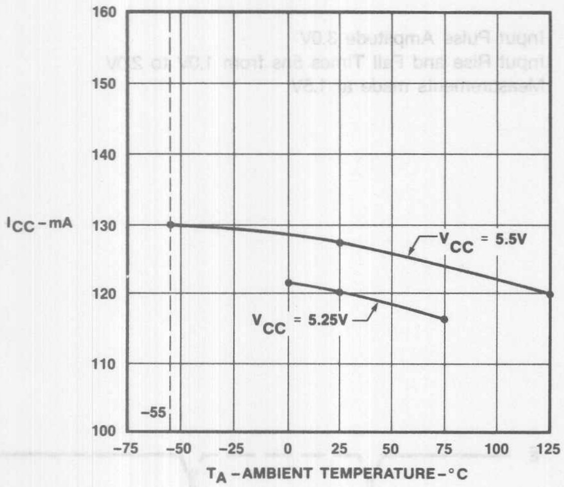


Typical T_{AA} vs Temperature

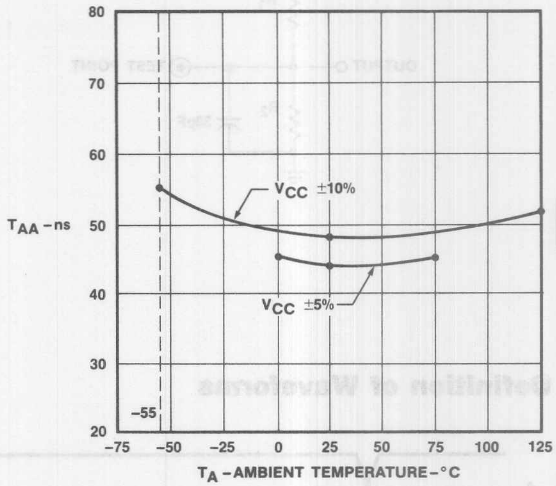


6389
5389

Typical I_{CC} vs Temperature

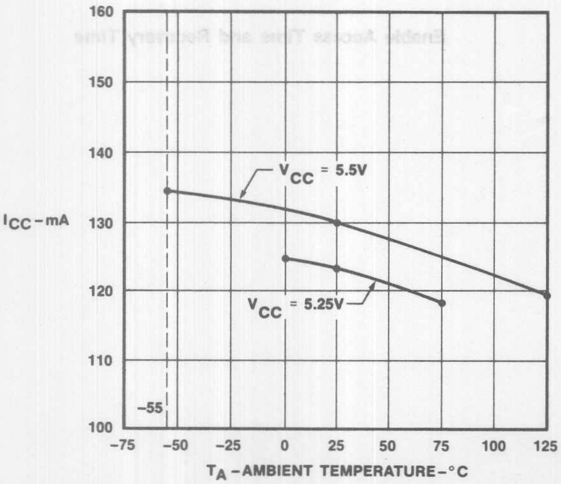


Typical T_{AA} vs Temperature

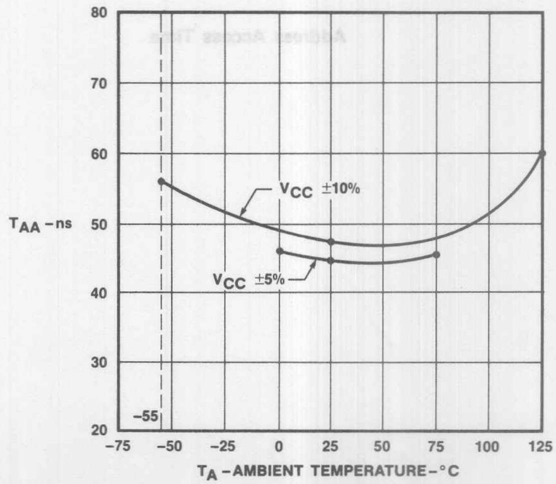


6381
5381

Typical I_{CC} vs Temperature

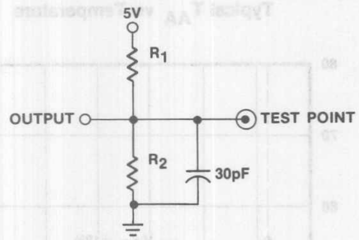


Typical T_{AA} vs Temperature



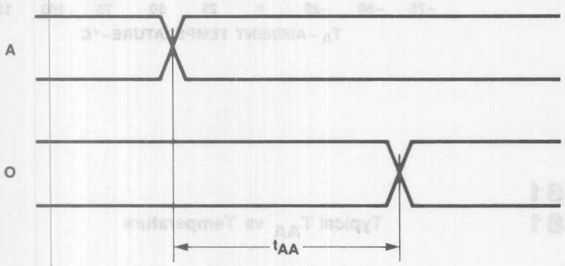
NOTE: Typical characteristic curves are for three-state devices. Equivalent open collector devices decrease in I_{CC} approximately 10 mA and increase in T_{AA} approximately 6 ns.

Standard Test Load

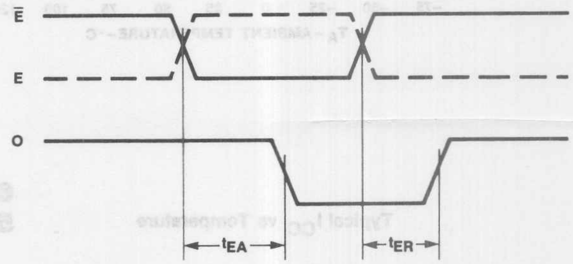


Input Pulse Amplitude 3.0V
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements made at 1.5V

Definition of Waveforms



Address Access Time



Enable Access Time and Recovery Time

High Performance 512x8 NiCr PROM

53/6340-2 53/6341-2

Features

- 4096 bit memory
- 55 ns max access time
- Reliability proven NiCr Fusible Links
- Available in 24-pin SKINNYDIP™
- Industry standard pin out

Applications

- Microprogram store
- Program store
- Look up table
- Programmable logic element
- Character generator

Description

The 6340/1-2 is a high speed 512x8 PROM which uses industry standard pin out. In addition, the device is available in the 24-pin (0.3 in.) SKINNYDIP™.

The family features low input current PNP inputs, full Schottky clamping, three-state and open collector outputs. The nichrome fuses store a logical high and are programmed to the low state. Special on-chip circuitry and extra fuses provide preprogramming tests which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Programming

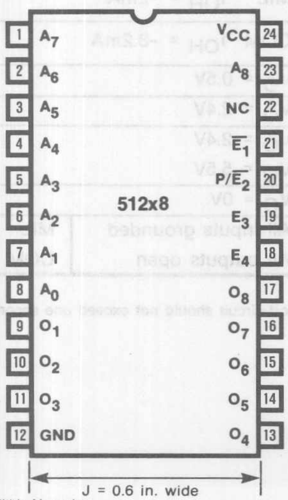
This PROM is programmed with the same programming algorithm as all other NiCr PROMs.

3

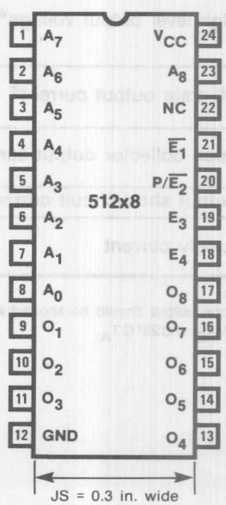
Ordering Information

MEMORY			PACKAGE		COMMERCIAL		MILITARY	
SIZE	ORGANIZATION		PINS	TYPE	PART NUMBER	MAX TAA	PART NUMBER	MAX TAA
4K	512x8	OC	24	J, JS	6340-2	70 ns	5340-2	90 ns
		TS			6341-2	55 ns	5341-2	70 ns

Pin Configurations



53/6340-2
53/6341-2



SKINNYDIP is a registered trademark of Monolithic Memories

Absolute Maximum Ratings

Supply voltage, V_{CC}	7V
Input voltage	7V
Off-state output voltage	5.5V
Storage temperature	-65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature	–55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA				-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45V				-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 4.5V (Program pin) V_I = V_{CC} MAX (Other pins)				40	µA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OL} = 12mA COM I_{OL} = 16mA				0.5	V
V_{OH}	High-level output voltage*	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = -2mA COM I_{OH} = -3.2mA		2.4			V
I_{OZL}	Off-state output current*	V_{CC} = MAX	V_O = 0.5V				-40	µA
I_{OZH}			V_O = 2.4V				40	µA
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4V V_O = 5.5V				40 100	µA
I_{OS}	Output short-circuit current**	V_{CC} = 5V	V_O = 0V		-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX	All inputs grounded All outputs open	MIL		120	175	mA
				COM		120	155	

*Three-state only.

**Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0V V_{CC} and 25°C T_A.

Switching Characteristics

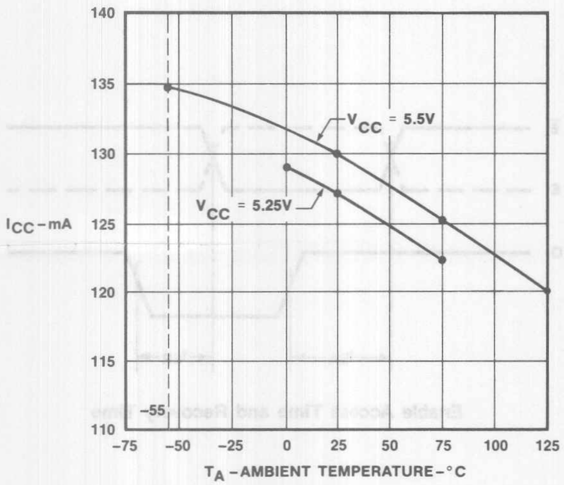
Over operating conditions

DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME		t_{EA} AND t_{ER} (ns) ENABLE ACCESS AND RECOVERY TIME		CONDITIONS (See standard test load)	
	TYP†	MAX	TYP	MAX	R1(Ω)	R2(Ω)
6340-2	49	70	19	30	300	600
6341-2	45	55	19	30		
5340-2	49	90	19	40		
5341-2	45	70	19	40		

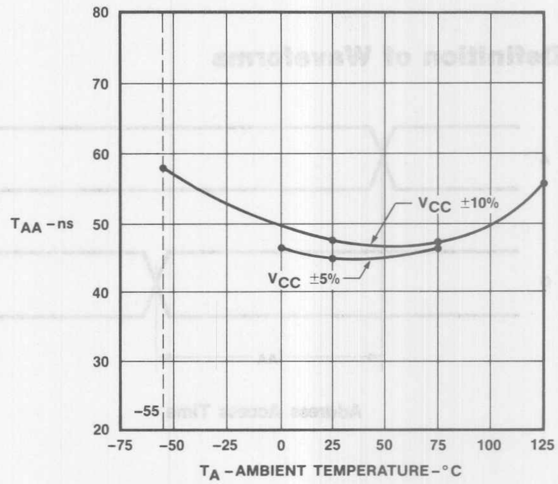
†Typicals at 5.0V V_{CC} and 25°C T_A.

3

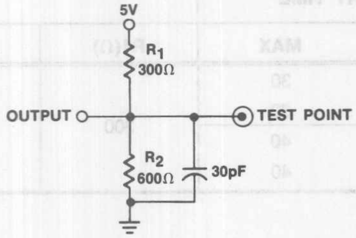
Typical I_{CC} vs Temperature



Typical T_{AA} vs Temperature

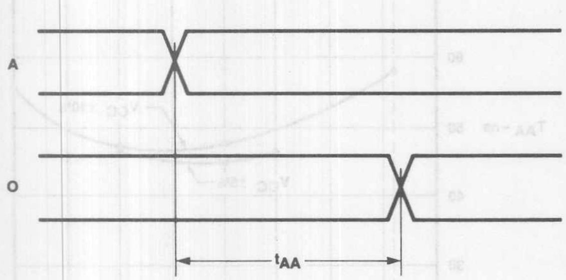


Standard Test Load

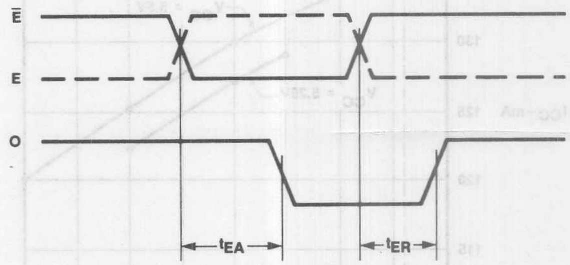


Input Pulse Amplitude 3.0V
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements made at 1.5V

Definition of Waveforms



Address Access Time



Enable Access Time and Recovery Time

High Performance 512x8 NiCr PROM

53/6348-2 53/6349-2

Features:

- 4096 bit memory
- 55 ns max access time
- Reliability proven NiCr Fusible Links
- Industry standard 20 pin out configuration

Applications

- Microprogram store
- Program store
- Look up table
- Programmable logic element
- Character generator

Description

The 6348/9 is a high speed 512x8 PROM which uses industry standard pin out.

The family features low input current PNP inputs, full Schottky clamping, three-state and open collector outputs. The nichrome fuses store a logical high and are programmed to the low state. Special on-chip circuitry and extra fuses provide preprogramming tests which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Programming

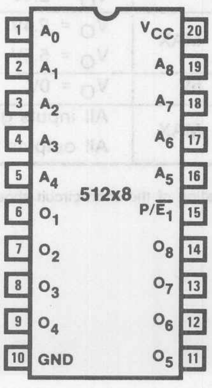
This PROM is programmed with the same programming algorithm as all other NiCr PROMs.

Ordering Information

MEMORY			PACKAGE		COMMERCIAL		MILITARY	
SIZE	ORGANIZATION		PINS	TYPE	PART NUMBER	MAX TAA	PART NUMBER	MAX TAA
4K	512x8	OC	20	J	6348-2	70 ns	5348-2	90 ns
		TS			6349-2	55 ns	5349-2	70 ns

Pin Configuration

53/6348-2
53/6349-2



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Absolute Maximum Ratings

Supply voltage, V_{CC} 7V
Input voltage 7V
Off-state output voltage 5.5V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 4.5V (Program pin) V_I = V_{CC} MAX (Other pins)			40	µA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OL} = 12mA COM I_{OL} = 16mA			0.5	V
V_{OH}	High-level output voltage*	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = −2mA COM I_{OH} = −3.2mA	2.4			V
I_{OZL}	Off-state output current*	V_{CC} = MAX	V_O = 0.5V			−40	µA
I_{OZH}			V_O = 2.4V			40	µA
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4V			40	µA
			V_O = 5.5V			100	
I_{OS}	Output short-circuit current**	V_{CC} = 5V	V_O = 0V	−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX	All inputs grounded, All outputs open — MIL		120	175	mA
			All inputs grounded, All outputs open — COM		120	155	

*Three-state only.

**Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

†Typicals at 5.0V V_{CC} and 25°C T_A.

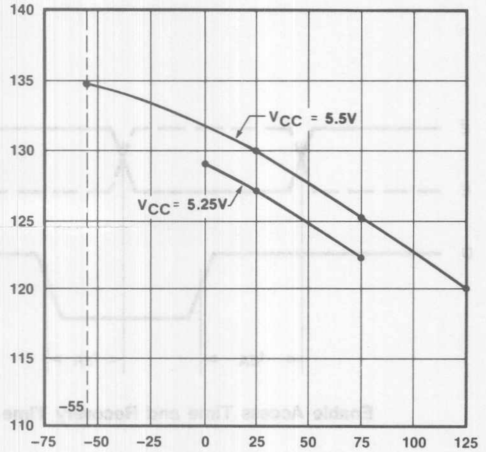
Switching Characteristics

Over Commercial Operating Conditions

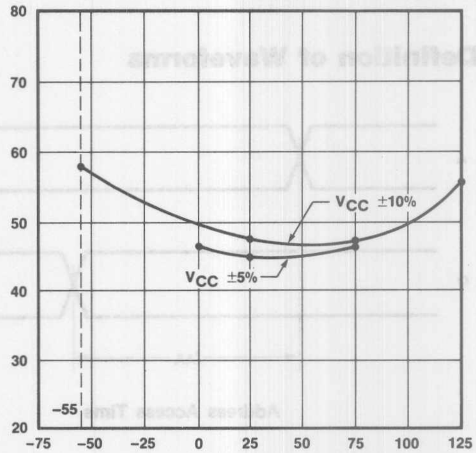
DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME		t_{EA} AND t_{ER} (ns) ENABLE ACCESS AND RECOVERY TIME		CONDITIONS (See standard test load)	
	TYP†	MAX	TYP	MAX	R1(Ω)	R2(Ω)
6348-2	49	70	19	30	300	600
6349-2	45	55	19	30		
5348-2	49	90	19	40		
5349-2	45	70	19	40		

†Typicals at 5.0V V_{CC} and 25°C T_A

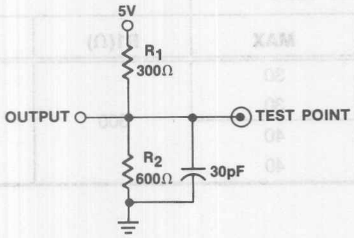
Typical I_{CC} vs Temperature



Typical T_{AA} vs Temperature

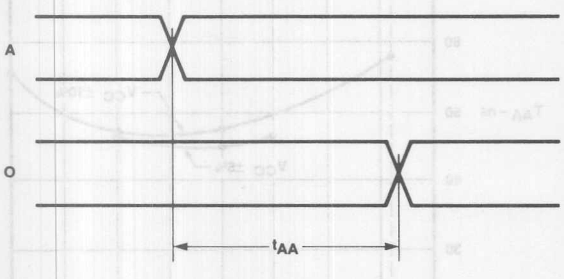


Standard Test Load

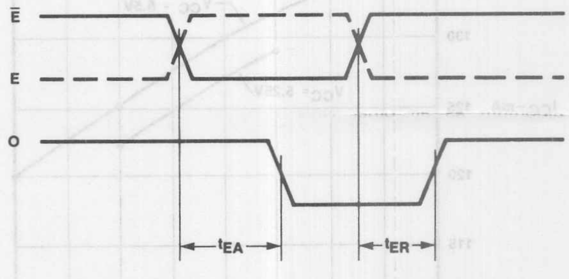


Input Pulse Amplitude 3.0V
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements made at 1.5V

Definition of Waveforms



Address Access Time



Enable Access Time and Recovery Time

High Performance 2048x4 NiCr PROM

53/6389-2

3

Features

- 8192 bit memory
- Three-state outputs
- 55 ns max access time
- Reliability proven NiCr Fusible Links
- Industry standard pin out

Applications

- Microprogram store
- Program store
- Look up table
- Programmable logic element
- Character generator

Programming

This PROM is programmed with the same programming algorithm as all other NiCr PROMs.

Ordering Information

MEMORY		PACKAGE		DEVICE TYPE	
SIZE	**ORGANIZATION**	**PINS**	**TYPE**	**COM**	**MIL**
8K	2048x4	18	J	6389-2	5389-2

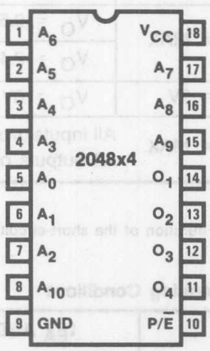
Description

The 6389-2 is a high speed 2Kx4 PROM which uses industry standard pin out.

The family features low input current PNP inputs, full Schottky clamping, three-state outputs. The nichrome fuses store a logical high and are programmed to the low state. Special on-chip circuitry and extra fuses provide preprogramming tests which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Pin Configuration



Absolute Maximum Ratings

Supply voltage, V_{CC} 7V
Input voltage 7V
Off-state output voltage 5.5V
Storage temperature .... –65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA				–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45V				–0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 4.5V (Program pin) V_I = V_{CC} MAX (Other pins)				40	μA
V_{OL}	Low-level output voltage*	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OL} = 12 mA COM I_{OL} = 16 mA				0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} 0.8V V_{IH} = 2V	MIL I_{OH} = –2mA COM I_{OH} = –3.2mA		2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.5V				–40	μA
I_{OZH}	Off-state output current	V_{CC} = MAX	V_O = 2.4V				40	μA
I_{OS}	Output short-circuit current*	V_{CC} = 5V	V_O = 0V		–20		–90	mA
I_{CC}	Supply current	V_{CC} = MAX	All inputs grounded. All outputs open	MIL		110	170	mA
				COM		110	155	mA

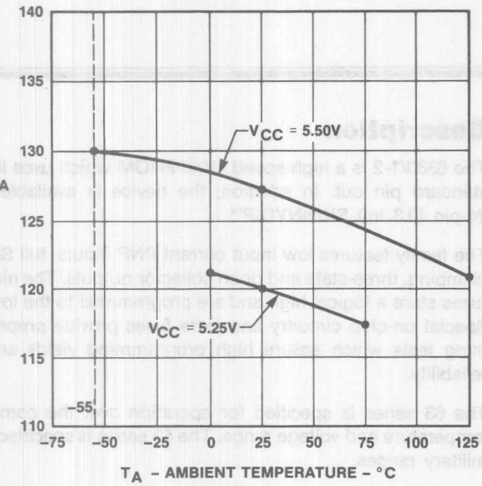
†Typicals at 5.0V V_{CC} and 25°C T_A.

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

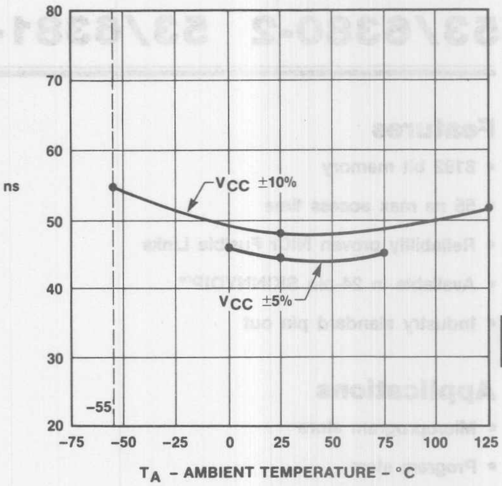
Switching Characteristics Over Operating Conditions

DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME		t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME		CONDITIONS (See standard test load)	
	TYP †	MAX	TYP†	MAX	R1(Ω)	R2(Ω)
6389-2	44	55	19	30	300	600
5389-2	44	70	19	40		

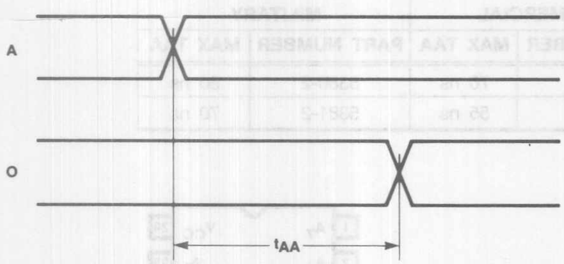
Typical I_{CC} vs Temperature



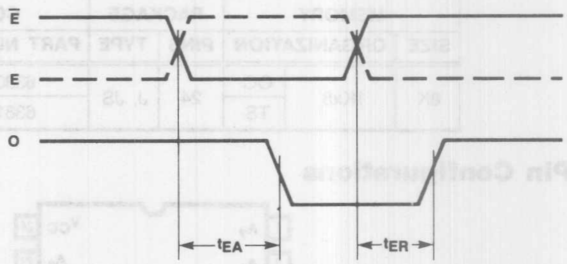
Typical T_{AA} vs Temperature



Definition of Waveforms

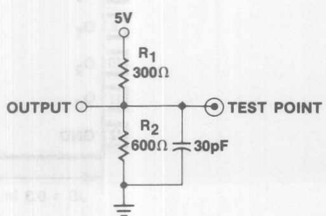


Address Access Time



Enable Access Time and Recovery Time

Standard Test Load



Input pulse amplitude 3.0V
Input rise and fall times 5ns from 1.0V to 2.0V
Measurements made at 1.5V

High Performance 1024x8 NiCr PROM

53/6380-2 53/6381-2

Features

- 8192 bit memory
- 55 ns max access time
- Reliability proven NiCr Fusible Links
- Available in 24-pin SKINNYDIP™
- Industry standard pin out

Applications

- Microprogram store
- Program store
- Look up table
- Programmable logic element
- Character generator

Description

The 6380/1-2 is a high speed 1Kx8 PROM which uses industry standard pin out. In addition, the device is available in the 24-pin (0.3 in.) SKINNYDIP™.

The family features low input current PNP inputs, full Schottky clamping, three-state and open collector outputs. The nichrome fuses store a logical high and are programmed to the low state. Special on-chip circuitry and extra fuses provide preprogramming tests which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

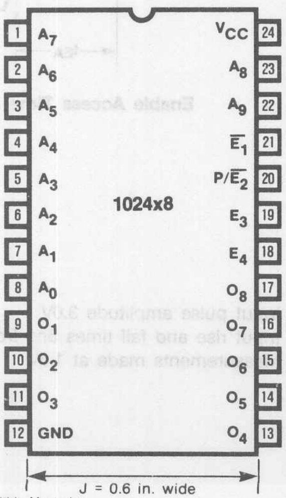
Programming

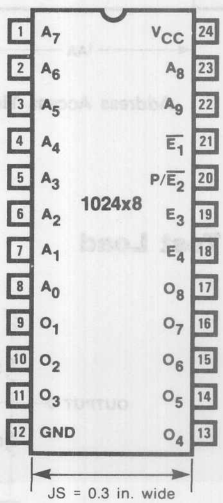
This PROM is programmed with the same programming algorithm as all other NiCr PROMs.

Ordering Information

MEMORY			PACKAGE		COMMERCIAL		MILITARY	
SIZE	ORGANIZATION		PINS	TYPE	PART NUMBER	MAX TAA	PART NUMBER	MAX TAA
8K	1Kx8	OC	24	J, JS	6380-2	70 ns	5380-2	90 ns
		TS			6381-2	55 ns	5381-2	70 ns

Pin Configurations





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Monolithic Memories MMI

Absolute Maximum Ratings

Supply voltage, V_{CC} 7V
Input voltage 7V
Off-state output voltage 5.5V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 4.5V (Program pin) V_I = V_{CC} MAX (Other pins)			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OL} = 12mA COM I_{OL} = 16mA			0.5	V
V_{OH}	High-level output voltage*	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = −2mA COM I_{OH} = −3.2mA	2.4			V
I_{OZL}	Off-state output current*	V_{CC} = MAX	V_O = 0.5V			−40	μA
I_{OZH}			V_O = 2.4V			40	μA
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4V			40	μA
			V_O = 5.5V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5V	V_O = 0V	−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX	All inputs grounded, All outputs open — MIL		120	175	mA
			All inputs grounded, All outputs open — COM		120	170	mA

*Three-state only.
**Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† Typicals at 5.0V V_{CC} and 25°C T_A.

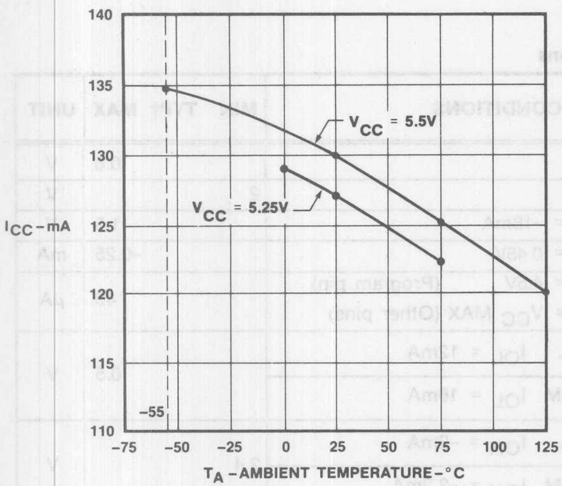
Switching Characteristics

Over Operating Conditions

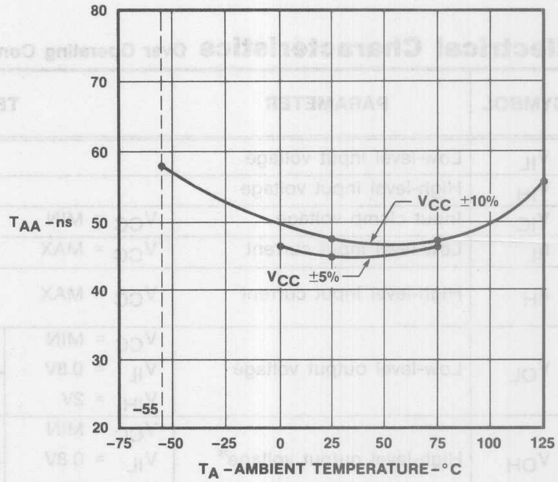
DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME		t_{EA} AND t_{ER} (ns) ENABLE ACCESS AND RECOVERY TIME		CONDITIONS (See standard test load)	
	TYP†	MAX	TYP	MAX	R1(Ω)	R2(Ω)
6380-2	49	70	19	30	300	600
6381-2	45	55	19	30		
5380-2	49	90	19	40		
5381-2	45	70	19	40		

†Typicals at 5.0V V_{CC} and 25°C T_A

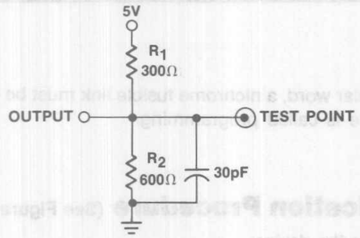
Typical I_{CC} vs Temperature



Typical T_{AA} vs Temperature

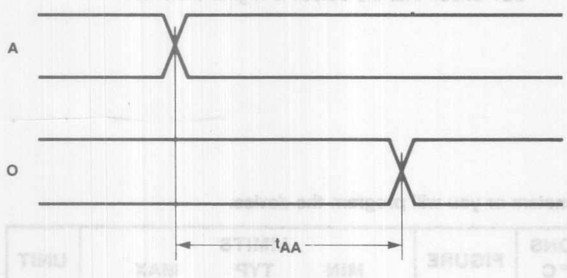


Standard Test Load

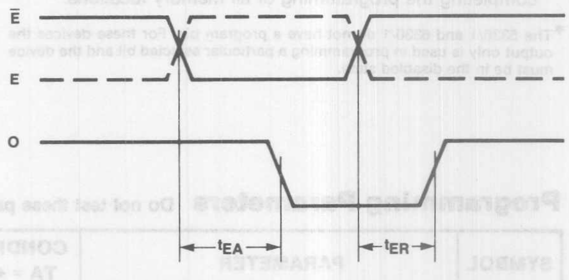


Input Pulse Amplitude 3.0V
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements made at 1.5V

Definition of Waveforms



Address Access Time



Enable Access Time and Recovery Time

NiCr PROM Programming Instructions 53/63XX

Description

The 53/63XX Generic PROM Family is manufactured with outputs high in all storage locations. To make an output low at A particular word, a nichrome fusible link must be opened. This procedure is called programming.

Programming Procedure (See Figure 1)

1. Apply the desired address to the inputs.
2. Enable Inputs may be left at any state.*
3. Apply 5.5V to V_{CC}.
4. Apply V_{PP} to the program pin. (This step is not used on the 32x8 PROM)*.
5. Apply V_{OUT} to the output to be programmed. (Program only one output at a time).
6. Remove V_{OUT}.
7. Remove V_{PP}.
8. Verification may be performed after each bit or word or after completing the programming of all memory locations.

*The 5330/1 and 6330/1 do not have a program pin. For these devices the output only is used in programming a particular selected bit and the device must be in the disabled state.

Verification Procedure (See Figure 2)

1. Enable the device.
2. To verify low-state:
   - 2A. Apply an address where the output should be low.
   - 2B. Apply 4.2V to V_{CC}.
   - 2C. Load the output with I_{OL} = 12 mA.
   - 2D. Check that the output is less than 0.8V.
3. To verify High-state:
   - 3A. Apply an address where the output should be high.
   - 3B. Apply 6V to V_{CC}.
   - 3C. Load the output with I_{OH} = 0.3 mA.
   - 3D. Check that the output is higher than 4.5V.

Programming Parameters **Do not test these parameters or you will program the device.**

SYMBOL	PARAMETER	CONDITIONS TA = +25° C	FIGURE	LIMITS MIN	TYP	MAX	UNIT
t_R	Slew rate of Programming Pulses†			0.3		0.5	V/μs
V_{CCP}	VCC During Programming			5.4	5.5	5.6	V
	Maximum Duty Cycle					25	%
V_{PP}	Programming Voltage on Program Pin*		1	27		33	V
V_{OUT}	Programming Voltage on Output Pin*		1	20		26	V
t_{D1}	Delay between V_{PP} and V_{OUT}		1	0	10	20	μs
t_{D2}				0	0.5	1	
t_p	Pulse width of V_{OUT}		1	10		40	μs
V_{OLV}	V_{OL} during verification	Chip enabled I_{OL} = 12 mA V_{CC} = 4.2V	2			0.8	V
V_{OHV}	V_{OH} during verification	Chip enabled I_{OH} = 0.3 mA V_{CC} = 6V	2	4.5			V

*Voltage supply must be capable of supplying at least 240 mA.

†Leading edge of V_{PP} and V_{OUT}

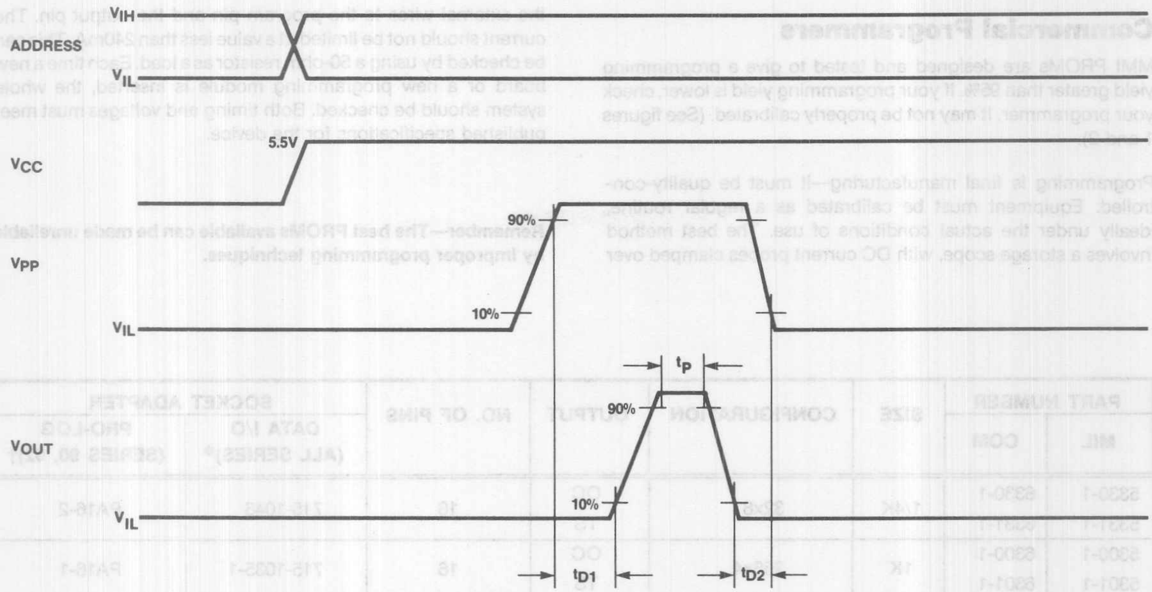


Figure 1. Programming Timing Diagram

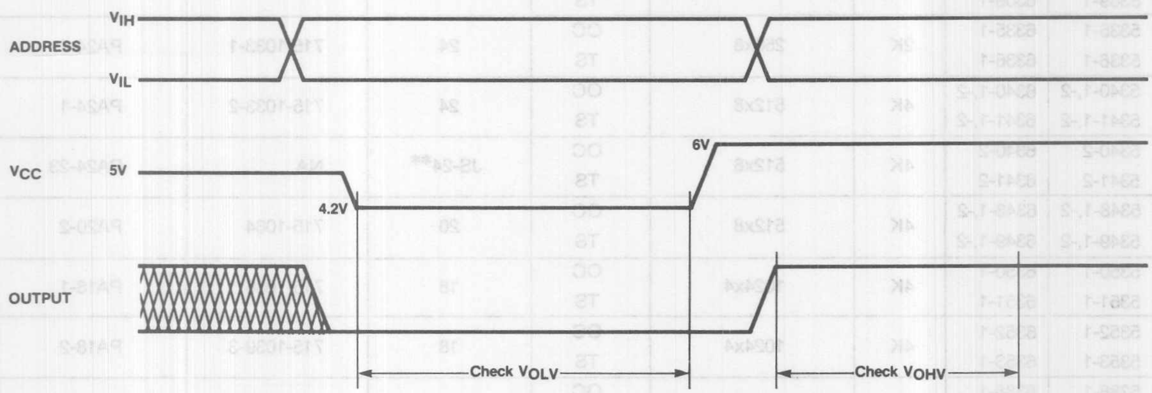


Figure 2. Verification Timing Diagram

Optimized Programming Algorithm

1. Pulse all fuses to be programmed with single, minimum voltage programming pulses (line 1 in the table).
2. Verify all fuses at low V_{CC} (4.2V). During this step, unprogrammed fuses are pulsed up to eight more times (see table).
3. Re-verify at low V_{CC} (4.2V) and high V_{CC} (6V).

PULSE NUMBER	PROGRAM PIN VOLTAGE	OUTPUT VOLTAGE
1 to 3	27V	20V
4 to 6	30V	23V
7 to 9	33V	26V

Commercial Programmers

MMI PROMs are designed and tested to give a programming yield greater than 95%. If your programming yield is lower, check your programmer. It may not be properly calibrated. (See figures 1 and 2).

Programming is final manufacturing—it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. The best method involves a storage scope, with DC current probes clamped over the external wires to the program pin and the output pin. The current should not be limited at a value less than 240mA. This can be checked by using a 50-ohm resistor as a load. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember—The best PROMs available can be made unreliable by improper programming techniques.

PART NUMBER		SIZE	CONFIGURATION	OUTPUT	NO. OF PINS	SOCKET ADAPTER	
MIL	COM					DATA I/O (ALL SERIES)*	PRO-LOG (SERIES 90, 92)†
5330-1 5331-1	6330-1 6331-1	1/4K	32x8	OC TS	16	715-1046	PA16-2
5300-1 5301-1	6300-1 6301-1	1K	256x4	OC TS	16	715-1035-1	PA16-1
5305-1 5306-1	6305-1 6306-1	2K	512x4	OC TS	16	715-1035-2	PA16-1
5308-1 5309-1	6308-1 6309-1	2K	256x8	OC TS	20	715-1028-1	PA20-2
5335-1 5336-1	6335-1 6336-1	2K	256x8	OC TS	24	715-1033-1	PA24-1
5340-1,-2 5341-1,-2	6340-1,-2 6341-1,-2	4K	512x8	OC TS	24	715-1033-2	PA24-1
5340-2 5341-2	6340-2 6341-2	4K	512x8	OC TS	JS-24**	NA	PA24-23
5348-1,-2 5349-1,-2	6348-1,-2 6349-1,-2	4K	512x8	OC TS	20	715-1064	PA20-2
5350-1 5351-1	6350-1 6351-1	4K	1024x4	OC TS	18	715-1036	PA18-1
5352-1 5353-1	6352-1 6353-1	4K	1024x4	OC TS	18	715-1039-3	PA18-2
5388-1 5389-1,-2	6388-1 6389-1,-2	8K	2048x4	OC TS	18	715-1039	PA18-2
5380-1,-2 5381-1,-2	6380-1,-2 6381-1,-2	8K	1024x8	OC TS	24	715-1033-3	PA24-1
5380-1,-2 5381-1,-2	6380-1,-2 6381-1,-2	8K	1024x8	OC TS	JS-24**	NA	PA24-23

*Program card set is 909-1226-1 for all series DATA I/O.
†Personality module is PM 9037 for all PRO-LOG (series 90, 92).
**JS is the 0.3 in. wide SKINNYDIP™ package.

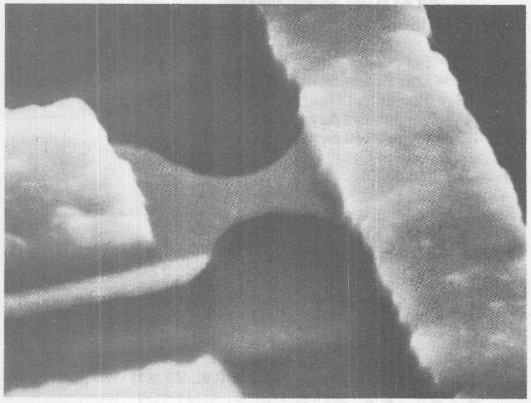
High Performance Ti-W PROMs

Features/Benefits

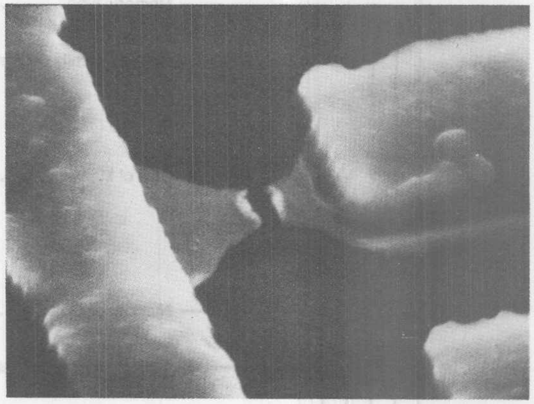
- Reliable Titanium-Tungsten fuses (Ti-W)
- Low voltage programming
- New advanced platinum silicide Schottky process allows designs with fastest speeds over operating temperature ranges
- Upwards pin compatibility in industry standard pin outs (most of which were first introduced by MMI in our Standard Performance PROM family).

New Programming Technique:

Our new HIGH Performance PROMs use an elevated voltage at V_{CC} instead of using a separate programming pin (one of the enables) as in the Standard Performance PROMs using nichrome fuses. Changes in the internal circuitry were made to optimize speed and accordingly the unblown fuse represents a LOW at the output. When a fuse is programmed it reflects a high at the output.*



Unblown Fuse



Blown Fuse

* NOTE: This is opposite to that of our standard performance Schottky PROMs using nichrome fuses.

MMI Part Numbering System

The new system approaches part numbering using the method of keying important attributes of the device. The military/commercial and PROM/ROM numbering system is preserved i.e., 5/6 - 3/2. These two digits are separated from the actual device number by a technology/configuration designator using letters.

"S" = Schottky
"LS" = Low Power Schottky
"PS" = Power Switched
"RA" = Registered Asynchronous
"RS" = Registered Synchronous

The number following this code describes....

1. The size of the memory (bits)
2. The memory organization by specifying the number of outputs
3. Output configuration and pin out/package options

If a higher performance part co-exists i.e., faster speed, then a suffix letter (A) is added to distinguish between the two devices. The normal package letter designator follows last as is custom.

NEW NUMBER	PART DESCRIPTION
Temperature Performance Range	5 = Military 6 = Commercial
Memory Type	3 = PROM (Fuse Programmable) 2 = ROM (Mask Programmable)
Generic Family Designator	S = Schottky LS = Low Power Schottky PS = Power Switched Schottky RA = Registered Asynchronous, Schottky RS = Registered Synchronous, Schottky
Size of Memory	0 = 256 Bit 1 = 1024 Bit 2 = 2048 Bit 4 = 4096 Bit 8 = 8192 Bit 16 = 16384 Bit
Number of Outputs	4 = 4 Outputs 8 = 8 Outputs
Output/Pinout Designator	0 = Open Collector, 1 = Tri-State: 1st pkg. (i.e., 20 pin) 2 = Open Collector, 3 = Tri-State: 2nd pkg. (i.e., 24 pin) etc., etc., etc.
Performance	Absence of letter indicates standard performance; A = enhanced (i.e., speed)
Package	J = Cerdip D = Side brazed N = Plastic F = Flatpack

□□□□□□□□ $\underbrace{□□□□}_{\text{Optional HI-REL Processing*}}$

* 883B MIL-Std-883, Method 5004 & 5005 Level B
883C MIL-Std-883, Method 5004 & 5005 Level C
"B" MIL-Std-883, Method 5004 equivalent
"C" MIL-Std-883, Method 5004 equivalent

High Performance Generic Ti-W PROM Family

53/63SXXX

Features/Benefits

- Reliable Titanium-Tungsten fuses (Ti-W)
- Low voltage programming
- Highest speed Schottky PROM family available
- Pin compatible with standard Schottky PROMs
- PNP inputs for low input current
- Compatible pin configurations for upward expansion

Description

The family features low input current PNP inputs, full Schottky clamping and three-state and open collector outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on chip circuitry and extra fuses provide pre-programming testing which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Applications

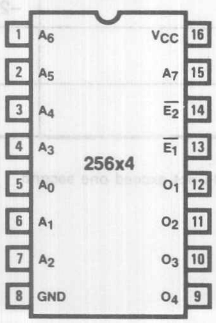
- Microprogram control store
- Microprocessor program store
- Look up table
- Character generator
- Random logic
- Code converter

High Performance Generic PROM Selection Guide

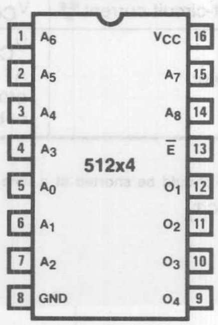
MEMORY			PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION		PINS	TYPE	0°C to +75°C	−55°C to +125°C
1K	256x4	OC	16	J,N	63S140	53S140
		TS			63S141	53S141
2K	512x4	OC	16	J,N	63S240	53S240
		TS			63S241	53S241

Pin Configurations

53/63S140
53/63S141



53/63S240
53/63S241



1165 East Arques Avenue, Sunnyvale, CA 94086 Tel: (408) 739-3535 TWX: 910-339-9229

Monolithic Memories

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature .... –65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA				–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				–0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	µA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 16mA	MIL			0.5	V
				COM			0.45	V
V_{OH}	High-level output voltage *	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = –2mA		2.4			V
			COM I_{OH} = –3.2mA					
I_{OZL}	Off-state output current *	V_{CC} = MAX	V_O = 0.4V				–40	µA
I_{OZH}			V_O = 2.4V				40	µA
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4V				40	µA
			V_O = 5.5V				100	
I_{OS}	Output short-circuit current ***	V_{CC} = 5V	V_O = 0V		–20		–90	mA
I_{CC}	Supply current	V_{CC} = MAX All inputs grounded. All outputs open.	'S140 'S141			80	130	mA
			'S240 'S241			90	130	

*Three-state only

**Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

†Typicals at 5.0V_{CC} and 25°C T_A

Switching Characteristics

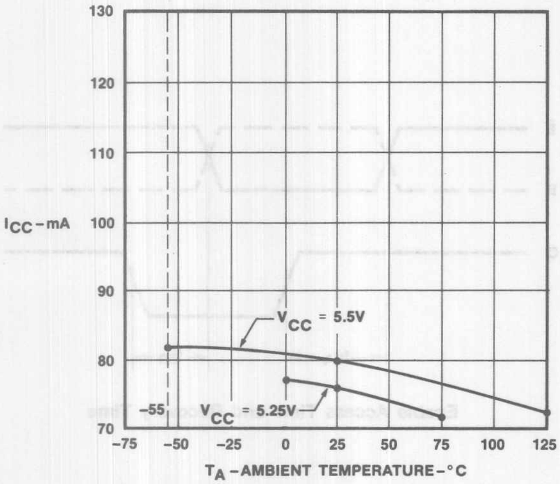
Over Commercial Operating Conditions

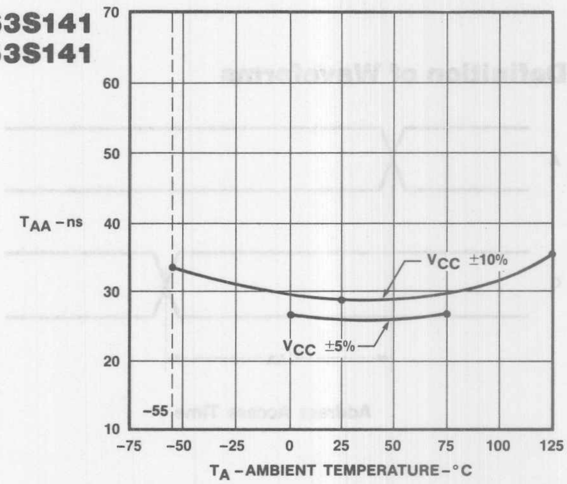
DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME		t_{EA} (ns) ENABLE ACCESS TIME		t_{ER} (ns) ENABLE RECOVERY TIME	
	TYP†	MAX	TYP	MAX	TYP	MAX
63S140/1	29	45	15	25	15	25
63S240/1	27	45	15	25	15	25
53S140/1	29	55	15	30	15	30
53S240/1	27	55	15	30	15	30

† Typicals at 5.0V/V_{CC} and 25°C T_A

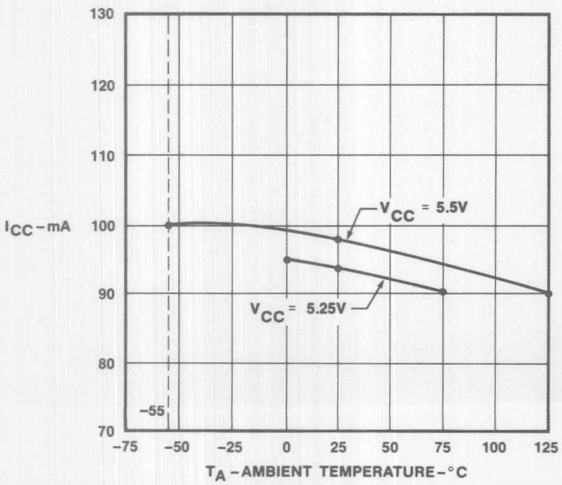
Typical I_{CC} vs Temperature **Typical T_{AA} vs Temperature**

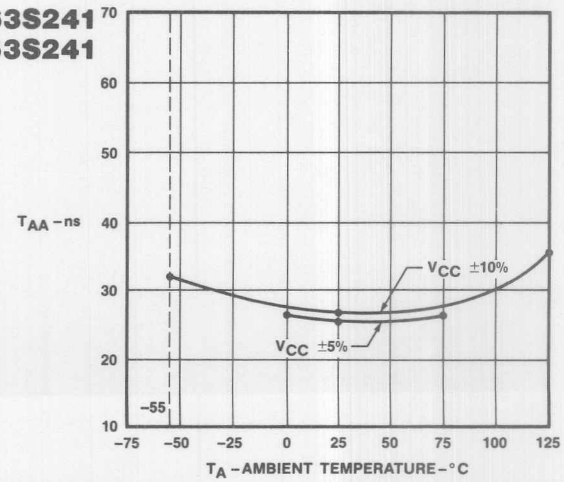
63S141
53S141



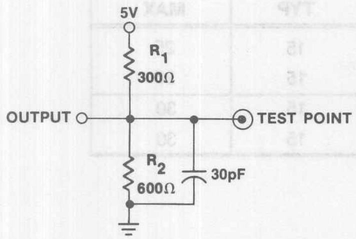


63S241
53S241



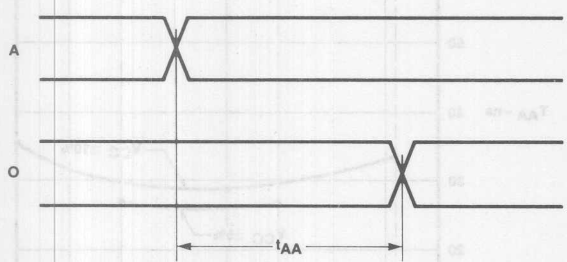


Standard Test Load

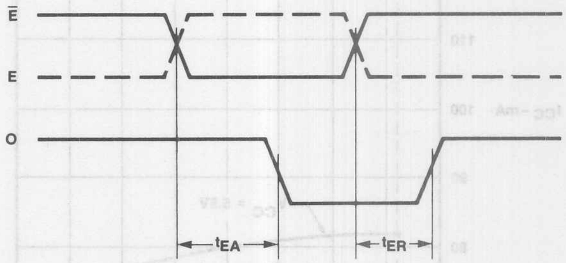


Input Pulse Amplitude 3.0V
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements made at 1.5V

Definition of Waveforms



Address Access Time



Enable Access Time and Recovery Time

Low Power Generic Ti-W PROM Family
53/63LSXXX

Features/Benefits

- Very low power
- Excellent speed-power product
- Reliable Titanium-Tungsten (Ti-W) fuses
- Low voltage programming
- Industry standard pin-out
- PNP inputs for low input current

Applications

- Microprogram control store
- Microprocessor program store
- Look up table
- Character generator
- Random logic
- Code converter

Description

The 'LSXXX family features very low speed power product, low input current PNP inputs, full Schottky clamping and three-state and open collector outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on chip circuitry and extra fuses provide preprogramming testing which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Programming

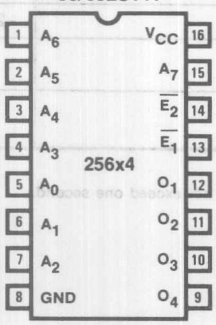
The low power ('LSXXX) generic PROM family has the same programming specifications as the standard TiW ('SXXX) PROMs. This allows the same generic programmer and personality card to be used for both 'LSXXX and 'SXXX PROMs.

Low Power Generic PROM Selection Guide

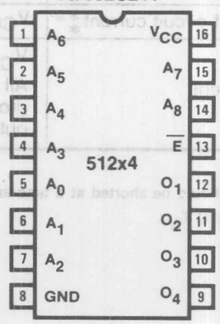
MEMORY			PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION		PINS	TYPE	0°C to +75°C	−55°C to +125°C
1K	256x4	OC	16	J,N	63LS140	53LS140
		TS			63LS141	53LS141
2K	512x4	OC	16	J,N	63LS240	53LS240
		TS			63LS241	53LS241

Pin Configurations

53/63LS140
53/63LS141



53/63LS240
53/63LS241



Absolute Maximum Ratings

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Off-state output voltage	5.5V
Storage temperature	−65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 16mA	MIL			0.5	V
				COM			0.45	V
V_{OH}	High-level output voltage*	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = −2mA		2.4			V
			COM I_{OH} = −3.2mA		2.4			V
I_{OZL}	Off-state output current*	V_{CC} = MAX	V_O = 0.4V				−40	μA
I_{OZH}	Off-state output current*	V_{CC} = MAX	V_O = 2.4V				40	μA
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4V				40	μA
			V_O = 5.5V				100	μA
I_{OS}	Output short-circuit current***	V_{CC} = 5V	V_O = 0V		−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX All inputs grounded. All outputs open.	'LS140, 'LS141			50	70	mA
			'LS240, 'LS241			50	70	mA

* Three-state only.

** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0V V_{CC} and 25°C T_A

Switching Characteristics

Over operating conditions

DEVICE TYPE	t_{AA}(ns) ADDRESS ACCESS TIME		t_{EA}(ns) ENABLE ACCESS TIME		t_{ER}(ns) ENABLE RECOVERY TIME	
	TYP†	MAX	TYP	MAX	TYP	MAX
63LS140/1	38	55	12	30	20	30
63LS240/1	44	60	16	30	15	30
53LS140/1	38	75	12	35	20	35
53LS240/1	44	75	16	35	21	35

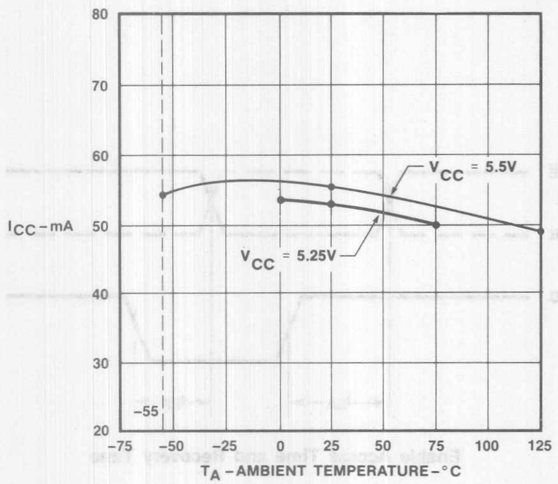
†Typicals at 5.0V V_{CC} and 25°C T_A.

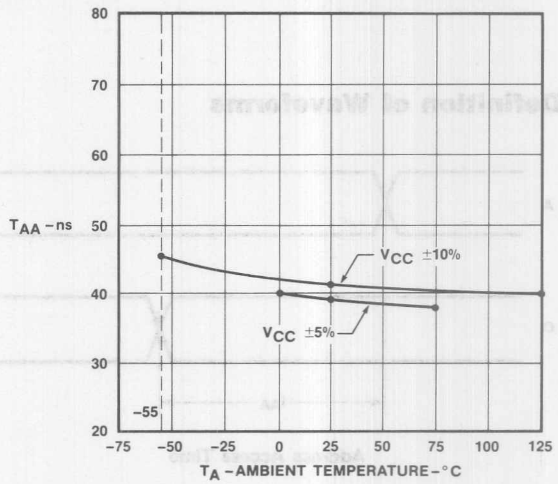
3

Typical I_{CC} vs Temperature

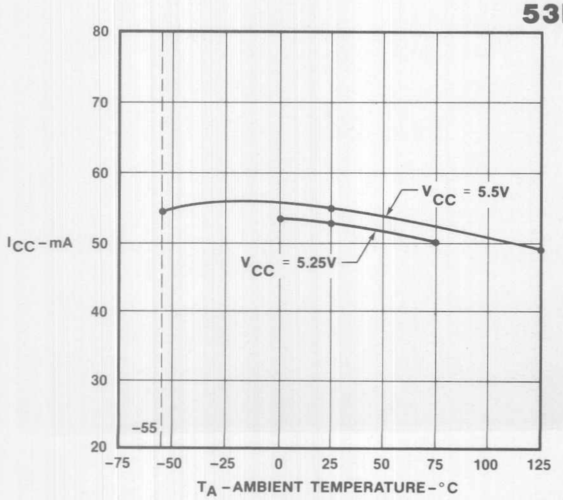
Typical T_{AA} vs Temperature

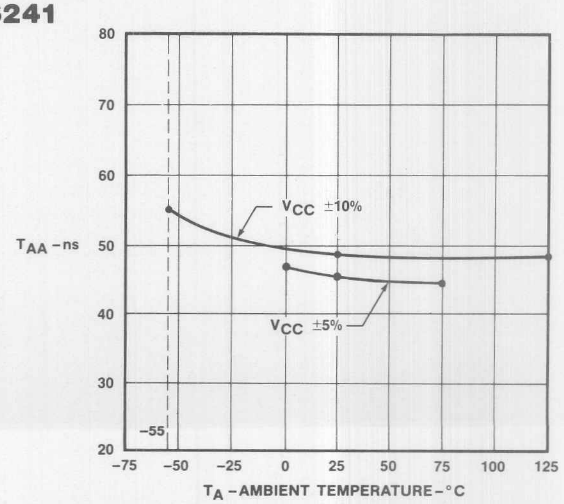
63LS141
53LS141



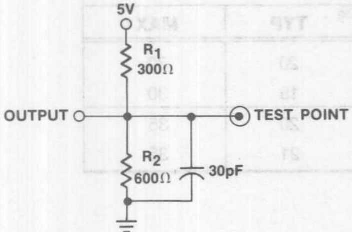


63LS241
53LS241



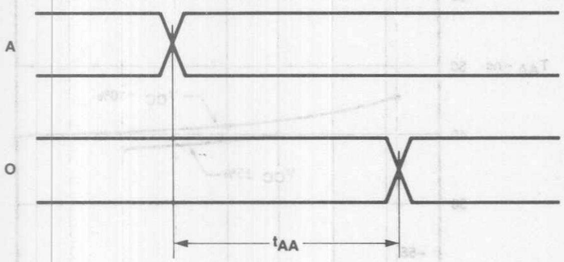


Standard Test Load

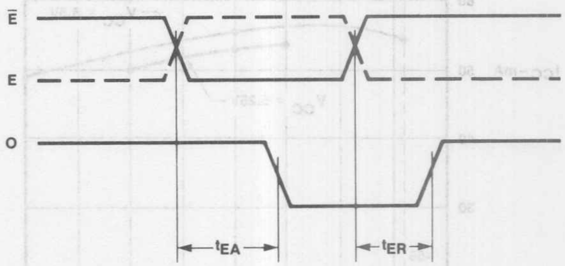


Input pulse amplitude 3.0V
Input rise and fall times 5ns from 1.0V to 2.0V
Measurements made at 1.5V

Definition of Waveforms



Address Access Time



Enable Access Time and Recovery Time

High Performance Registered 1024x4 PROM
53/63RA441

Features/Benefits

- Edge triggered "D" registers
- Advanced Schottky processing
- 4-bit-wide in 18 pin for high board density
- Lower system package counts
- Lower system power
- Faster cycle times
- 16mA I_{OL} output drive capability

Applications

- Pipelined microprogramming
- State sequencers
- Next address generation
- Mapping PROM

Description

A family of registered PROMs offers new savings for designers of pipelined microprogrammable systems. The wide instruction register which holds the microinstruction during execution, is now incorporated into the PROM chip.

Ordering Information

MEMORY		PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION	PINS	TYPE	MIL	COM
4K	1024x4	18	J, N	53RA441	63RA441

3

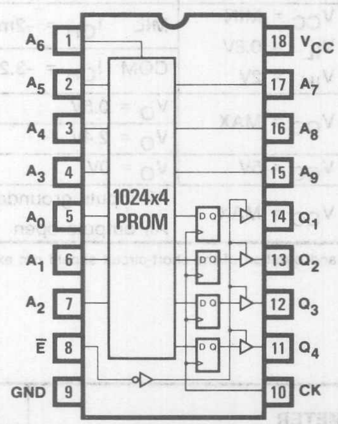
Edge Triggered Register

The PROM output is loaded into a 4-bit register on the rising edge of the clock. The use of the term "register" is to be distinguished from the term "latch," in that a register contains master slave flip-flops and the latch contains gated flip-flops. The advantages of using a register are that system timing is simplified, and faster micro cycle times can be obtained.

The output of the register is buffered by three-state drivers which are compatible with the new low-power Schottky three-state bus standard.

Pin Configuration

53/63RA441



Supply voltage, V_{CC} 7V
Input voltage 7V
Off-state output voltage 5.5V
Storage temperature .... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
t_{su}	Address set-up time	60	30		50	30		
t_h	Address hold time	0	-10		0	-10		
t_w	Clock pulse width	25	8		20	8		
T_A	Operating free-air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18mA				-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	$V_I = V_{CC}$				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 16mA				0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = -2mA COM I_{OH} = -3.2mA		2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.5V				-40	μA
I_{OZH}			V_O = 2.4V				40	μA
I_{OS}	Output short-circuit current*	V_{CC} = 5V	V_O = 0V		-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX	All inputs grounded All outputs open	MIL		120	175	mA
				COM		120	165	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

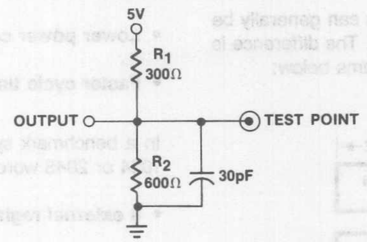
†Typicals at 5.0V V_{CC} and 25°C T_A

Switching Characteristics

Over Operating Conditions

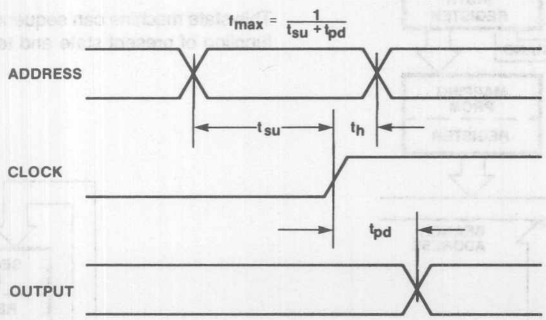
SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	Clock to output access time		20	35		20	30	
t_{ER}/t_{EA}	Enable to output access and recovery time		19	35		19	30	

Standard Test Load



Input Pulse Amplitude 3.0V
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements made at 1.5V

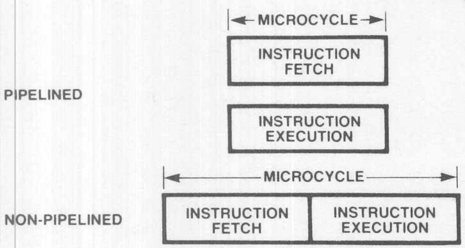
Definition of Waveforms



Registered PROMs Impact Computer Architecture by John Birkner

Pipelined Microprogrammable Systems

Microprogrammed processors and controllers can generally be classified as either pipelined or non-pipelined. The difference is demonstrated by the microcycle timing diagrams below:



Clearly, the benefit of pipelining is that the microcycle time is defined by the **longer of either** fetch or execution times, rather than the **sum of both** fetch and execution times. This gain can be as much as 2:1, if fetch and execution times are equal. The gain in cycle time is, of course, lost when a branch requires the look ahead fetch to be discarded. The ratio of sequential fetches to branches varies according to application. In heavily decision-oriented applications, the ratio may be as low as 3:1. Typically, the ratio is 5:1. An example of a pipelined microprogrammed processor is shown in Figure 1.

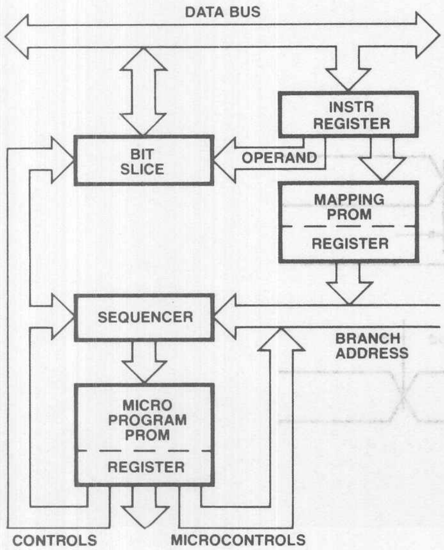


Figure 1. Pipelined Microprogrammed Processor

Benefits

Advantages of registered PROMs in pipelined microprogrammable systems are:

- **Lower package counts**
- **Lower power consumption**
- **Faster cycle times**

In a benchmark system requiring a control store of 64 bits by 1024 or 2048 words, these benefits are equated to:

- **8 external register package savings**
- **Over 1 amp max I_{CC} reduction (compared to Schottky registers)**
- **280mA max I_{CC} reduction (compared to low power Schottky registers)**
- **20nsec faster cycle time (compared to low power Schottky registers)**

Structured Logic

The registered PROM is a structured logic primitive which, along with other primitives, can be used as building blocks to define a variety of processor and controller architectures.

The most basic architecture is formed by feeding the outputs of a registered PROM back to the address inputs.

This state machine can sequence from one step to the next as a function of present state and test inputs.

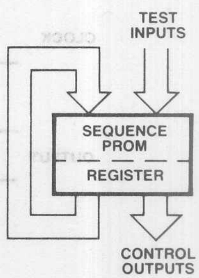


Figure 2. State Sequencer

A powerful microprogram sequencer can be constructed from registered PROMs, as shown in Figure 3. The Next Address PROM provides the normal sequence while the Branch Address PROM provides instant availability of an alternate sequence when the branch condition is satisfied. The Return Jump RAM provides a microsubroutine capability.

An 8-bit microprogrammed computer can be constructed, Figure 4, using as little as 30 ICs. A 100nsec microcycle is easily achievable. Instruction decode is accomplished by direct vector from 8-bit macro instruction into microspace. Dynamic RAM control signals RAS, CAS and WRITE are under direct microprogram control.

The 8-bit computer, Figure 4, is a particularly good example of how the registered PROM takes its place among RAMs, registers and buffers as a basic building block in high performance microprogrammable systems.

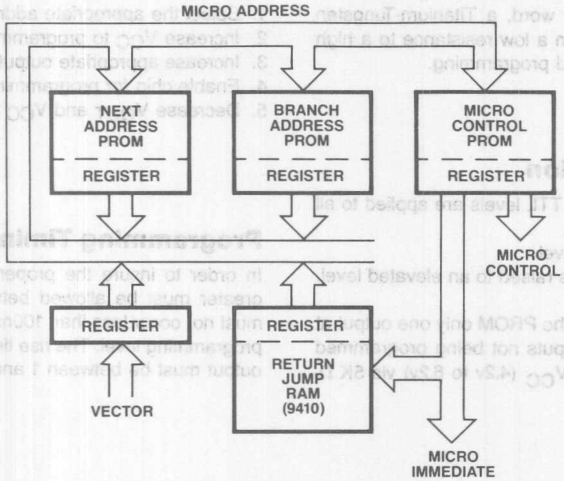


Figure 3. Microprogram Sequencer

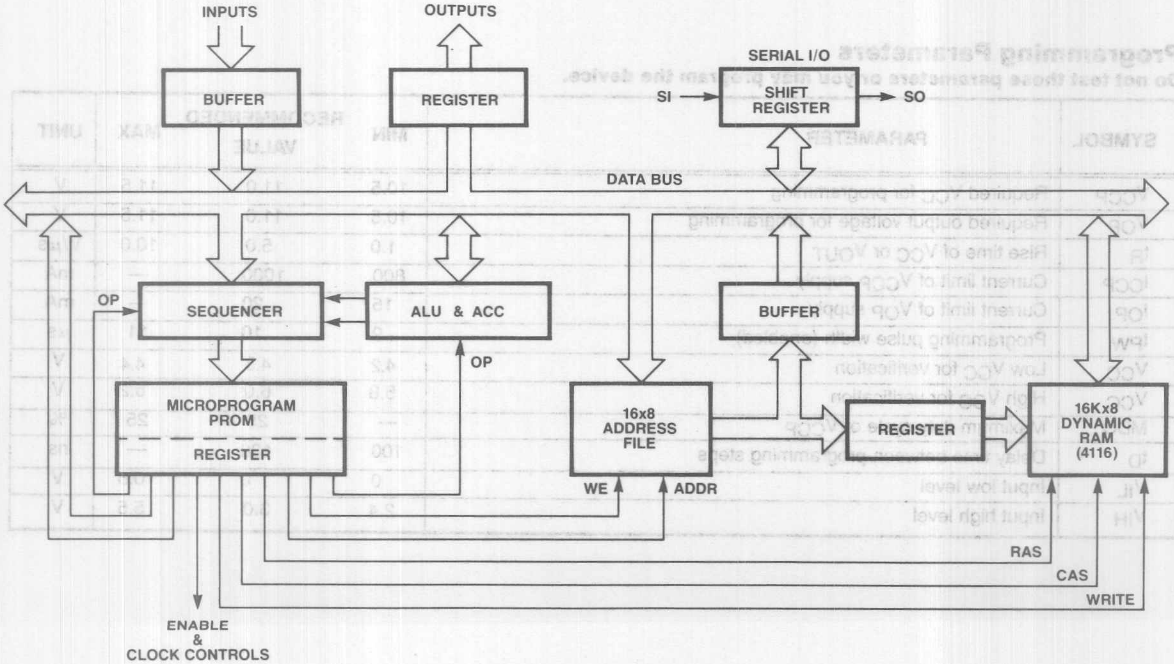


Figure 4. 8-Bit Computer

Ti-W PROM Programming Instructions

Device Description

All of the High Performance Generic Ti-W PROM Families are manufactured with all outputs low in all storage locations. To produce a high at a particular word, a Titanium-Tungsten Fusible-Link must be changed from a low resistance to a high resistance. This procedure is called programming.

Programming Description

To program a particular bit normal TTL levels are applied to all inputs. Programming occurs when:

1. V_{CC} is raised to an elevated level.
2. The output to be programmed is raised to an elevated level.
3. The device is enabled.

In order to avoid misprogramming the PROM only one output at at time is to be programmed. Outputs not being programmed should be left open or connected to V_{CC} (4.2v to 6.2v) via 5K Ω resistors.

Programming Sequence

The sequence of programming conditions is critical and must occur in the following order:

1. Select the appropriate address with chip disabled
2. Increase V_{CC} to programming voltage
3. Increase appropriate output voltage to programming voltage
4. Enable chip for programming pulse width
5. Decrease V_{OUT} and V_{CC} to normal levels

Programming Timing

In order to insure the proper sequence, a delay of 100ns or greater must be allowed between steps. The enabling pulse must not occur less than 100ns after the output voltage reaches programming level. The rise time of the voltage on V_{CC} and the output must be between 1 and 10 V/μs.

Programming Parameters

Do not test these parameters or you may program the device.

SYMBOL	PARAMETER	MIN	RECOMMENDED VALUE	MAX	UNIT
V_{CCP}	Required V_{CC} for programming	10.5	11.0	11.5	V
V_{OP}	Required output voltage for programming	10.5	11.0	11.5	V
t_R	Rise time of V_{CC} or V_{OUT}	1.0	5.0	10.0	V/μs
I_{CCP}	Current limit of V_{CCP} supply	800	1000	—	mA
I_{OP}	Current limit of V_{OP} supply	15	20	—	mA
t_{PW}	Programming pulse width (enabled)	9	10	11	μs
V_{CC}	Low V_{CC} for verification	4.2	4.3	4.4	V
V_{CC}	High V_{CC} for verification	5.8	6.0	6.2	V
MDC	Maximum duty cycle of V_{CCP}	—	25	25	%
t_D	Delay time between programming steps	100	120	—	ns
V_{IL}	Input low level	0	0	0.5	V
V_{IH}	Input high level	2.4	3.0	5.5	V

Verification

After each programming pulse verification of the programmed bit should be made with both low and high V_{CC}. The loading of the output is not critical and any loading within the DC specifications of the part is satisfactory.

Additional Pulses

Up to 10 programming pulses should be applied until verification indicates that the bit has programmed. After verification an additional 5 programming pulses must be applied to insure the reliability of the programmed bit.

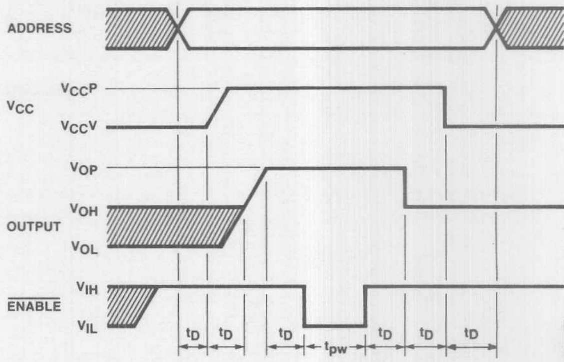
Board Level Programming

Board level programming is easily accomplished since only an enabled PROM is programmed. At the board level only the desired PROM and output should be enabled.

Programming Registered PROMs

The registered PROM is programmed in the same manner as standard PROMs.

Programming Waveforms



t_D = 100ns min
t_{pw} = 9μs min 11μs max

NOTE: Programming pulse t_{pw} is applied for 5 additional pulses after verification indicates a bit is blown.

Figure 1.

Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 95%. If your programming yield is lower, check your programmer. It may not be properly calibrated. (See figure 1)

Programming is final manufacturing—it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember—The best PROMs available can be made unreliable by improper programming techniques.

PART NUMBER		SIZE	CONFIGURATION	OUTPUT	NO. OF PINS	SOCKET ADAPTER	
MILITARY	COMMERCIAL					DATA I/O (ALL SERIES)*	PRO-LOG (SERIES 90, 92)†
53S140 53S141	63S140 63S141	1K	256x4	OC TS	16	715-1035-1	PA16-1
53LS140 53LS141	63LS140 63LS141	1K	256x4	OC TS	16	715-1035-1	PA16-1
53S240 53S241	63S240 63S241	2K	512x4	OC TS	16	715-1035-2	PA16-1
53LS240 53LS241	63LS240 63LS241	2K	512x4	OC TS	16	715-1035-2	PA16-1
53RA441	63RA441	4K	1024x4	TS	18	715-1435	PA18-5

* Program card set is 909-1515-1 for all series DATA/I/O

† Personality module is PM9066 for all PRO-LOG (series 90, 92)

Generic ROM Family

52/62XX-1 52/62XX-2

Features/Benefits

- High bit density up to 16K
- PNP inputs for low input current
- High speed Schottky technology
- Open collector or three state outputs

Applications

- Character generator
- Look up table
- Microprocessor program store
- Microprogram store
- Random logic
- Code converter

Description

The 52/6200 series generic ROM family is available in sizes from 8K through 16K bits. The 8-bit-wide ROMs are available as 1Kx8 and 2Kx8 organization. Additional 9-bit and 10-bit-wide output configurations are available for custom logic or character generator applications.

Generic ROM Selection Guide

MEMORY			PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION				COMMERCIAL	MILITARY
8192	1024x8	OC	J24	F24	6280-1	5280-1
		TS		F24	6281-1	5281-1
		OC		F4-24	6280-2	5280-2
		TS		F4-24	6281-2	5281-2
		OC		F24	6282-1	5282-1
		TS		F24	6283-1	5283-1
9216	1024x9	OC	J24		6260-1	5260-1
		TS			6261-1	5261-1
10240	1024x10	OC	J24		6255-1	5255-1
		TS			6256-1	5256-1
10368	1152x9	OC	J24		6290*	5290*
		TS			6291*	5291*
16384	2048x8	OC	J24		6275-1	5275-1
		TS			6276-1	5276-1

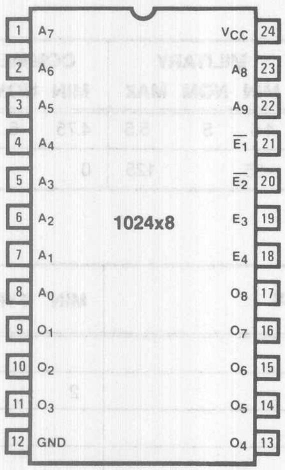
*Detailed information in section 5 (character generators)

1165 East Arques Avenue, Sunnyvale, CA 94086 Tel: (408) 739-3535 TWX: 910-339-9229

Monolithic Memories

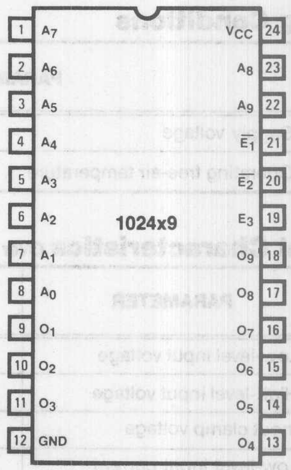
Pin Configurations

52/6280-1 52/6280-2 *52/6282-1
52/6281-1 52/6281-2 *52/6283-1

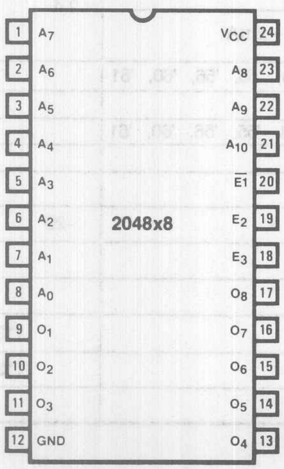


*"OR" ENABLE = $\overline{E1}\ \overline{E2}$ + E3 E4

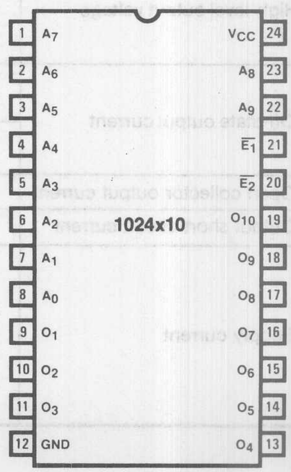
52/6260-1
52/6261-1



52/6275-1
52/6276-1



52/6255-1
52/6256-1



4

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45V				−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V				40	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1.0	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OL} = 8mA; COM I_{OL} = 10mA	'75, '76, '80, '81, '82, '83			0.5	V
			MIL COM I_{OL} = 6mA	'55, '56, '60, '61				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OH} = −1mA		2.4			V
			COM I_{OH} = −2mA					
I_{OZL}	Off-state output current	V_{CC} = MAX, V_O = 0.5V	'80, '81, '82, '83, '55, '56, '60, '61				−50	μA
			'75, '76				−100	
I_{OZH}		V_{CC} = MAX, V_O = 2.4V	'80, '81, '82, '83, '55, '56, '60, '61				50	μA
			'75, '76				100	
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4V				100	μA
I_{OS}	Output short-circuit current	V_{CC} = 5.0V	V_O = 0V		−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX, All inputs grounded All outputs open	'55, '60				165	mA
			'56, '61				175	
			'82 '83			113	155	
			'80, '81			113	155	
			'75, '76				190	

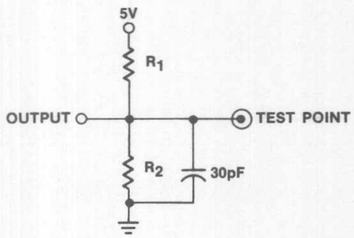
Switching Characteristics

Over Operating Conditions

DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME	t_{EA} (ns) ENABLE ACCESS TIME	t_{ER} (ns) ENABLE RECOVERY TIME	CONDITIONS (See standard test load)	
	MAX	MAX	MAX	R1Ω	R2Ω
6255-1, 6256-1	100	70	40	750	1500
5255-1, 5256-1	150	80	45		
6260-1, 6261-1	100	70	40		
5260-1, 5261-1	150	80	45		
6275-1, 6276-1	110	40	40	560	1110
5275-1, 5276-1	120	50	50		
6280-1, 6281-1	80	70	45		
5280-1, 5281-1	140	90	50		
6282-1, 6283-1	80	70	45		
5282-1, 5283-1	140	90	50		

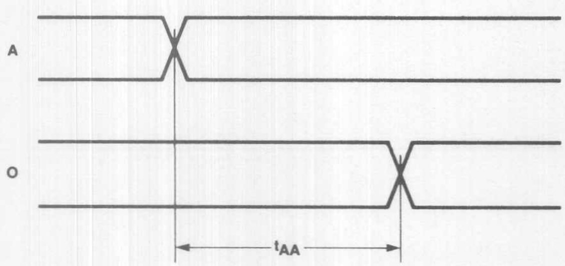
4

Standard Test Load

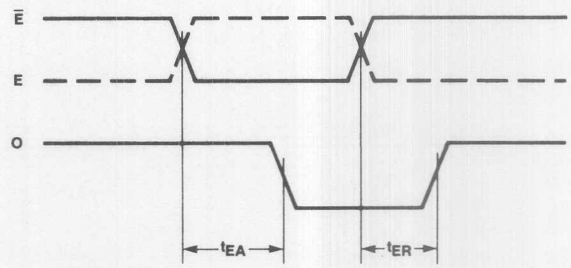


Input Pulse Amplitude
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements made at 1.5V

Definition of Waveforms



Address Access Time



Enable Access Time and Recovery Time

High Speed Character Generators

Features/Benefits

- 100 ns max. access time
- Low power dissipation—500 mW
- Standard packaging—18 pin dip/24 pin dip
- Single 5 volt supply
- 64/128 characters in one package
- Open collector or three-state

Applications

- CRT displays
- Printing calculators
- LED arrays
- Typesetting

Description

The intended application for these devices is the generation of 64 or 128 ASCII alpha-numeric characters utilizing a read out system which generates the characters either horizontally or vertically, one word line at a time.

5

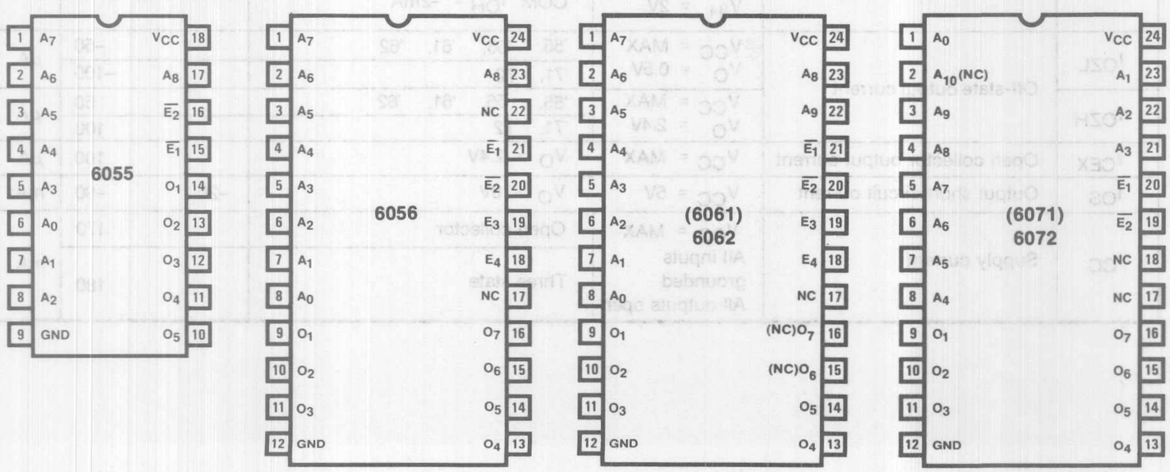
Character Generator Selection Guide

GENERIC PART NO.	CHARACTERS NO.	CHARACTERS TYPE	MATRIX	SCAN	COMMERCIAL OC	COMMERCIAL TS	MILITARY OC	MILITARY TS	PKG
6055	64	ASCII	5 x 7	Row	6055	6155	5055	5155	J18
6056 †			5 x 7	Column	6056	6156	*	*	J24
6071			7 x 9	Row	6071	6171	*	*	J24
6061 †	128	ASCII	5 x 7	Row	6061	6161	*	*	J24
6062 †			5 x 7	Column	6062	6162	*	*	
6072			7 x 9	Row	6072	6172	*	*	
6290	128	Custom	7 x 9	Row	6290	6291	5290	5291	J24
6292			9 x 9	Row/Column	6292	6293	5292	5293	

* For military versions of these Character Generators contact the factory.

† "OR" enable = $\overline{E1}\,\overline{E2}$ + E3 E4

Pin Configurations



Off-state output voltage 5.5V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

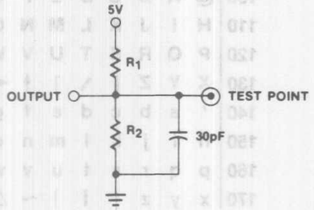
SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45V				−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V				40	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OL} = 8mA COM I_{OL} = 10mA	'55, '56, '61, '62			0.5	V
			I_{OL} = 6mA	'71, '72				
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = −1mA COM I_{OH} = −2mA		2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX V_O = 0.5V	'55, '56, '61, '62				−50	μA
			'71, '72				−100	
I_{OZH}		V_{CC} = MAX V_O = 2.4V	'55, '56, '61, '62				50	μA
			'71, '72				100	
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4V				100	μA
I_{OS}	Output short-circuit current	V_{CC} = 5V	V_O = 0V		−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX All inputs grounded All outputs open	Open collector				170	mA
			Three state				180	

Switching Characteristics

Over Operating Conditions

DEVICE TYPE	tAA(ns) ADDRESS ACCESS TIME	tEA(ns) ENABLE ACCESS TIME	tER(ns) ENABLE RECOVERY TIME	CONDITIONS (See standard test load)	
	MAX	MAX	MAX	R1Ω	R2Ω
6X55, 6X56, 6X61, 6X62	100	70	45	560	1100
5055, 5155	175	90	50		
6X71, 6X72	125	75	40	750	1500

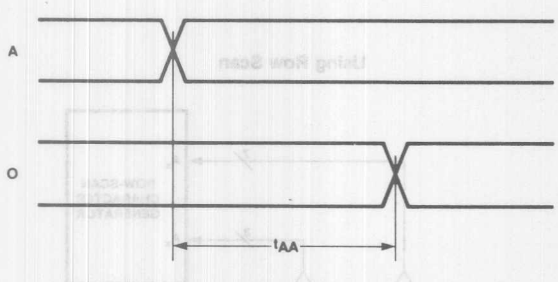
Standard Test Load



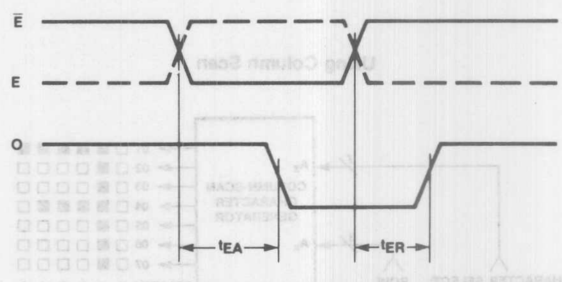
Input Pulse Amplitude 3.0V
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements Made at 1.5V

5

Definition of Waveforms



Address Access Time



Enable Access Time and Recovery Time

Tabulation by Octal Select-Code

64 ASCII Characters

Row Scan 6055, 6071

Column Scan 6056

	0	1	2	3	4	5	6	7
0	@	A	B	C	D	E	F	G
10	H	I	J	K	L	M	N	O
20	P	Q	R	S	T	U	V	W
30	X	Y	Z	[	\	]	↑	←
40		!	"	#	$	%	&	'
50	(	)	*	+	,	—	.	/
60	0	1	2	3	4	5	6	7
70	8	9	:	;	<	=	>	?

Example:

The Character $ is addressed by the octal code 44

128 ASCII Characters

Row Scan 6061, 6072

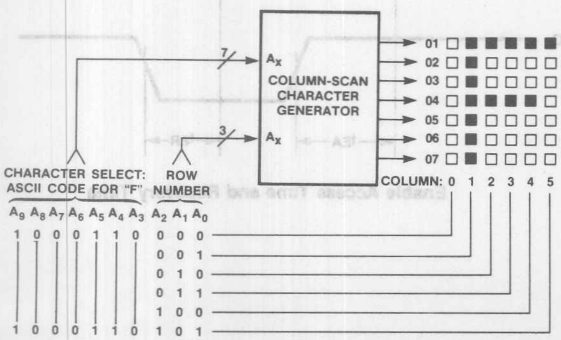
Column Scan 6062

	0	1	2	3	4	5	6	7
0	△	△	△	△	△	△	△	△
10	△	△	△	△	△	△	△	△
20	△	△	△	△	△	△	△	△
30	△	△	△	△	△	△	△	△
40		!	"	#	$	%	&	'
50	(	)	*	+	,	—	.	/
60	0	1	2	3	4	5	6	7
70	8	9	:	;	<	=	>	?
100	@	A	B	C	D	E	F	G
110	H	I	J	K	L	M	N	O
120	P	Q	R	S	T	U	V	W
130	X	Y	Z	[	\	]	↑	←
140	'	a	b	c	d	e	f	g
150	h	i	j	k	l	m	n	o
160	p	q	r	s	t	u	v	w
170	x	y	z	{	|	}	~	△

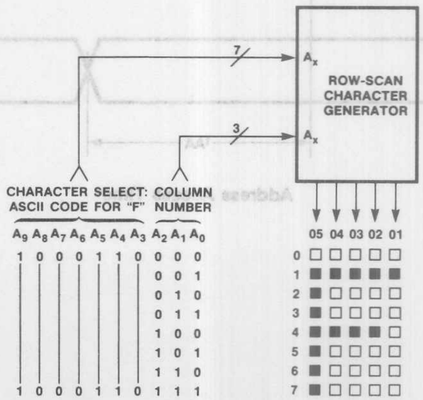
△ This ASCII code represents a control character.
For the corresponding display character see the detailed data sheet.

Generation of the Letter "F"

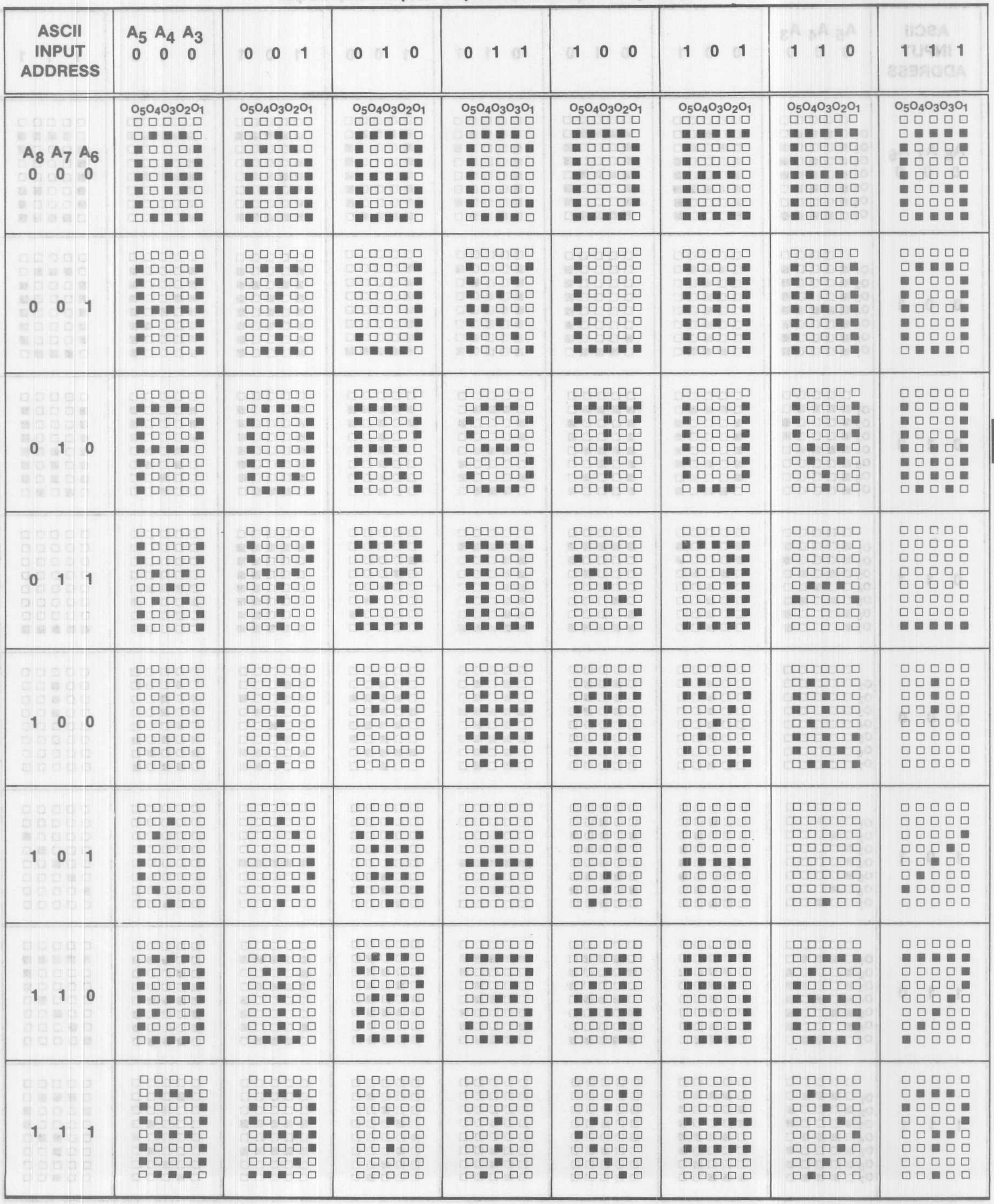
Using Column Scan



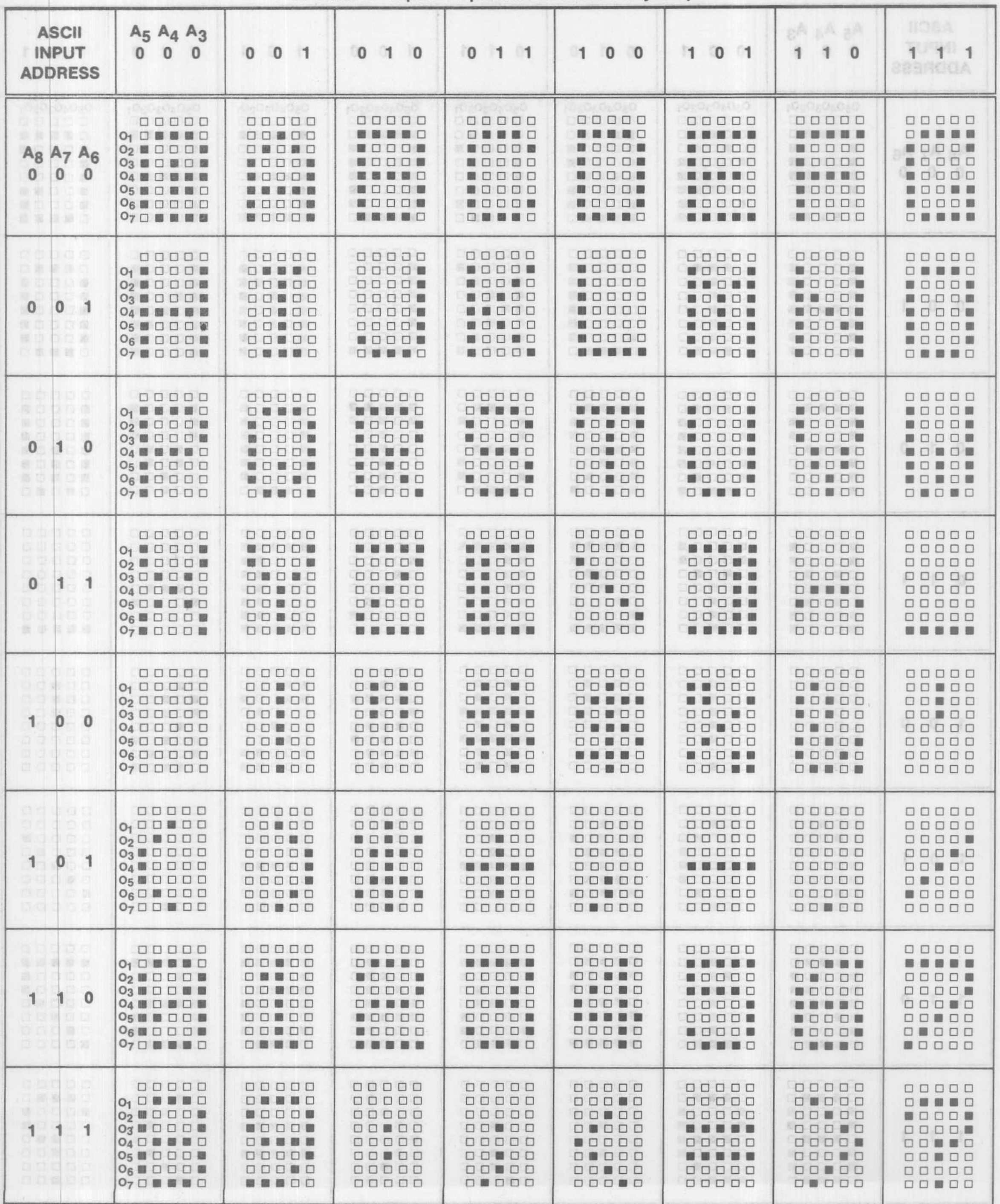
Using Row Scan



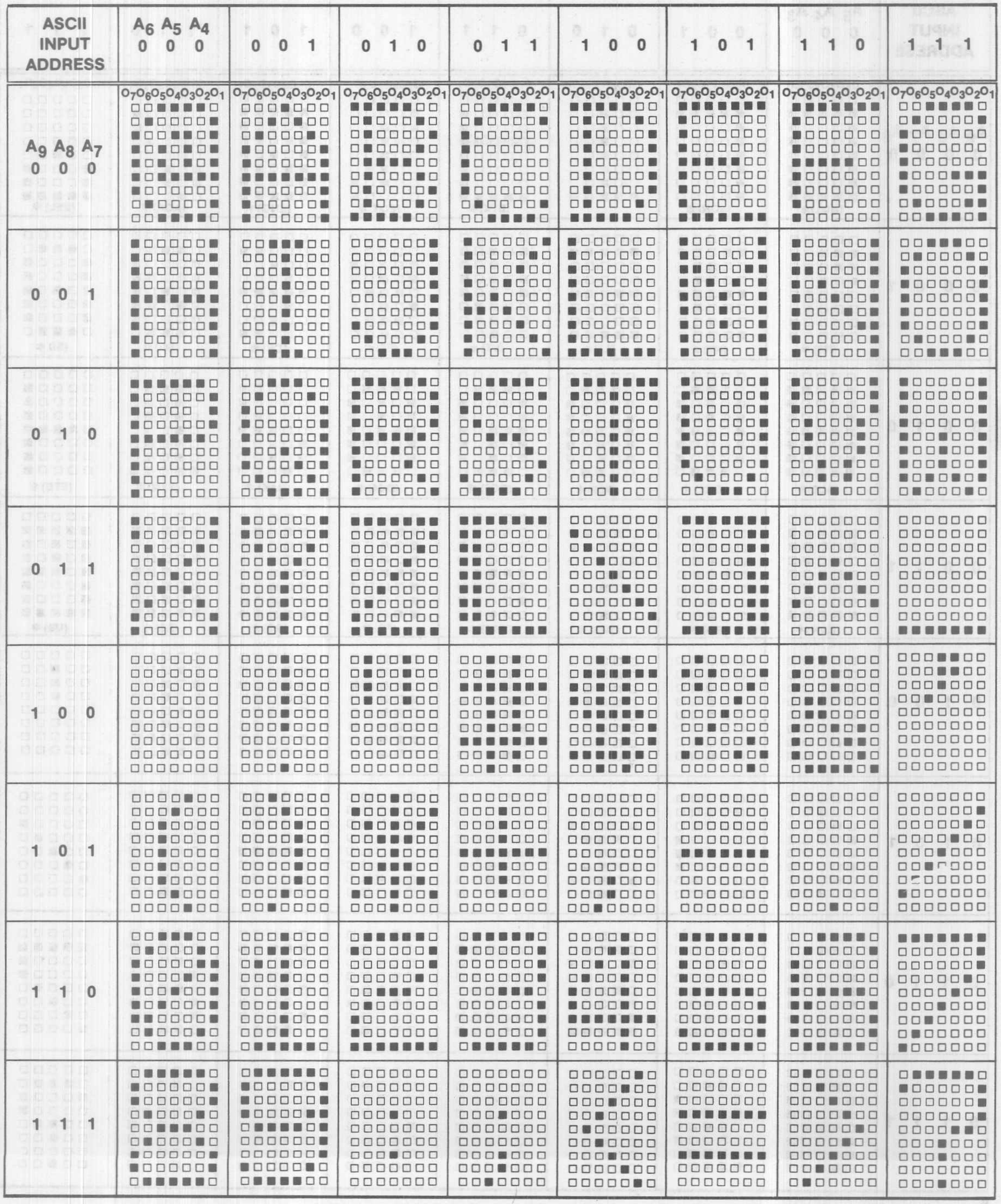
A "Filled In" Square Represents a Low Memory Output



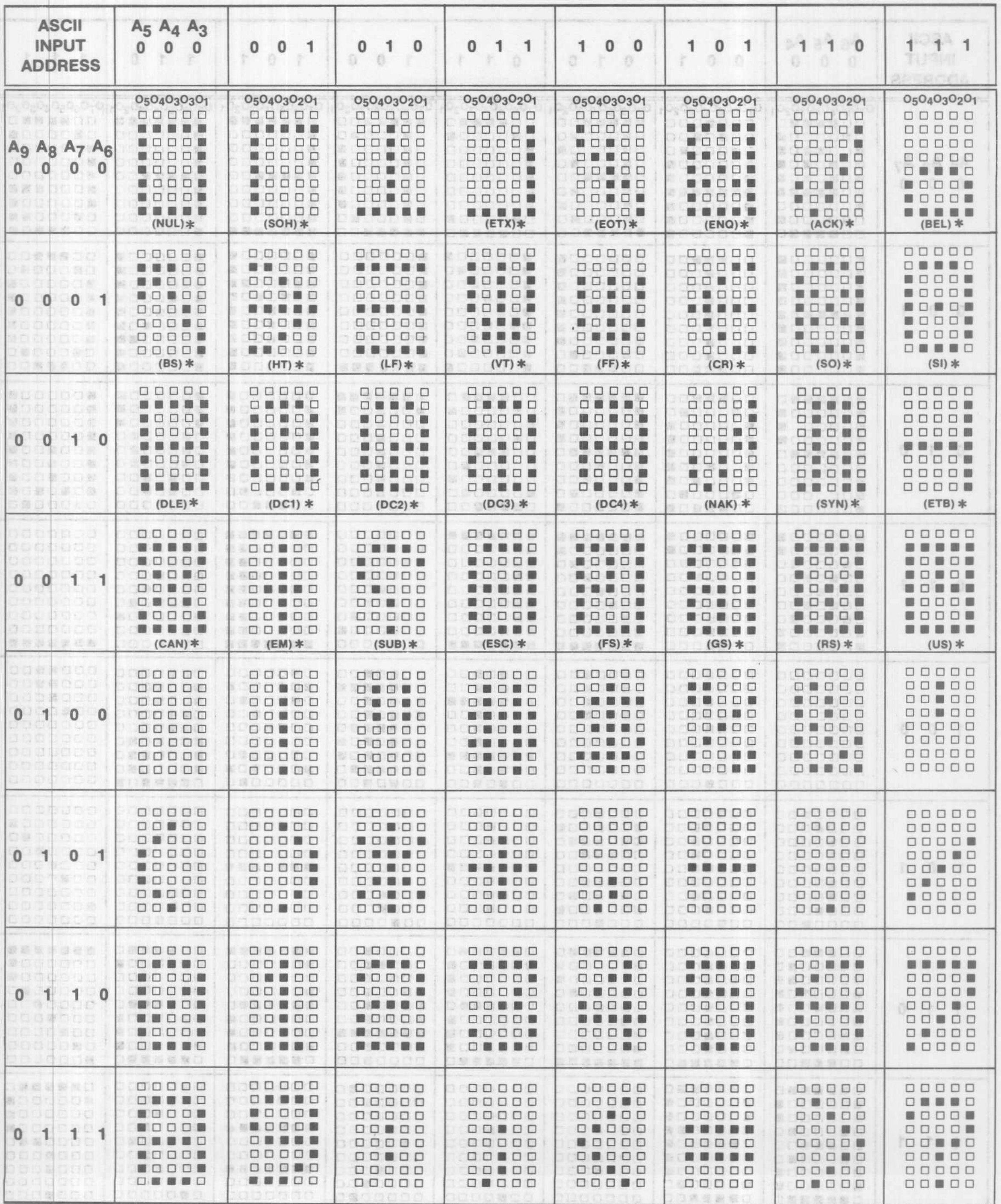
A "Filled In" Square Represents a Low Memory Output



A "Filled In" Square Represents a Low Memory Output

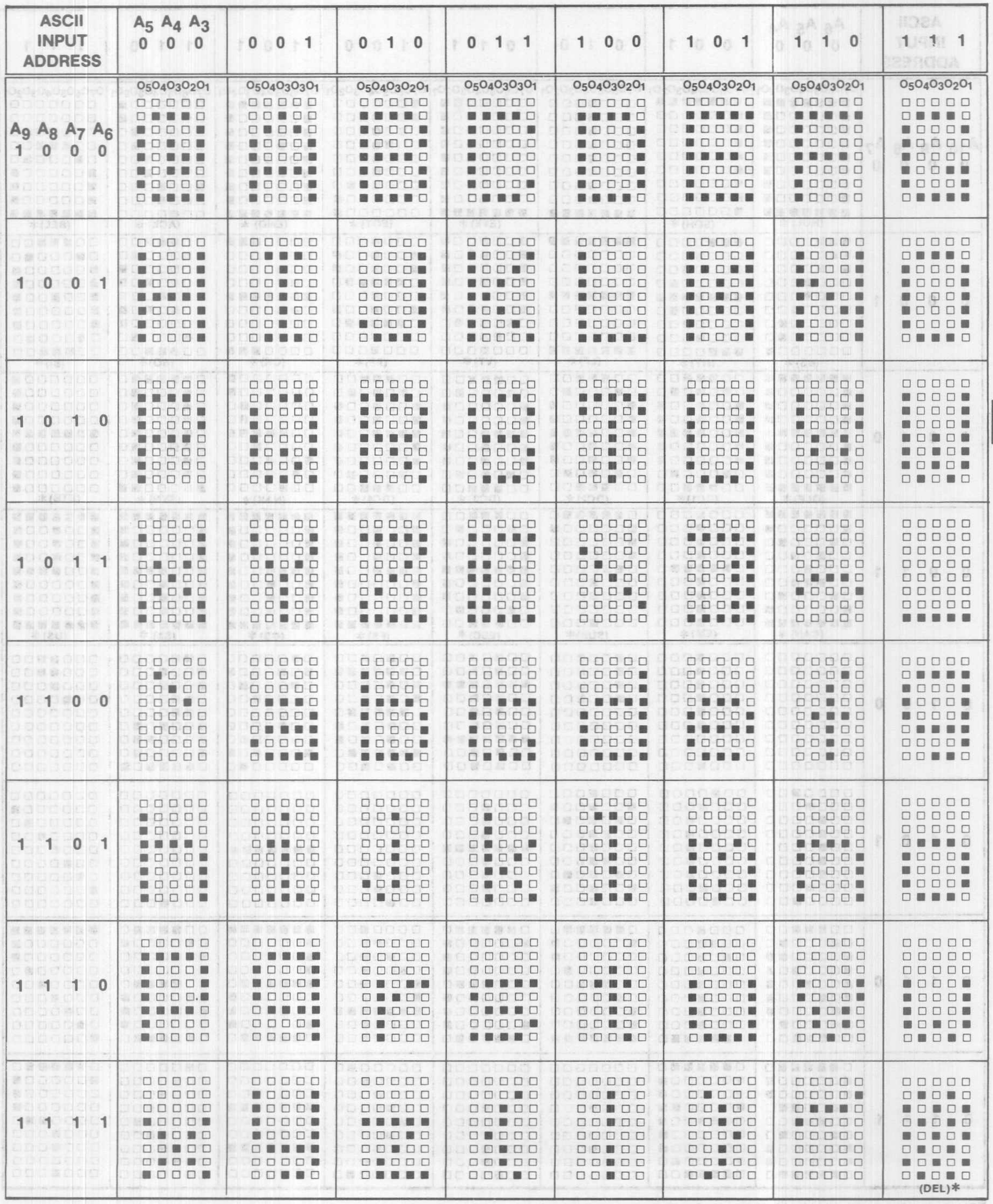


A "Filled In" Square Represents a Low Memory Output



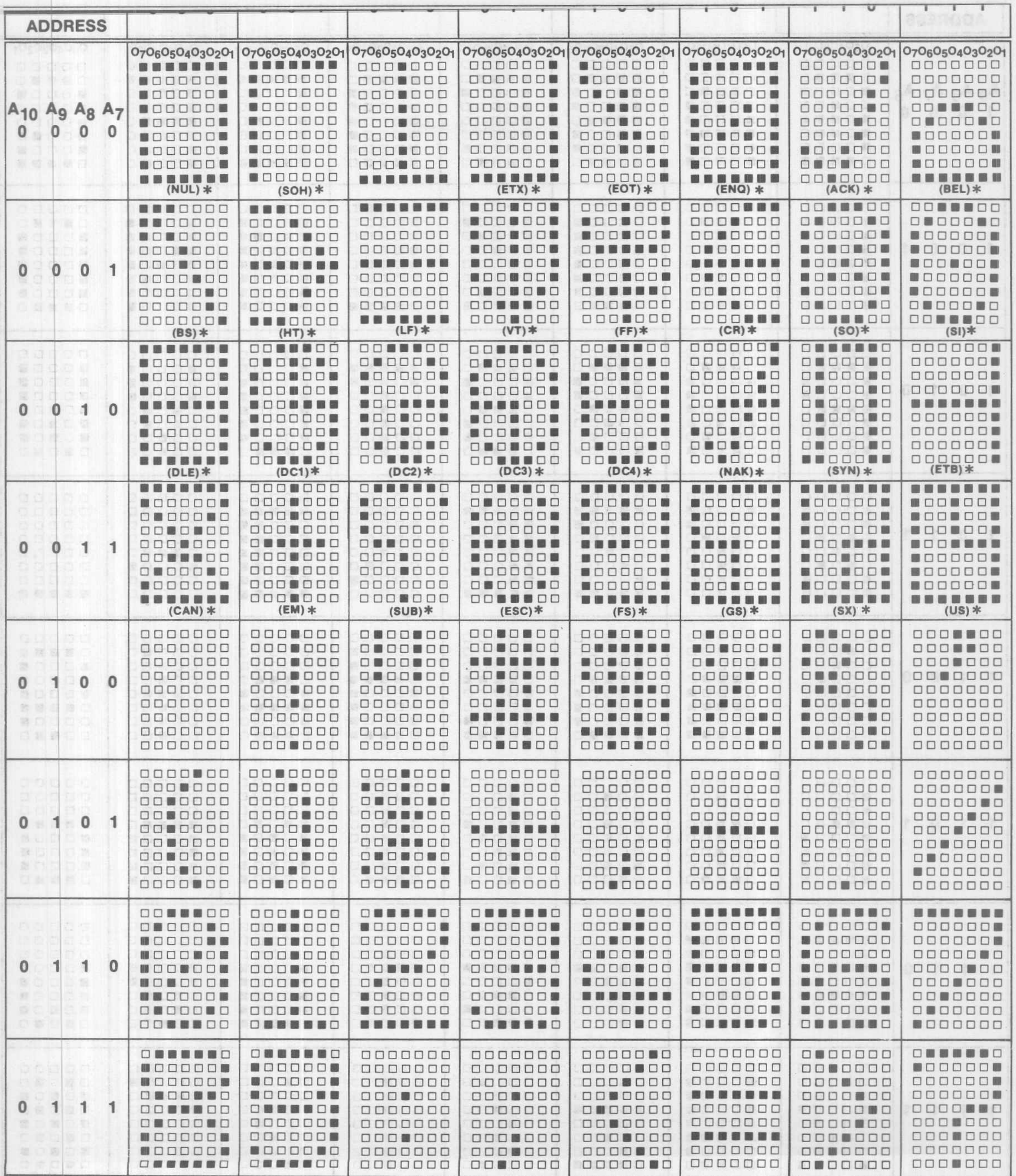
* The letters in parenthesis identify the control code corresponding to the appropriate pictorial represention. These representations were obtained from the USASI X 3.2 Code Practice Manual.

A "Filled In" Square Represents a Low Memory Output



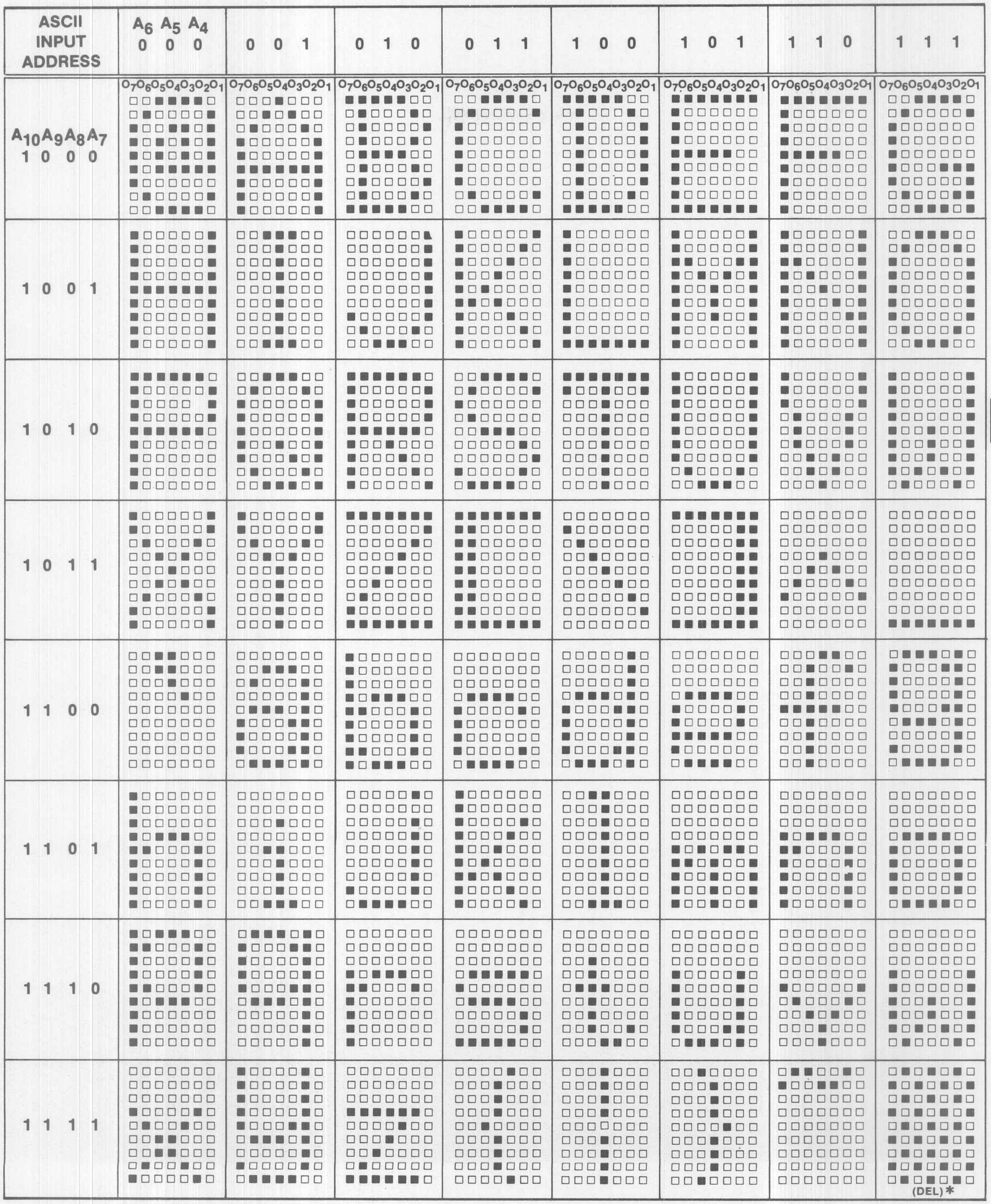
5

7 x 9 Character Font 6072 6172



*The letters in parenthesis identify the control code corresponding to the appropriate pictorial represention. These representations were obtained from the USASI X 3.2 Code Practice Manual.

A "Filled In" Square Represents a Low Memory Output



5

High Speed
Custom Character Generators
52/6290 52/6291 52/6292 52/6293

Features/Benefits

- Schottky—high speed 10MHz
- Specifically designed for custom 7 x 9 row scan and 9 x 9 font character generators
- Up to 128 characters in one package
- Low power dissipation—500mW
- Standard packaging—24 pin dip
- Single 5 volt supply
- 125 ns max. access time

Applications

- A single package high speed bipolar replacement for slow multiple package MOS character generators
- CRT displays
- Printing calculators
- LED arrays
- Typesetting
- Navigation systems

Description

A 7 x 9 font row scan character has 7 outputs and 9 rows per character. The character is formed one row at a time. 9 words of a ROM with 7 outputs per word are required for each character. 128 characters required on 1152 x 7 ROM which is the size of the 5290/1, 6290/1. For custom column scan 7 x 9 characters consult the standard bipolar 7 x 9 character generator data sheet.

A 9 x 9 font character has 9 outputs and 9 rows of columns per character depending upon whether we are forming a row or column scan. 9 words of a ROM with 9 outputs per row are required for each character. 128 characters require an 1152 x 9 ROM which is the 5292/3, 6292/3.

A_3, A_2, A_1, and A_0 pins are used to scan through the 9 ROM words per character. This is usually implemented by "short counting" a 4-bit binary counter so that it counts from 0000 to 1000 (9 counts) continuously (See applications section). A_4 thru A_{10} are used to pick one of the 128 characters. A_4 is the least significant binary digit and A_{10} is the most significant binary digit.

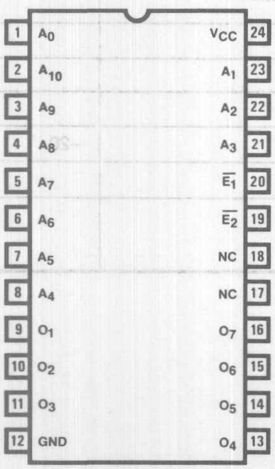
The enable E_1, and E_2 must both be low to activate the part. A disabled part (E_1 or E_2 high) has high memory outputs permitting wire ORing or blanking.

Custom Font

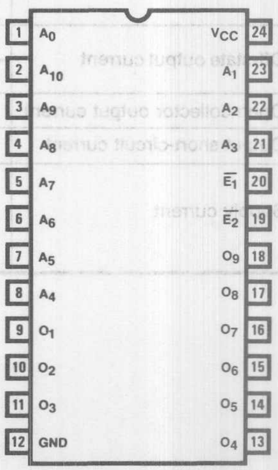
It's easy to go from custom font to the punched card or tape format preferred by Monolithic Memories Inc. Several examples are shown. We have arbitrarily assumed that a character is formed by a series of low memory outputs in a background of high memory outputs. The assumption, of course can be reversed.

Pin Configuration

5290/1, 6290/1 (7 x 9 Row Scan)



5292/3, 6292/3 (9 x 9 Row or Column Scan)



Note 1): A_0, A_1, A_2, A_3 are used for the character scan.
2): Both enables must be low to advance the device.

1165 East Arques Avenue, Sunnyvale, CA 94086 Tel: (408) 739-3535 TWX: 910-339-9229

Monolithic Memories

5

Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature .... –65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

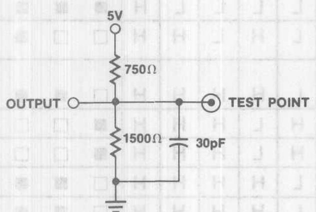
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA			–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45V			–0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V			40	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 6mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = –1mA COM I_{OH} = –2mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.5V			–100	μA
I_{OZH}	Off-state output current	V_{CC} = MAX	V_O = 2.4V			100	μA
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current	V_{CC} = 5V	V_O = 0V	–20		–90	mA
I_{CC}	Supply current	V_{CC} = MAX All inputs grounded All outputs open	Open collector			170	mA
			Three state			180	mA

Switching Characteristics

Over Operating Conditions

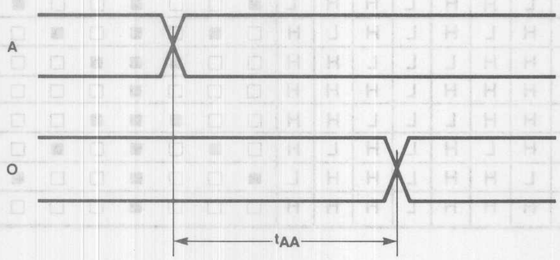
DEVICE TYPE	t_{AA}(ns) ADDRESS ACCESS TIME	t_{EA}(ns) ENABLE ACCESS TIME	t_{ER}(ns) ENABLE RECOVERY TIME
	MAX	MAX	MAX
6290/1, 6292/3	125	75	40
5290/1, 5292/3	150	85	50

Standard Test Load

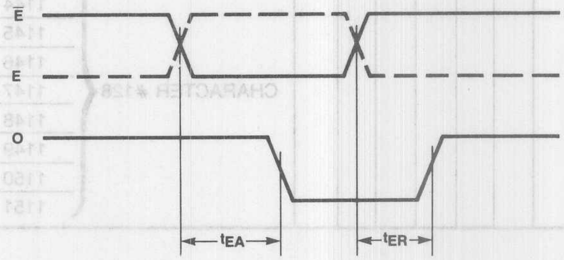


Input Pulse Amplitude 3.0V
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements Made at 1.5V

Definition of Waveforms



Address Access Time



Enable Access Time and Recovery Time

Custom Truth Table Coding—5290/1, 6290/1

7 x 9 ROW SCAN

The characters $, &, *, are shown below along with the ROM coding. A "filled in" dot is arbitrarily coded with a low (L)

CHARACTER SELECT A10	A9	A8	A7	A6	A5	A4		A3	A2	A1	A0	ROM WORD (DECIMAL)	OUTPUTS O7	O6	O5	O4	O3	O2	O1	FONT O7	O6	O5	O4	O3	O2	O1
L	L	L	L	L	L	L	CHARACTER #1	0	0	0	0	0	H	H	L	H	L	H	H	□	□	■	□	■	□	□
								0	0	0	1	1	H	L	L	L	L	L	L	□	■	■	■	■	■	■
								0	0	1	0	2	L	H	L	H	L	H	H	■	□	■	□	■	□	□
								0	0	1	1	3	L	H	L	H	L	H	H	■	□	■	□	■	□	□
								0	1	0	0	4	H	L	L	L	L	L	H	□	■	■	■	■	■	□
								0	1	0	1	5	H	H	L	H	L	H	L	□	□	■	□	■	□	■
								0	1	1	0	6	H	H	L	H	L	H	L	□	□	■	□	■	□	■
								0	1	1	1	7	L	L	L	L	L	L	H	■	■	■	■	■	■	□
								1	0	0	0	8	H	H	L	H	L	H	H	□	□	■	□	■	□	□
L	L	L	L	L	L	H	CHARACTER #2					9	H	L	L	H	H	H	H	□	■	■	□	□	□	□
												10	L	H	H	L	H	H	H	■	□	□	■	□	□	□
												11	L	H	H	L	H	H	H	■	□	□	■	□	□	□
												12	H	L	L	H	H	H	H	□	■	■	□	□	□	□
												13	H	L	L	H	H	H	H	□	■	■	□	□	□	□
												14	L	H	H	L	H	L	H	■	□	□	■	□	■	□
												15	L	H	H	H	L	L	H	■	□	□	□	■	■	□
												16	L	H	H	H	H	L	H	■	□	□	□	□	■	□
												17	H	L	L	L	L	H	L	□	■	■	■	■	□	■
H	H	H	H	H	H	H	CHARACTER #128					1143	H	H	H	L	H	H	H	□	□	□	■	□	□	□
												1144	L	H	H	L	H	H	L	■	□	□	■	□	□	■
												1145	H	L	H	L	H	L	H	□	■	□	■	□	■	□
												1146	H	H	L	L	L	H	H	□	□	■	■	■	□	□
												1147	H	H	H	L	H	H	H	□	□	□	■	□	□	□
												1148	H	H	L	L	L	H	H	□	□	■	■	■	□	□
												1149	H	L	H	L	H	L	H	□	■	□	■	□	■	□
												1150	L	H	H	L	H	H	L	■	□	□	■	□	□	■
												1151	H	H	H	L	H	H	H	□	□	□	■	□	□	□

Use of Custom Truth Table Form—5290/1, 6290/1

Truth table forms are available from Monolithic Memories upon request. For customers desiring to make their own forms an example is shown below coded to the 7 x 9 Row Scan example:

WORD NUMBER	OUTPUTS PIN	16 O_7	15 O_6	14 O_5	13 O_4	11 O_3	10 O_2	9 O_1
0		H	H	L	H	L	H	H
1		H	L	L	L	L	L	L
•		•	•	•	•	•	•	•
•		•	•	•	•	•	•	•
•		•	•	•	•	•	•	•
1151		H	H	H	L	H	H	H

NOTE:
A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pin so for example word 511 = HHHHHHHHH.

Custom Truth Table Coding—5292/3, 6292/3

9 x 9 COLUMN SCAN

The characters $, &, *, can be seen in the font if this page is rotated 90° clockwise. A "filled in" dot is arbitrarily coded with a low (L).

9 x 9 ROW SCAN

The 9 x 9 row scan translation would be similar to the 7 x 9 row scan previously shown except that there would be a 9 x 9 font for each character and outputs 8 and 9 in the ROM would be used and coded.

CHARACTER SELECT								ROM WORD (DECIMAL)	OUTPUTS									FONT								
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4			O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
L	L	L	L	L	L	L	CHARACTER #1	8	H	L	H	H	H	L	L	H	H	□	■	□	□	□	■	■	□	□
								7	H	L	H	H	L	H	H	L	H	□	■	□	□	■	□	□	■	□
								6	H	L	H	H	L	H	H	L	H	□	■	□	□	■	□	□	■	□
								5	L	L	L	L	L	L	L	L	L	■	■	■	■	■	■	■	■	■
								4	H	L	H	H	L	H	H	L	H	□	■	□	□	■	□	□	■	□
								3	L	L	L	L	L	L	L	L	L	■	■	■	■	■	■	■	■	■
								2	H	L	H	H	L	H	H	L	H	□	■	□	□	■	□	□	■	□
								1	H	L	H	H	L	H	H	L	H	□	■	□	□	■	□	□	■	□
								0	H	H	L	L	H	H	H	L	H	□	□	■	■	□	□	□	■	□
L	L	L	L	L	L	H	CHARACTER #2	17	H	H	H	H	H	H	H	H	H	□	□	□	□	□	□	□	□	□
								16	H	H	H	H	H	H	L	H	L	□	□	□	□	□	□	■	□	■
								15	H	H	H	H	H	H	L	L	H	□	□	□	□	□	□	■	■	□
								14	H	H	H	H	H	H	L	H	L	□	□	□	□	□	□	■	□	■
								13	H	L	L	L	L	L	H	H	L	□	■	■	■	■	■	□	□	■
								12	L	H	H	L	L	H	H	H	L	■	□	□	■	■	□	□	□	■
								11	L	H	H	L	L	H	H	H	L	■	□	□	■	■	□	□	□	■
								10	L	H	H	L	L	H	H	L	H	■	□	□	■	■	□	□	■	□
								9	H	L	L	H	H	L	L	H	H	□	■	■	□	□	■	■	□	□
H	H	H	H	H	H	H	CHARACTER #128	1151	H	H	H	H	H	H	H	H	H	□	□	□	□	□	□	□	□	□
								1150	H	L	H	H	H	H	H	L	H	□	■	□	□	□	□	□	■	□
								1149	H	H	L	H	H	H	L	H	H	□	□	■	□	□	□	■	□	□
								1148	H	H	H	L	H	L	H	H	H	□	□	□	■	□	■	□	□	□
								1147	L	L	L	L	L	L	L	L	L	■	■	■	■	■	■	■	■	■
								1146	H	H	H	L	H	L	H	H	H	□	□	□	■	□	■	□	□	□
								1145	H	H	L	H	H	H	L	H	H	□	□	■	□	□	□	■	□	□
								1144	H	L	H	H	H	H	H	L	H	□	■	□	□	□	□	□	■	□
								1143	H	H	H	H	H	H	H	H	H	□	□	□	□	□	□	□	□	□

Use of Custom Truth Table Form—5292/3, 6292/3

Truth table forms are available from Monolithic Memories upon request. For customers desiring to make their own forms an example is shown below coded to the 9 x 9 column scan example:

WORD NUMBER	OUTPUTS									
	PIN	18	17	16	15	14	13	11	10	9
		O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0		H	H	L	L	H	H	H	L	H
1		H	L	H	H	L	H	H	L	H
•		•	•	•	•	•	•	•	•	•
•		•	•	•	•	•	•	•	•	•
•		•	•	•	•	•	•	•	•	•
1151		H	H	H	H	H	H	H	H	H

NOTE:
A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pin so for example word 511 = HHHHHHHHH.

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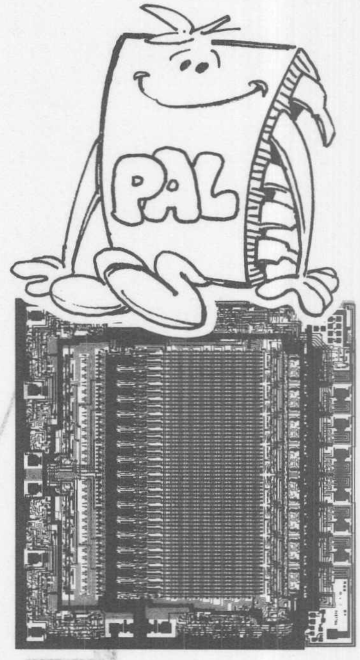


The PAL™ Concept

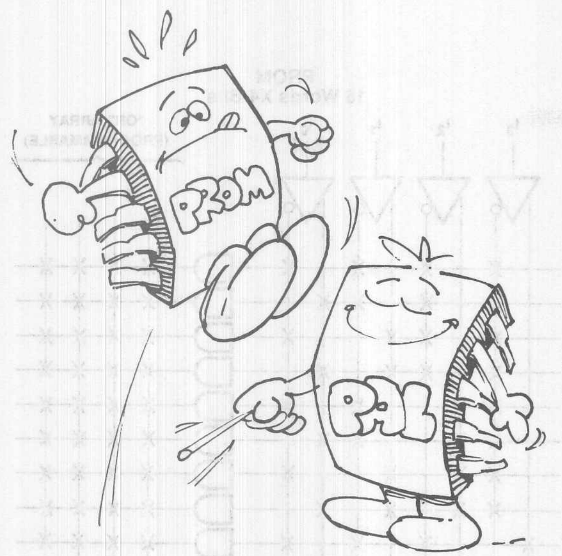
Monolithic Memories' family of PAL devices gives designers a powerful tool with unique capabilities for use in new and existing logic designs. The PAL saves time and money by solving many of the system partitioning and interface problems brought about by increases in semiconductor device technology.

Rapid advances in large scale integration technology have led to larger and larger standard logic functions; single I.C.s now perform functions that formerly required complete circuit cards. While LSI offers many advantages, advances have been made at the expense of device flexibility. Most LSI devices still require large numbers of SSI/MSI devices for interfacing with user systems. Designers are still forced to turn to random logic for many applications.

The designer is confronted with another problem when a low to medium complexity product is designed. Often the function is well defined and could derive significant benefits from fabrication as an integrated circuit. However, the design cycle for a custom circuit is long and the costs can be very high. This makes the risk significant enough to deter most users. The technology to support maximum flexibility combined with fast turn around on custom logic has simply not been available. Monolithic Memories offers the programmable solution.

The PAL family offers a fresh approach to using fuse programmable logic. PALs are a conceptually unified group of devices which combine programmable flexibility with high speed and an extensive selection of interface options. PALs can lower inventory, cut design cycles and provide high complexity with maximum flexibility. These features, combined with lower package count and high reliability, truly make the PAL a circuit designer's best friend.

The PAL—Teaching Old PROMs New Tricks



MMI developed the modern PROM and introduced many of the architectures and techniques now regarded as industry standards. As the world's largest PROM manufacturer, MMI has the proven technology and high volume production capability required to manufacture and support the PAL.

The PAL is an extension of the fusible link technology pioneered by Monolithic Memories for use in bi-polar PROMs. The fusible link PROM first gave the digital systems designer the power to "write on silicon." In a few seconds he was able to transform a blank PROM from a general purpose device into one containing a custom algorithm, microprogram, or Boolean transfer function. This opened up new horizons for the use of PROMs in computer control stores, character generators, data storage tables and many other applications. The wide acceptance of this technology is clearly demonstrated by today's multi-million dollar PROM market.

The key to the PROM's success is that it allows the designer to quickly and easily customize the chip to fit his unique requirements. The PAL extends this programmable flexibility by utilizing proven fusible link technology to implement logic functions. Using PALs the designer can quickly and effectively implement custom logic varying in complexity from random gates to complex arithmetic functions.

ANDs and ORs

The PAL implements the familiar sum of products logic by using a programmable AND array whose output terms feed a fixed OR array. Since the sum of products form can express any Boolean transfer function, the PAL's uses are only limited by the number of terms available in the AND - OR arrays. PAL's come in different sizes to allow for effective logic optimization.

Figure 1 shows the basic PAL structure for a two input, one output logic segment. The general logic equation for this segment is

$$\text{Output} = (I_1+\overline{f_1})(\overline{I_1}+\overline{f_2})(I_2+\overline{f_3})(\overline{I_2}+\overline{f_4}) + (I_1+\overline{f_5})(\overline{I_1}+\overline{f_6})(I_2+\overline{f_7})(\overline{I_2}+\overline{f_8})$$

where the "f" terms represent the state of the fusible links in the PAL's AND array. An unblown link represents a logic 1. Thus,

fuse blown, f = 0

fuse intact, f = 1

An unprogrammed PAL has all fuses intact.

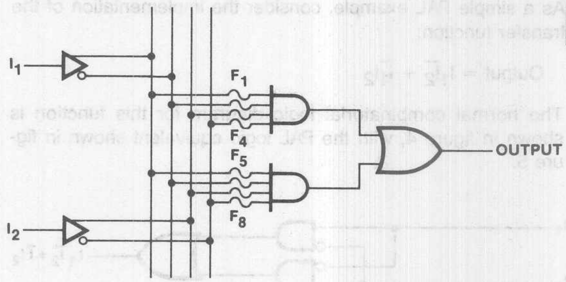


Figure 1

PAL Notation

Logic equations, while convenient for small functions, rapidly become cumbersome in large systems. To reduce possible confusion, complex logic networks are generally defined by logic diagrams and truth tables. Figure 2 shows the logic convention adopted to keep PAL logic easy to understand and use. In the figure, an "x" represents an intact fuse used to perform the logic AND function. (Note: the input terms on the common line with the x's are not connected together.) The logic symbology shown in Figure 2 has been informally adopted by integrated circuit manufacturers because it clearly establishes a one-to-one correspondence between the chip layout and the logic diagram. It also allows the logic diagram and truth table to be combined into a compact and easy to read form, thereby serving as a convenient shorthand for PALs. The two input - one output example from Figure 1 redrawn using the new logic convention is shown in Figure 3.

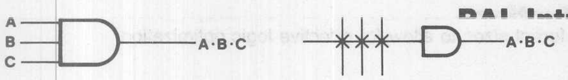


Figure 2

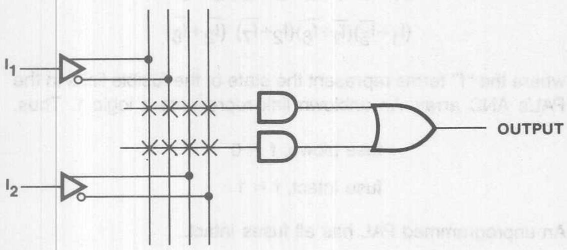


Figure 3

As a simple PAL example, consider the implementation of the transfer function:

$$\text{Output} = I_1\overline{I_2} + \overline{I_1}I_2$$

The normal combinatorial logic diagram for this function is shown in figure 4, with the PAL logic equivalent shown in figure 5.

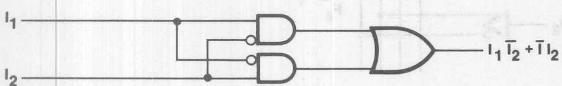


Figure 4

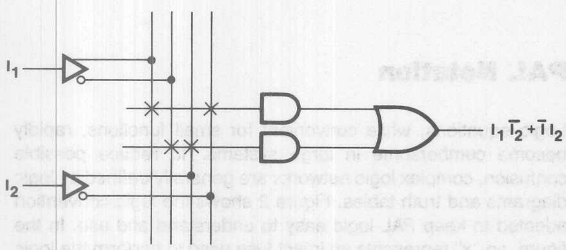


Figure 5

Using this logic convention it is now possible to compare the PAL structure to the structure of the more familiar PROM and PLA. The basic logic structure of a PROM consists of a fixed AND array whose outputs feed a programmable OR array (figure 6). PROMs are low-cost, easy to program, and available in a variety of sizes and organizations. They are most commonly

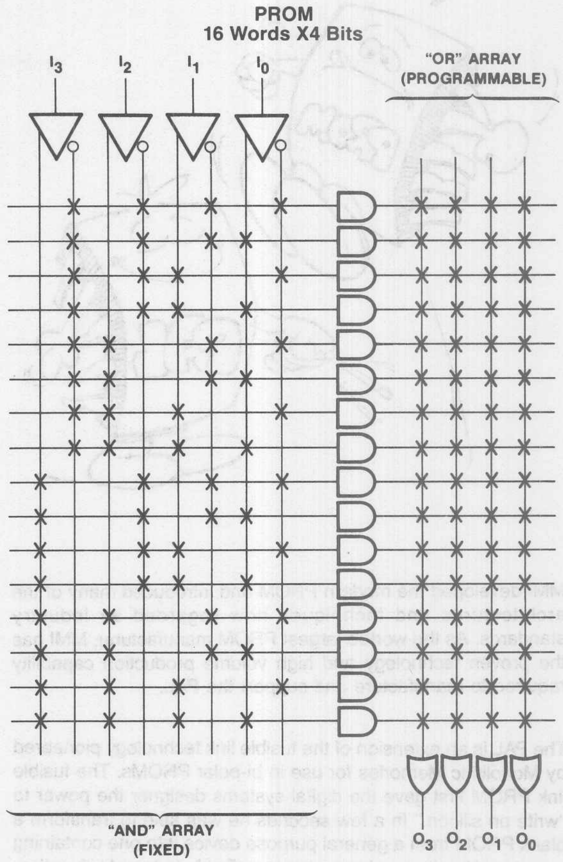


Figure 6

The basic logic structure of the PLA consists of a programmable AND array whose outputs feed a programmable OR array (Figure 7). Since the designer has complete control over all inputs and outputs, the PLA provides the ultimate flexibility for implementing logic functions. They are used in a wide variety of applications. However, this generality makes PLA's expensive, quite formidable to understand, and are costly to program (they require special programmers).

The basic logic structure of the PAL, as mentioned earlier, consists of a programmable AND array whose outputs feed a fixed OR array (Figure 8). The PAL combines much of the flexibility of the PLA with the low cost and easy programmability of the PROM. Table 1 summarizes the characteristics of the PROM, PLA, and PAL logic families.

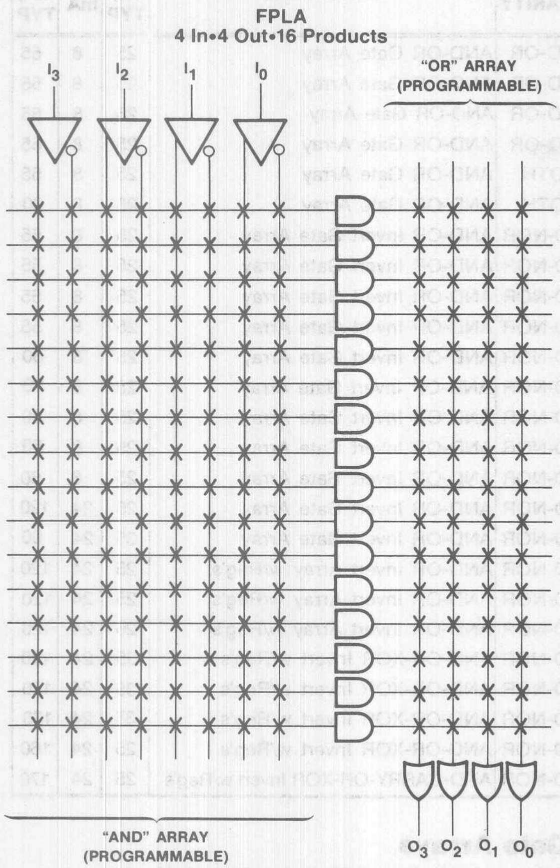


Figure 7

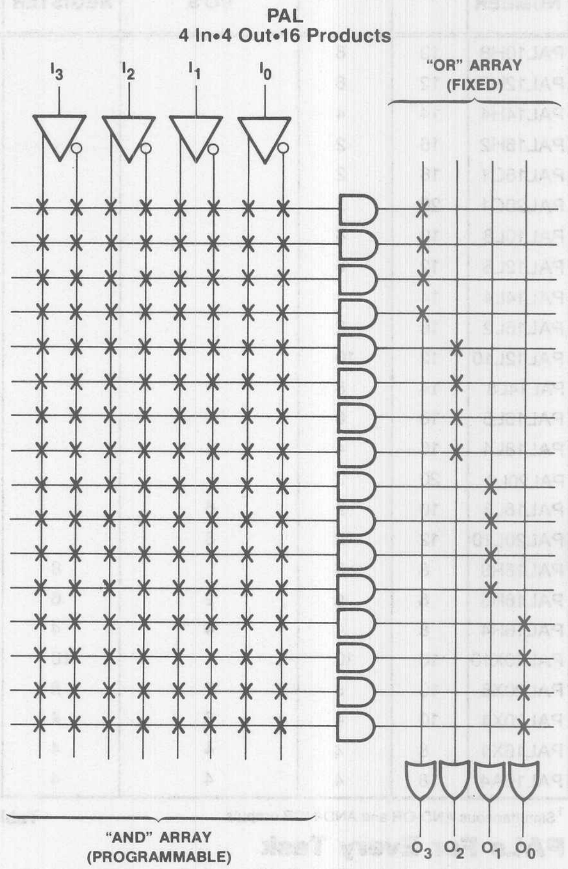


Figure 8

	AND	OR	OUTPUT OPTIONS
PROM	Fixed	Prog	TS, OC
FPLA	Prog	Prog	TS, OC, Fusible Polarity
FPGA	Prog	None	TS, OC, Fusible Polarity
FPLS	Prog	Prog	TS, Registered Feedback, I/O
PAL	Prog	Fixed	TS, Registered, Feedback, I/O

Table 1

6

PAL Input/Output/Function Chart

PART NUMBER	INPUT	OUTPUT	PROGRAMMABLE I/O'S	FEEDBACK REGISTER	OUTPUT POLARITY	FUNCTIONS	T_{PD} ns, TYP	I_{OL} mA	I_{CC} mA, TYP
PAL10H8	10	8			AND-OR	AND-OR Gate Array	25	8	55
PAL12H6	12	6			AND-OR	AND-OR Gate Array	25	8	55
PAL14H4	14	4			AND-OR	AND-OR Gate Array	25	8	55
PAL16H2	16	2			AND-OR	AND-OR Gate Array	25	8	55
PAL16C1	16	2			BOTH	AND-OR Gate Array	25	8	55
PAL20C1	20	2			BOTH	AND-OR Gate Array	25	8	60
PAL10L8	10	8			AND-NOR	AND-OR Invert Gate Array	25	8	55
PAL12L6	12	6			AND-NOR	AND-OR Invert Gate Array	25	8	55
PAL14L4	14	4			AND-NOR	AND-OR Invert Gate Array	25	8	55
PAL16L2	16	2			AND-NOR	AND-OR Invert Gate Array	25	8	55
PAL12L10	12	10			AND-NOR	AND-OR Invert Gate Array	25	8	60
PAL14L8	14	8			AND-NOR	AND-OR Invert Gate Array	25	8	60
PAL16L6	16	6			AND-NOR	AND-OR Invert Gate Array	25	8	60
PAL18L4	18	4			AND-NOR	AND-OR Invert Gate Array	25	8	60
PAL20L2	20	2			AND-NOR	AND-OR Invert Gate Array	25	8	60
PAL16L8	10	2	6		AND-NOR	AND-OR Invert Gate Array	25	24	120
PAL20L10	12	2	8		AND-NOR	AND-OR Invert Gate Array	35	24	90
PAL16R8	8	8		8	AND-NOR	AND-OR Invert Array w/Reg's	25	24	120
PAL16R6	8	6	2	6	AND-NOR	AND-OR Invert Array w/Reg's	25	24	120
PAL16R4	8	4	4	4	AND-NOR	AND-OR Invert Array w/Reg's	25	24	120
PAL20X10	10	10		10	AND-NOR	AND-OR-XOR Invert w/Reg's	35	24	120
PAL20X8	10	8	2	8	AND-NOR	AND-OR-XOR Invert w/Reg's	35	24	120
PAL20X4	10	4	6	4	AND-NOR	AND-OR-XOR Invert w/Reg's	35	24	120
PAL16X4	8	4	4	4	AND-NOR	AND-OR-XOR Invert w/Reg's	25	24	160
PAL16A4	8	4	4	4	AND-NOR	AND-CARRY-OR-XOR Invert w/Reg's	25	24	170

[1] Simultaneous AND-OR and AND-NOR outputs

Table 2

PALs For Every Task

The members of the PAL family and their characteristics are summarized in Table 2. They are designed to cover the spectrum of logic functions at reduced cost and lower package count. This allows the designer to select the PAL that best fits his application. PALs come in the following basic configurations:

Gate Arrays

PAL gate arrays are available in sizes from 12x10 (12 input terms, 10 output terms) to 20x2, with both active high and active low output configurations available. This wide variety of input/output formats allows the PAL to replace many different sized blocks of combinatorial logic with single packages.

Programmable I/O

A feature of the high-end members of the PAL family is programmable input/output. This allows the product terms to directly control the outputs of the PAL (Figure 9). One product term is used to enable the three-state buffer, which in turn gates the summation term to the output pin. The output is also fed back into the PAL array as an input. Thus the PAL drives the I/O pin when the three-state gate is enabled; the I/O pin is an input to the PAL array when the three-state gate is disabled. This feature can be used to allocate available pins for I/O functions or to provide bi-directional output pins for operations such as shifting and rotating serial data.

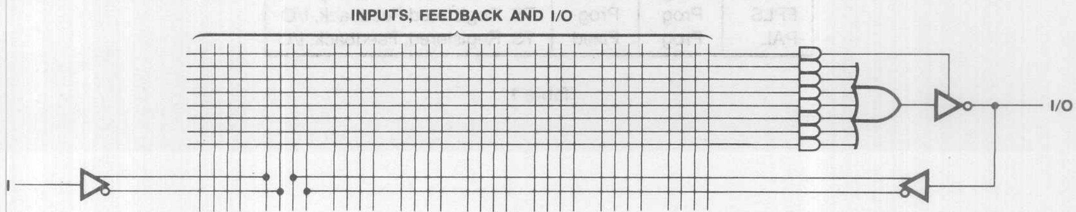


Figure 9

Registered Outputs with Feedback

Another feature of the high end members of the PAL family is registered data outputs with register feedback. Each product term is stored into a D-type output flip-flop on the rising edge of the system clock (Figure 10). The Q output of the flip-flop can then be gated to the output pin by enabling the active low three-state buffer.

In addition to being available for transmission, the Q output is fed back into the PAL array as an input term. This feedback allows the PAL to "remember" the previous state, and it can alter its function based upon that state. This allows the designer to configure the PAL as a state sequencer which can be programmed to execute such elementary functions as count up, count down, skip, shift, and branch. These functions can be executed by the registered PAL at rates of up to 20 MHz.

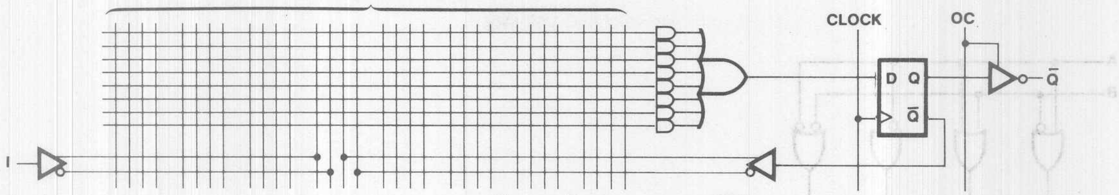


Figure 10

XOR PALs

These PALs feature an exclusive OR function. The sum of products is segmented into two sums which are then exclusive ORed (XOR) at the input of the D-type flip-flop. All of the features of the Registered PALs are included in the XOR PALs. The XOR function provides an easy implementation of the HOLD operation used in counters.

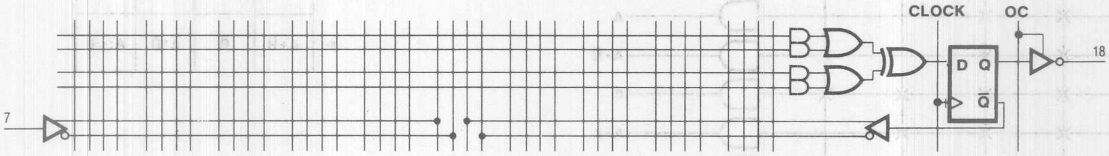


Figure 11

Arithmetic Gated Feedback

The arithmetic functions add, subtract, greater than, and less than are implemented by addition of gated feedback to the features of the XOR PALs. The XOR at the input of the D-type flip-flop allows carrys from previous operations to be XORed with two variable sums generated by the PAL array. The flip-flop Q output is fed back to be gated with input terms I. This gated feedback provides any one of the 16 possible Boolean combinations which are mapped in the Karnaugh map (figure 14). Figure 13 shows how the PAL array can be programmed to perform these 16 operations. These features provide for versatile operations on two variables and facilitate the parallel generation of carrys necessary for fast arithmetic operations.

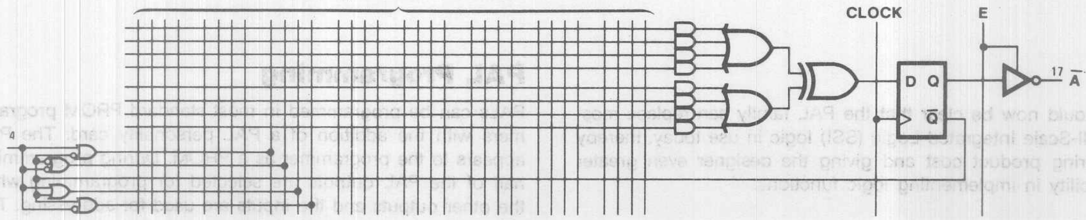


Figure 12

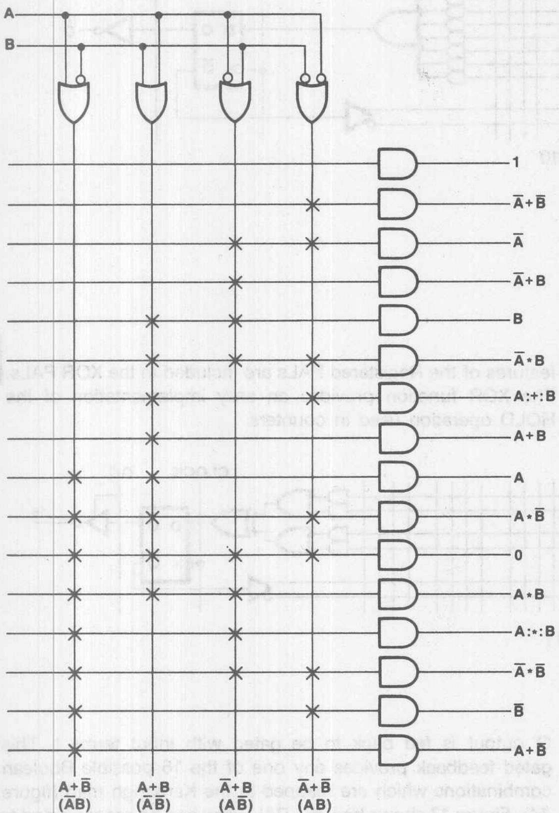


Figure 13

$(\overline{A}+B), (\overline{A}+\overline{B})$ / $(A+\overline{B}), (A+B)$	--	-x	xx	x-
--	1	$\overline{A}+\overline{B}$	$\overline{A}$	$\overline{A}+B$
-x	A+B	A:+:B	$\overline{A}*B$	B
xx	A	$A*\overline{B}$	0	A * B
x-	$A+\overline{B}$	$\overline{B}$	$\overline{A}*\overline{B}$	A:*:B

Figure 14

It should now be clear that the PAL family can replace most Small-Scale Integrated Logic (SSI) logic in use today, thereby lowering product cost and giving the designer even greater flexibility in implementing logic functions.

PAL Programming

PALs can be programmed in most standard PROM programmers with the addition of a PAL personality card. The PAL appears to the programmer as a PROM. During programming half of the PAL outputs are selected for programming while the other outputs and the inputs are used for addressing. The outputs are then switched to program the other locations. Verification uses the same procedure with the programming lines held in a low state.

PAL Technology

PALs are manufactured using the proven TTL Schottky bipolar Ti-W fuse process used to make fusible-link PROMs. An NPN emitter follower array forms the programmable AND array. PNP inputs provide high-impedance inputs (0.25 mA max) to the array. All outputs are standard TTL drivers with internal active pull-up transistors. Typical PAL propagation delay time is 25 ns, and all PALs are packaged in space saving 20-pin and 24-pin SKINNYDIP™.

PAL Data Security

The circuitry used for programming and logic verification can be used at any time to determine the logic pattern stored in the PAL array. For security, the PAL has a "last fuse" which can be blown to disable the verification logic. This provides a significant deterrent to potential copiers, and it can be used to effectively protect proprietary designs.

Programmable Array Logic Family

PAL® Series 20

U.S. Patent 4124899

March 1981

Features/Benefits

- Programmable replacement for conventional TTL logic.
- Reduces IC inventories substantially and simplifies their control.
- Reduces chip count by 4 to 1.
- Expedites and simplifies prototyping and board layout.
- Saves space with 20-pin SKINNY DIP® packages.
- High speed: 25ns typical propagation delay.
- Programmed on standard PROM programmers.
- Programmable three-state outputs.
- Special feature reduces possibility of copying by competitors.

Description

The PAL family utilizes an advanced Schottky TTL process and the Bipolar PROM fusible link technology to provide user programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The family lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production.

The PAL transfer function is the familiar sum of products. Like the PROM, the PAL has a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array). In addition the PAL provides these options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback
- Arithmetic capability

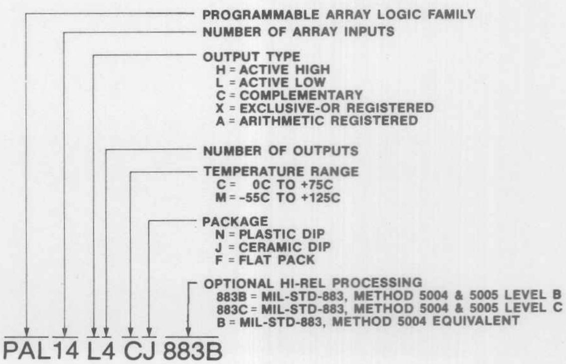
PAL® is a registered trademark of Monolithic Memories.

PART NUMBER	PKG	DESCRIPTION
PAL10H8	N,J,F	Octal 10 Input And-Or Gate Array
PAL12H6	N,J,F	Hex 12 Input And-Or Gate Array
PAL14H4	N,J,F	Quad 14 Input And-Or Gate Array
PAL16H2	N,J,F	Dual 16 Input And-Or Gate Array
PAL16C1	N,J,F	16 Input And-Or/And-Or-Invert Gate Array
PAL10L8	N,J,F	Octal 10 Input And-Or-Invert Gate Array
PAL12L6	N,J,F	Hex 12 Input And-Or-Invert Gate Array
PAL14L4	N,J,F	Quad 14 Input And-Or-Invert Gate Array
PAL16L2	N,J,F	Dual 16 Input And-Or-Invert Gate Array
PAL16L8	N,J,F	Octal 16 Input And-Or-Invert Gate Array
PAL16R8	N,J,F	Octal 16 Input Registered And-Or Gate Array
PAL16R6	N,J,F	Hex 16 Input Registered And-Or Gate Array
PAL16R4	N,J,F	Quad 16 Input Registered And-Or Gate Array
PAL16X4	N,J	Quad 16 Input Registered And-Or-Xor Gate Array
PAL16A4	N,J	Quad 16 Input Registered And-Carry-Or-Xor Gate

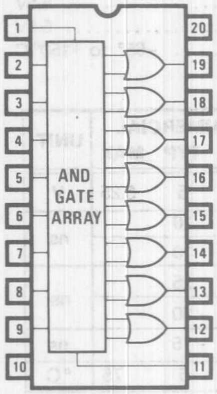
Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops which are loaded on the low to high transition of the clock. PAL Logic Diagrams are shown with all fuses blown, enabling the designer use of the diagrams as coding sheets.

The entire PAL family is programmed on inexpensive conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

Ordering Information



1165 East Arques Avenue, Sunnyvale, CA 94086 Tel: (408) 739-3535 TWX: 910-339-9229

PAL10H8


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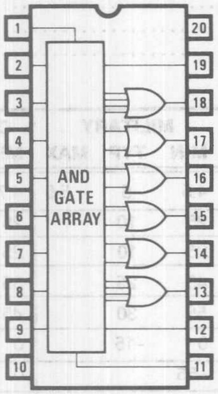

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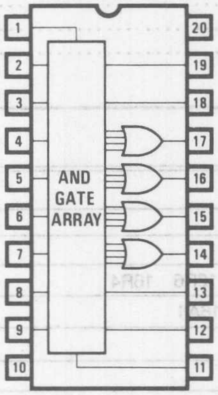

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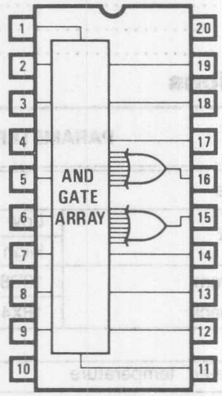

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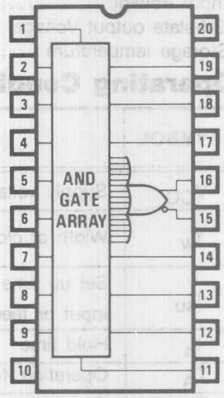

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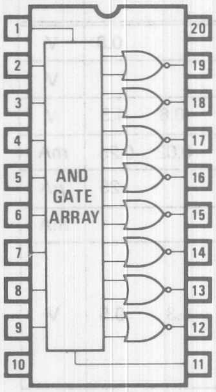

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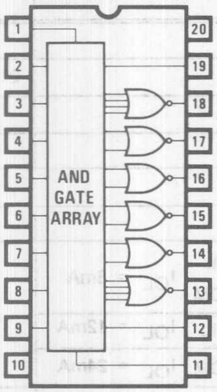

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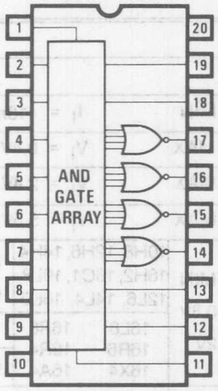

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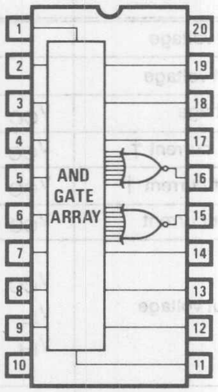

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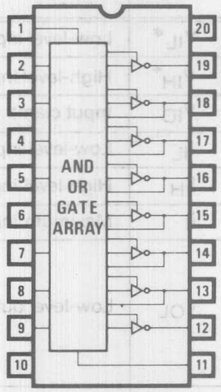

6

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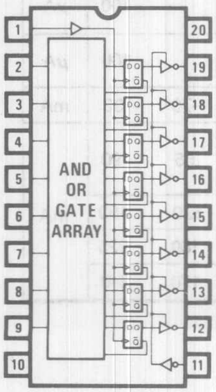

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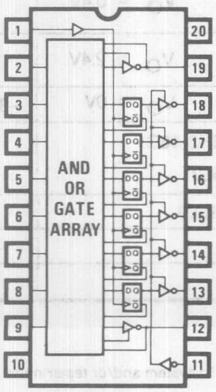

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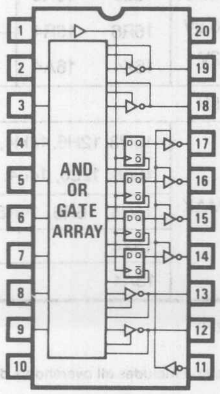

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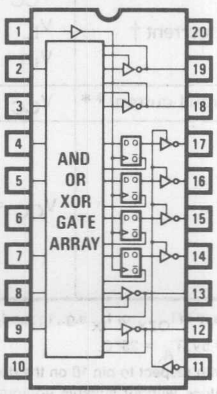

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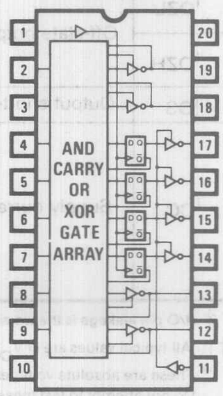


Off-state output Voltage 5.5V
Storage temperature .... –65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	25	10		25	10		ns
		High	25	10		25	10		
t_{su}	Set up time from input or feedback	16R8 16R6 16R4	45	25		35	25		ns
		16X4 16A4	55	30		45	30		
t_h	Hold time		0	–15		0	–15		ns
T_A	Operating free-air temperature		–55			0	5	75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

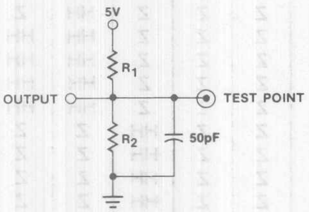
SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = –18mA		–0.8	–1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX		V_I = 0.4V		–0.02	–0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX		V_I = 2.4V			25	µA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	10H8, 12H6, 14H4, 16H2, 16C1, 10L8, 12L6, 14L4, 16L2	MIL, COM: I_{OL} = 8mA		0.3	0.5	V
			16L8 16R8 16R6 16R4 16X4 16A4	MIL: I_{OL} = 12mA				
				COM: I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OH} = –2mA	2.4	2.8		V
			COM	I_{OH} = –3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	16L8 16R8 16R6 16R4 16X4 16A4	V_O = 0.4V			–100	µA
I_{OZH}				V_O = 2.4V			100	µA
I_{OS}	Output short-circuit current **	V_{CC} = 5V		V_O = 0V	–30	–70	–130	mA
I_{CC}	Supply current	V_{CC} = MAX	10H8, 12H6, 14H4, 16H2, 16C1, 10L8, 12L6, 14L4, 16L2			55	90	mA
			16R4, 16R6, 16R8, 16L8			120	180	
			16X4			160	225	
			16A4			170	240	

† I/O pin leakage is the worst case of I_{OZX} or I_{IX} e.g., I_{IL} and I_{OZH}.
†† All typical values are at V_{CC} = 5V, T_A = 25°C.
* These are absolute voltages with respect to pin 10 on the device and includes all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
** Only one output shorted at a time.

Switching Characteristics
Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input to output	10H8 12H6 14H4 16H2 10L8 12L6 14L4 16L2	$R_1 = 560\Omega$ $R_2 = 1.1k\Omega$		25	45		25	35	ns
		16C1			25	45		25	40	
t_{PD}	Input or feed-back to output	16R6 16R4 16L8			25	45		25	35	ns
		16X4 16A4			30	45		30	40	
t_{CLK}	Clock to output or feedback				15	25		15	25	ns
t_{PZY}	Pin 11 to output enable				15	25		15	25	ns
t_{PXZ}	Pin 11 to output disable		$R_1 = 200\Omega$ $R_2 = 390\Omega$		15	25		15	25	ns
t_{PZX}	Input to output enable	16R6 16R4 16L8			25	45		25	35	ns
		16X4 16A4			30	45		30	40	
t_{PXZ}	Input to output disable	16R6 16R4 16L8			25	45		25	35	ns
		16X4 16A4			30	45		30	40	
f_{MAX}	Maximum frequency	16R8 16R6 16R4		14	25		16	25		MHz
		16X4 16A4		12	22		14	22		

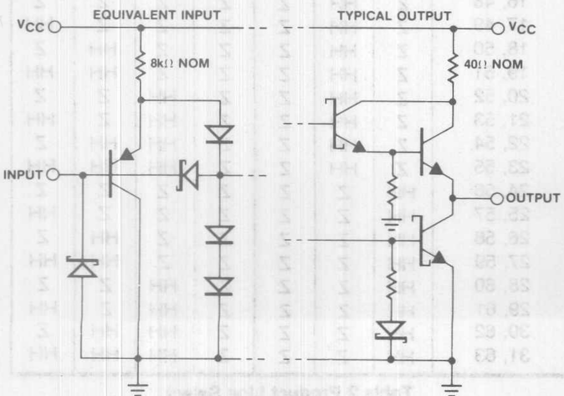
Test Load



Available Programmers

MANUFACTURER	PERSONALITY CARD SET	SOCKET ADAPTER CONFIGURATION
Data I/O Corporation	909-1427	715 1428-1 715 1428-2 715 1428-3
Pro-Log Corporation	PM9068	
Stag Systems	PM202	AM10H8 AM10L8 AM12H6 AM12L6 AM14H4 AM14L4 AM16H2 AM16L2 AM16C1
Structured Design	SD20/24	

Schematic of Inputs and Outputs



Programming

PAL fuses are programmed using a low-voltage linear-select procedure which is common to all 15 PAL types. The array is divided into two groups, products 0 thru 31 and products 32 thru 63, for which pin identifications are shown in Pin Configurations below. To program a particular fuse, both an input line and a product line are selected according to the following procedure:

Step 1 Raise Output Disable, OD, to V_{IHH}

Step 2 Select an input line by specifying $I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7$ and L/R as shown in Table 1.

Step 3 Select a product line by specifying A_0, A_1 and A_2 one-of-eight select as shown in Table 2.

Step 4 Raise V_{CC} (pin 20) to V_{IHH}

Step 5 Program the fuse by pulsing the output pins, O, of the selected product group to V_{IHH} as shown in Programming Waveform.

Step 6 Lower V_{CC} (pin 20) to 6.0 V

Step 7 Pulse the CLOCK pin and verify the output pin, O, to be Low for active Low PAL types or High for active High PAL types.

Step 8 Lower V_{CC} (pin 20) to 4.5 V and repeat step 7.

Step 9 Should the output not verify, repeat steps 1 thru 8 up to five (5) times.

This procedure is repeated for all fuses to be blown (see Programming Waveforms).

To prevent further verification, two last fuses may be blown by raising pin 1 and pin 11 to V_P. V_{CC} is not required during this operation.

Voltage Legend

L = Low-level input voltage, V_{IL}
H = High-level input voltage, V_{IH}
HH = High-level program voltage, V_{IHH}
Z = High impedance (e.g., 10kΩ to 5.0V)

INPUT LINE NUMBER	PIN IDENTIFICATION								
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	Z
29	H	HH	HH	HH	HH	HH	HH	HH	Z
30	L	HH	HH	HH	HH	HH	HH	HH	HH
31	H	HH	HH	HH	HH	HH	HH	HH	HH

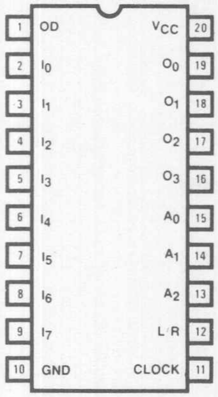
Table 1 Input Line Select

PRODUCT LINE NUMBER	PIN IDENTIFICATION						
	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

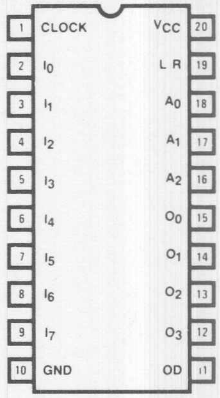
Table 2 Product Line Select

Pin Configurations

PRODUCTS 0 THRU 31



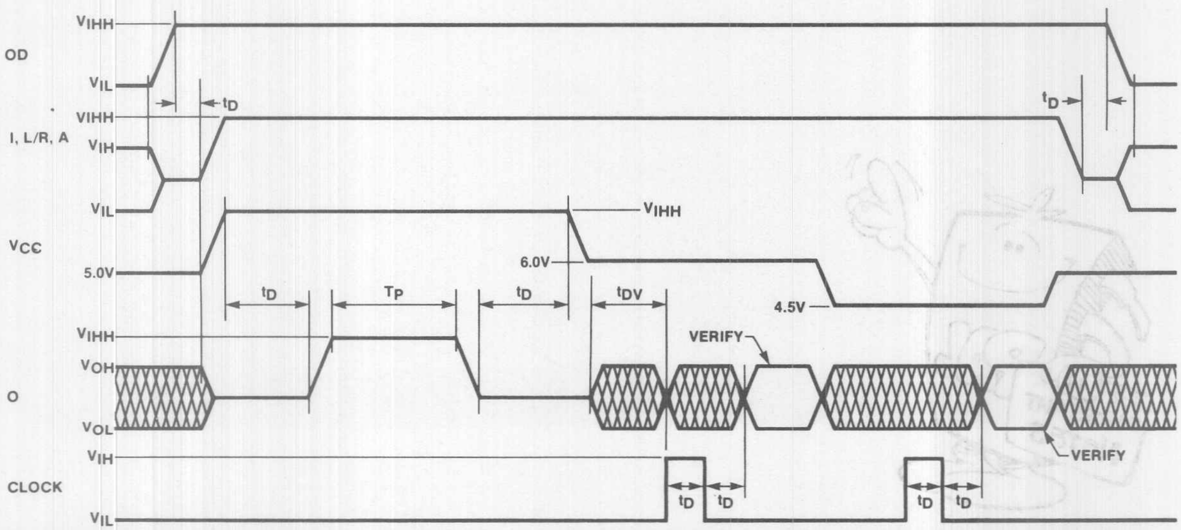
PRODUCTS 32 THRU 63



Programming Parameters $T_A = 25°C$

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNIT
V_{IHH}	Program-level input voltage		11	11.5	12	V
I_{IHH}	Program-level input current	Output Program Pulse			50	mA
		OD, L/R			25	
		All Other Inputs			5	
I_{CCH}	Program Supply Current				400	mA
T_P	Program Pulse Width		10		50	μs
t_D	Delay time		100			ns
t_{DV}	Delay Time to Verify		100			μs
	Program Pulse duty cycle				25	%
V_P	Verify-Protect-input voltage		20	21	22	V
I_P	Verify-Protect-input current				400	mA
T_{PP}	Verify-Protect Pulse Width		20		50	msec

Programming Waveforms



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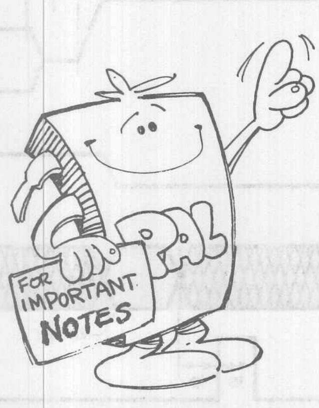
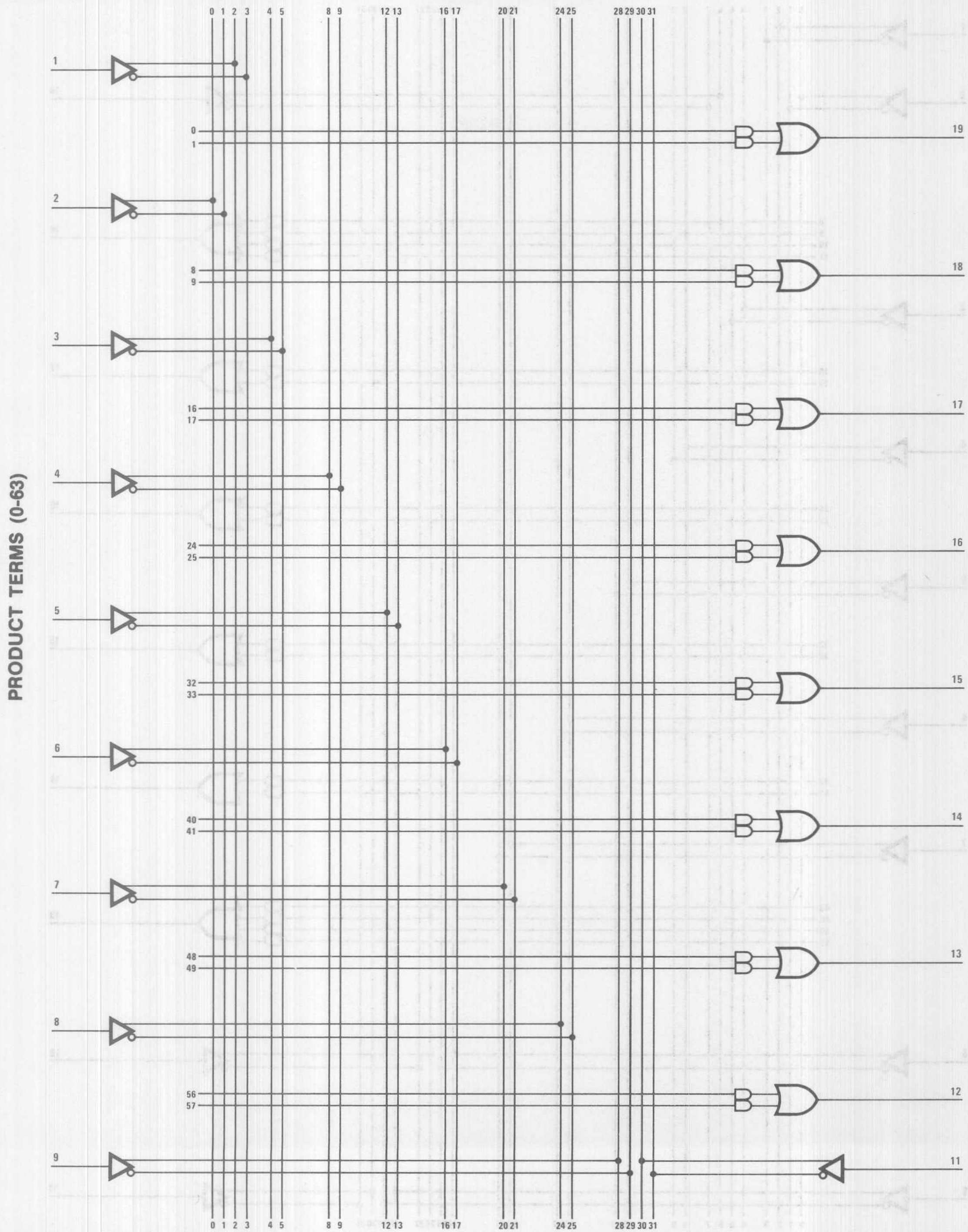
Notes




PRODUCT TERMS (0-63)
0 1 2 3 4 5 8 9 12 13 16 17 20 21 24 25 28 29 30 31
1
2
3
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9
11
12
13
14
15
16
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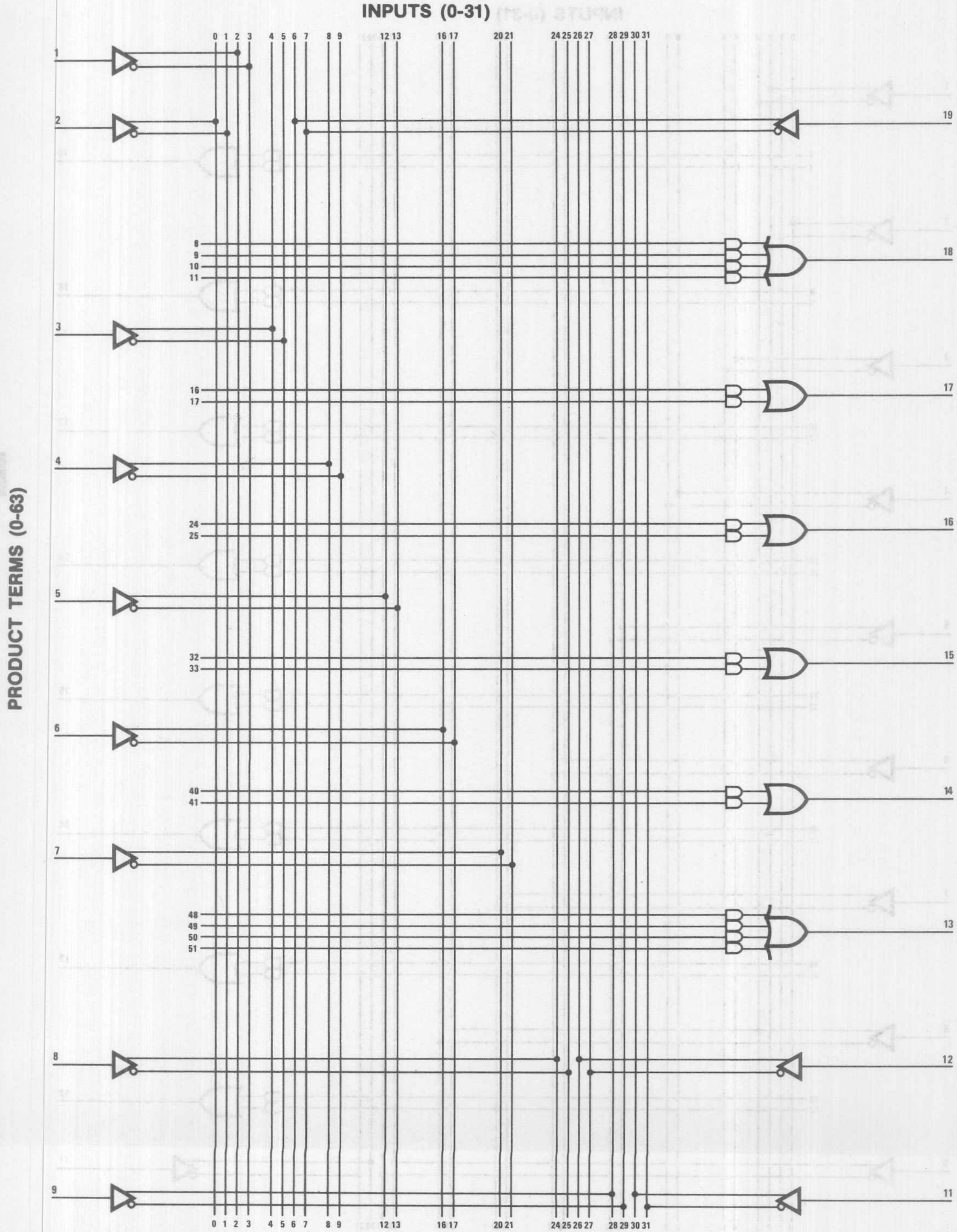
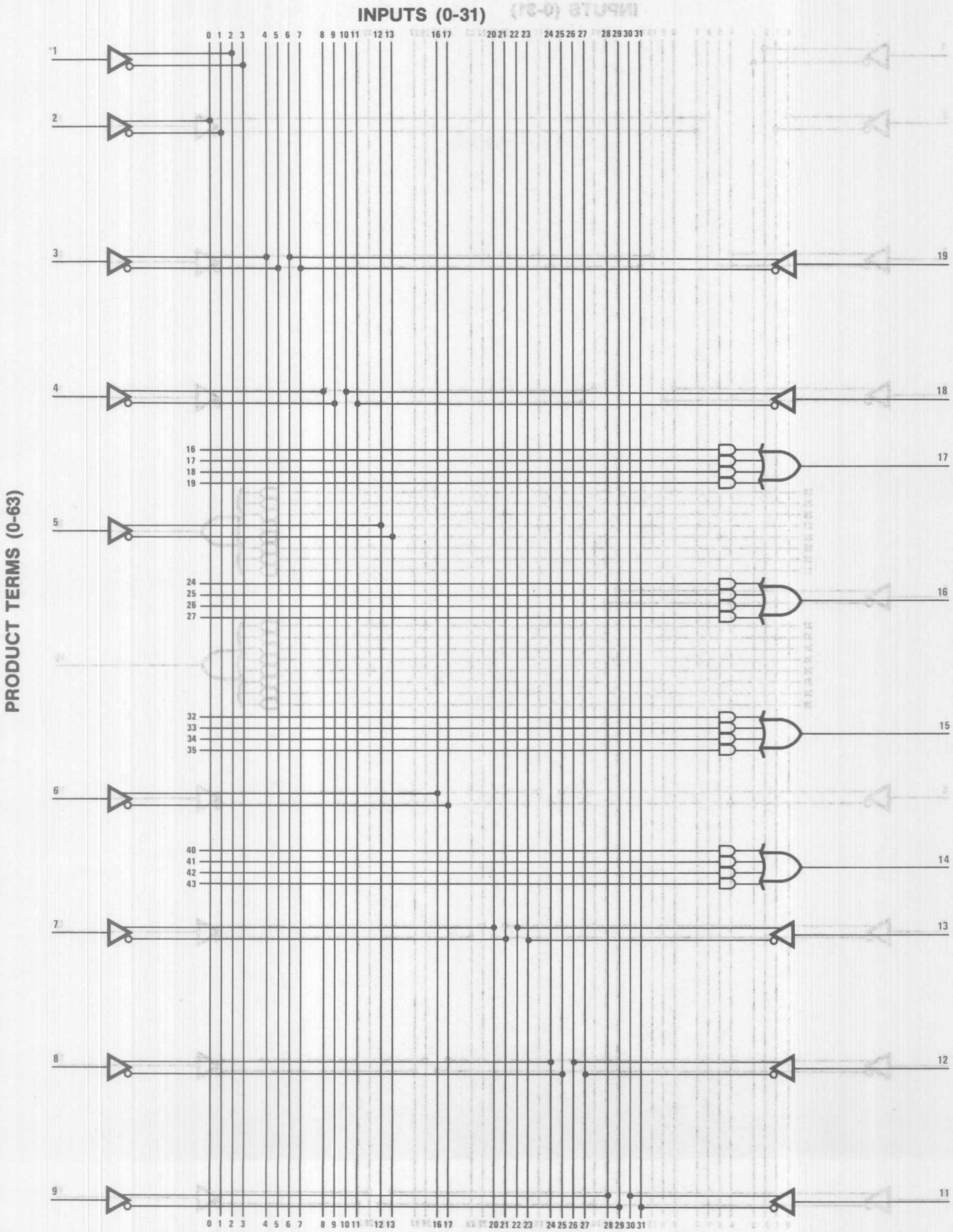
Logic Diagram PAL12H6

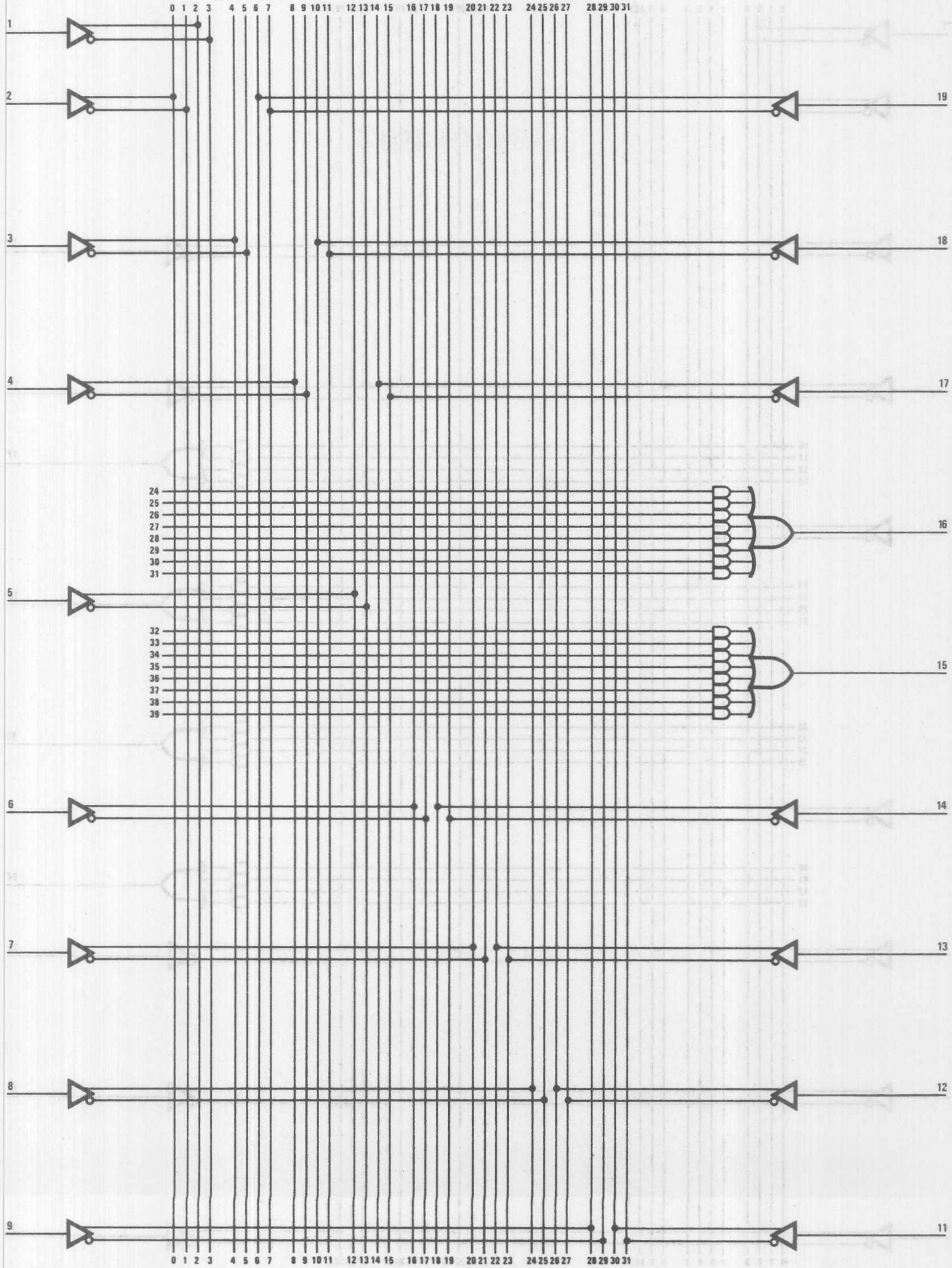


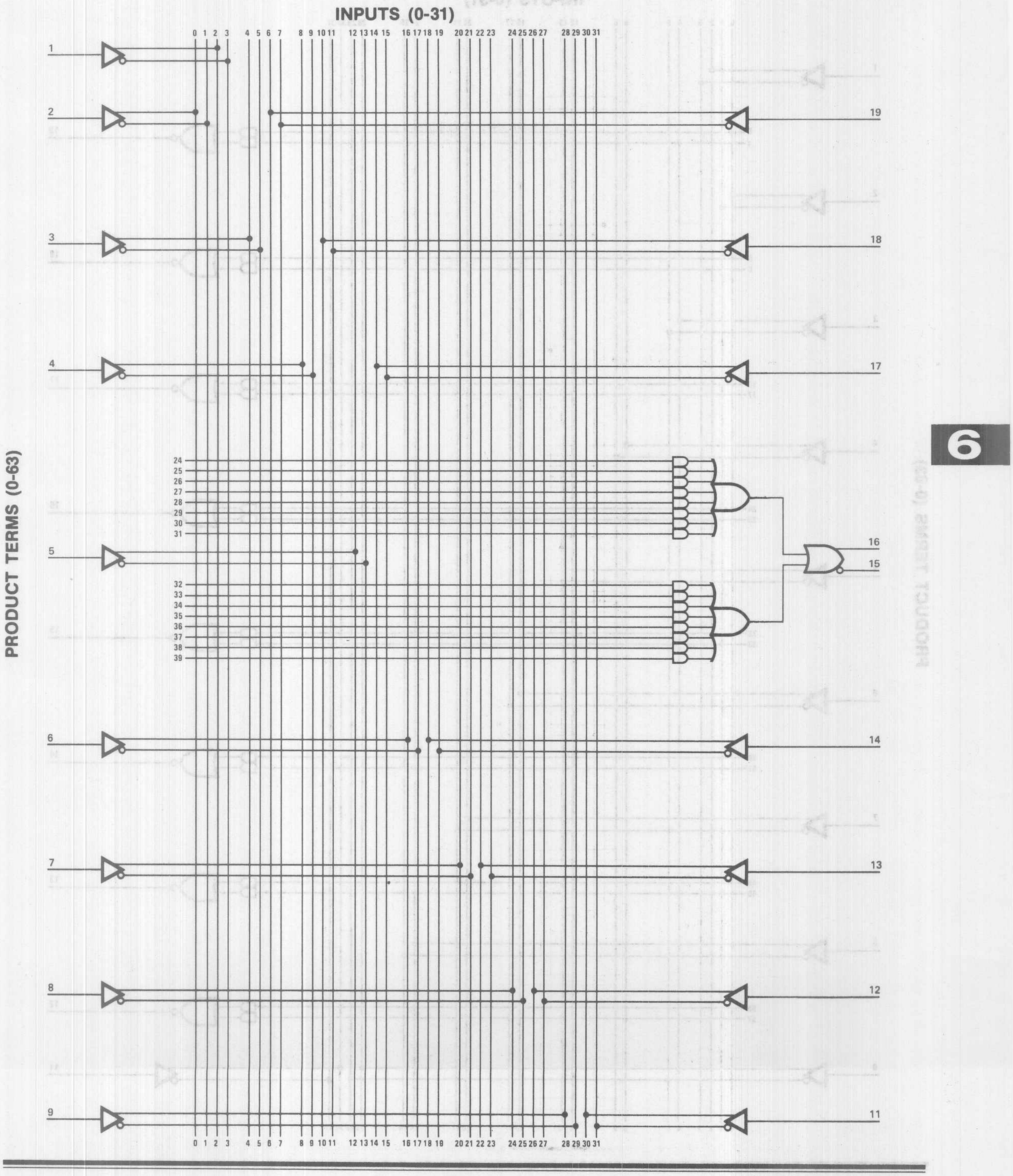
Logic Diagram PAL14H4



6

PRODUCT TERMS (0-63)




INPUTS (0-31)
PRODUCT TERMS (0-63)
1
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14
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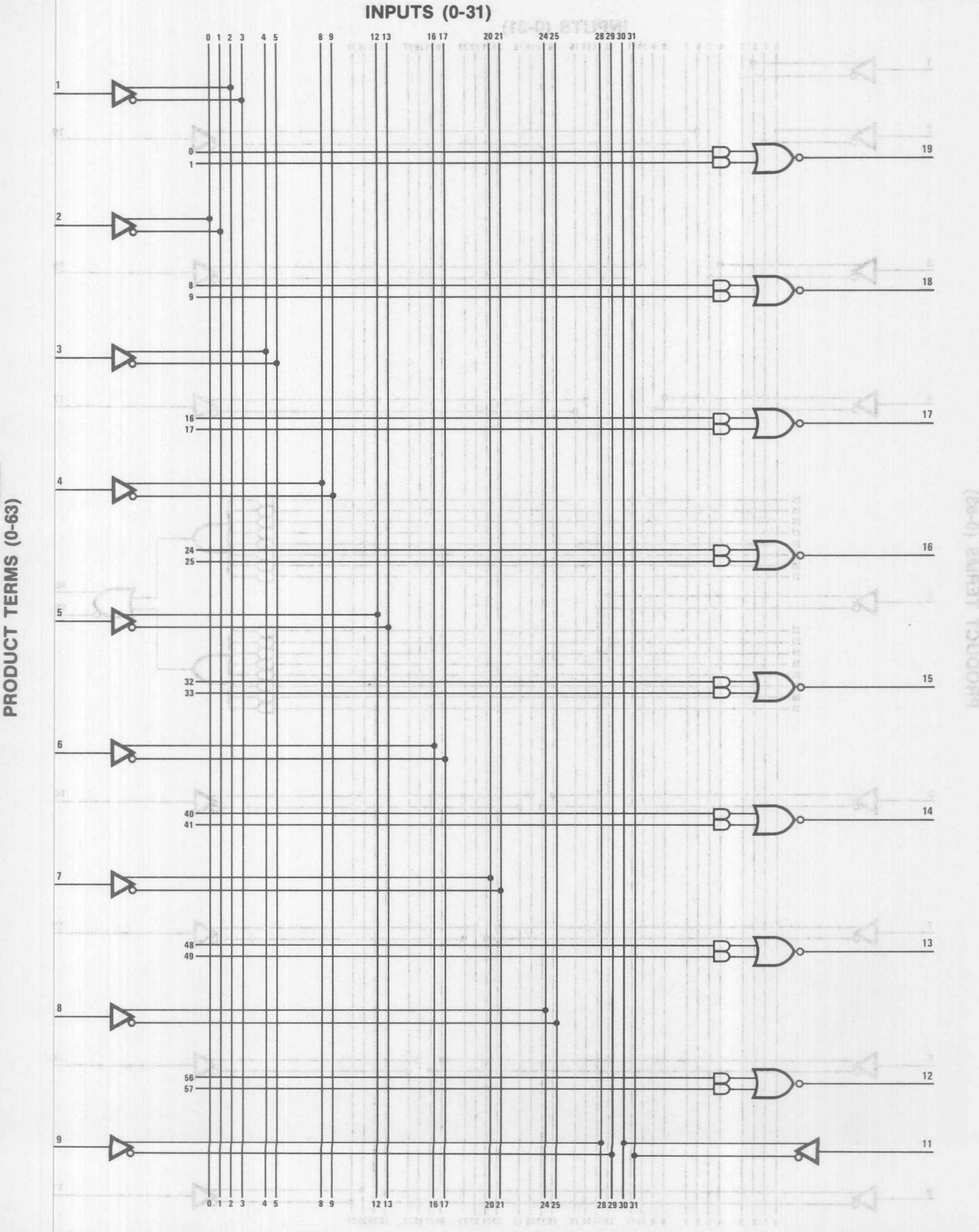
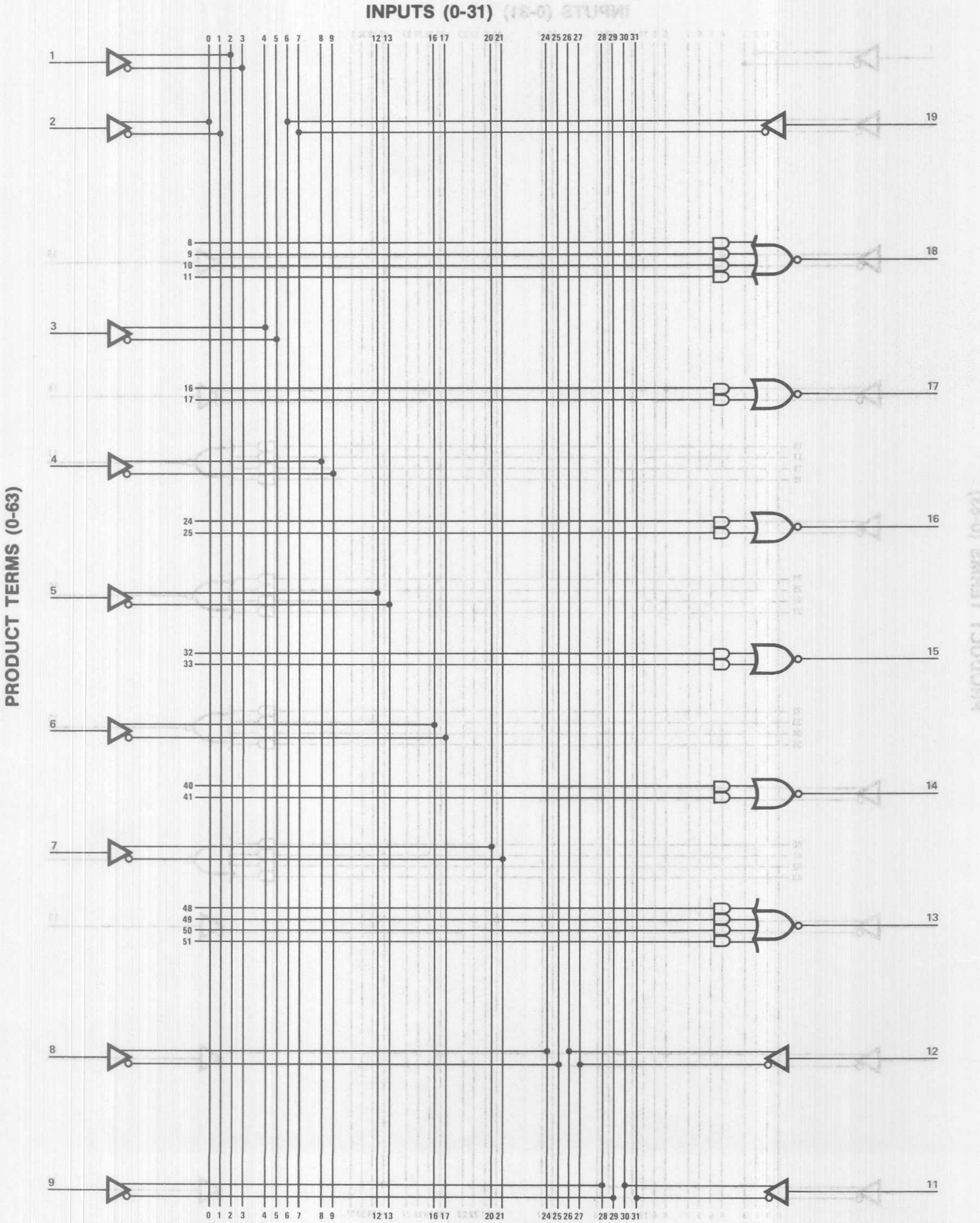
Logic Diagram PAL10L8



Logic Diagram PAL12L6



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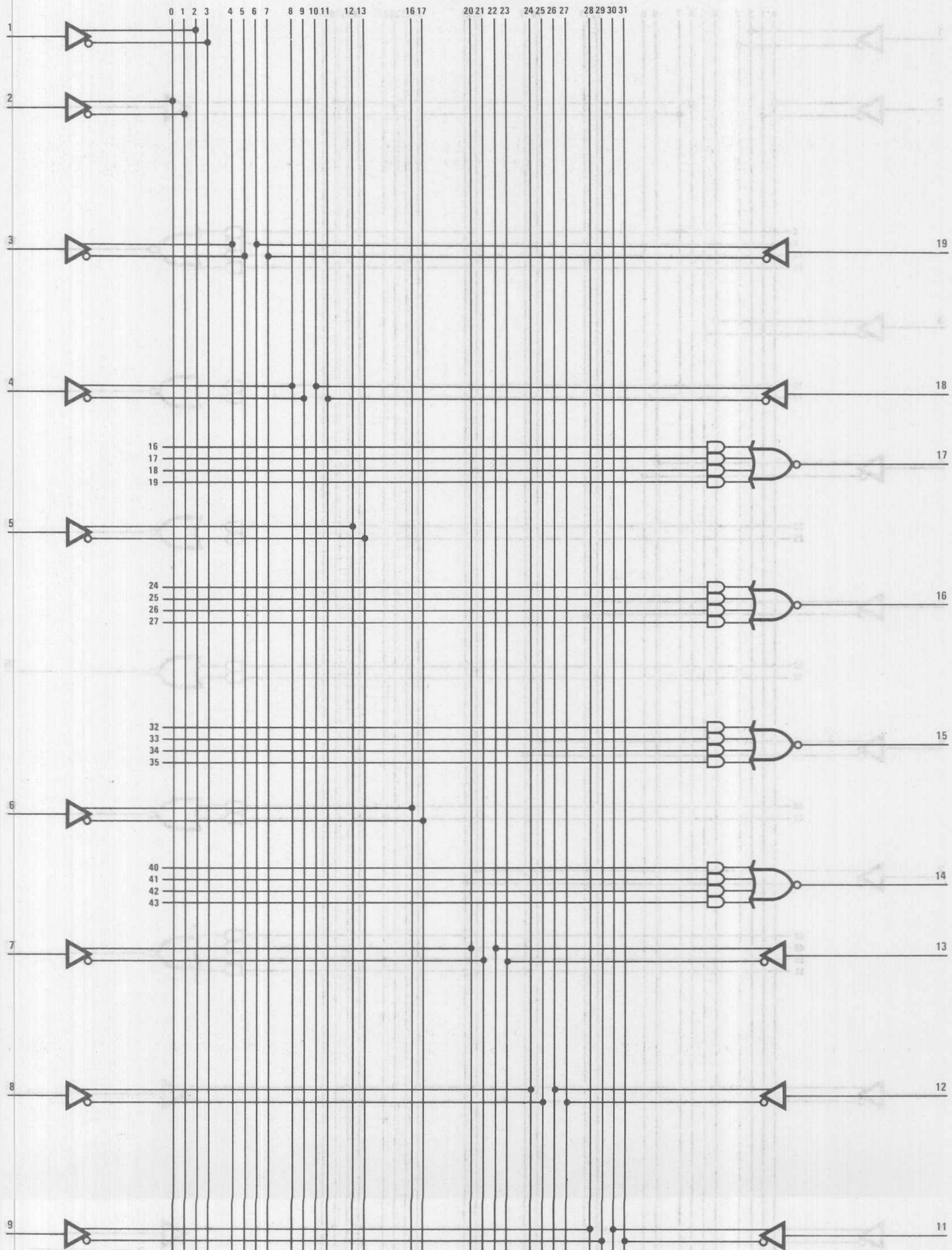
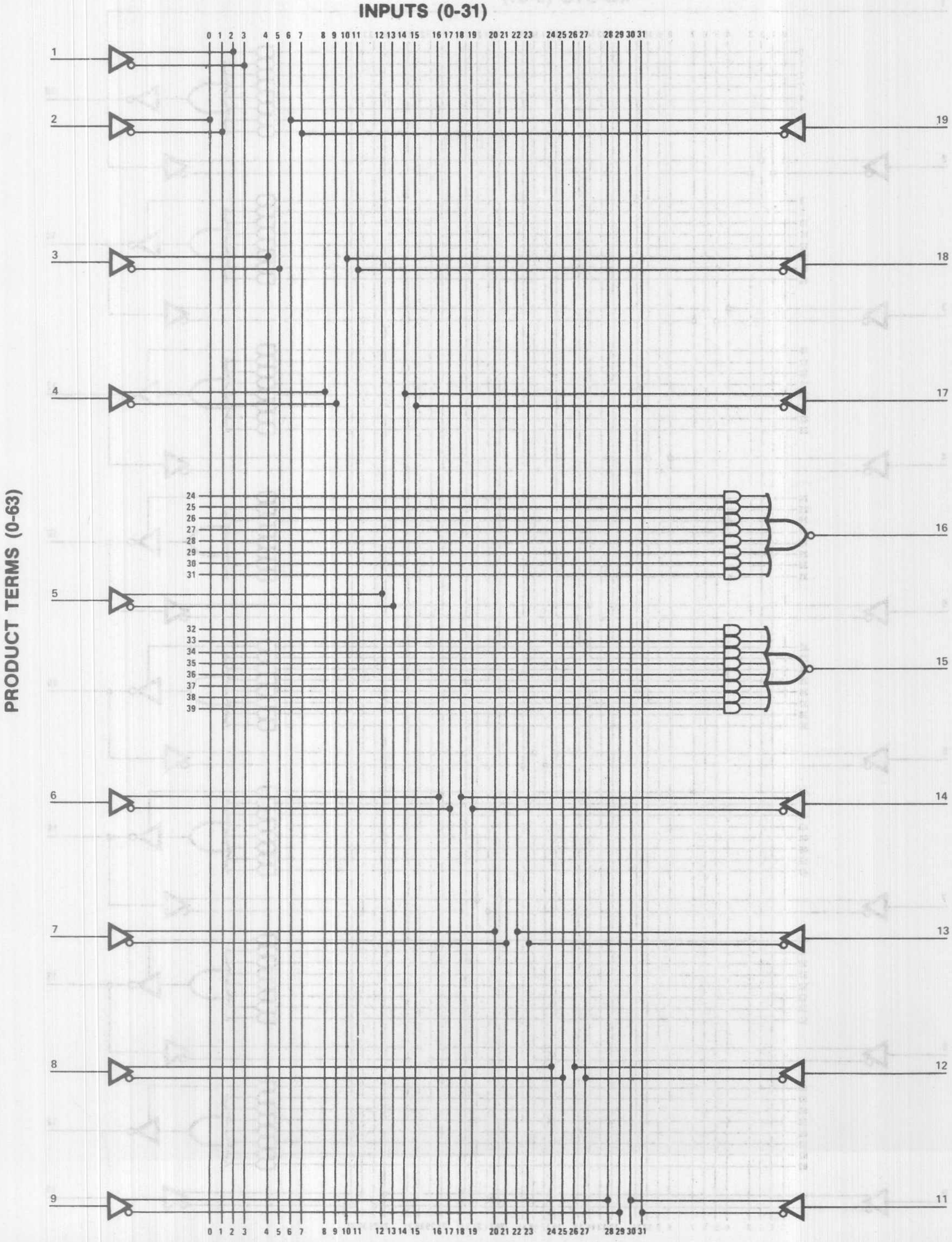

PRODUCT TERMS (0-63)


INPUTS (0-31)
PRODUCT TERMS (0-63)
1
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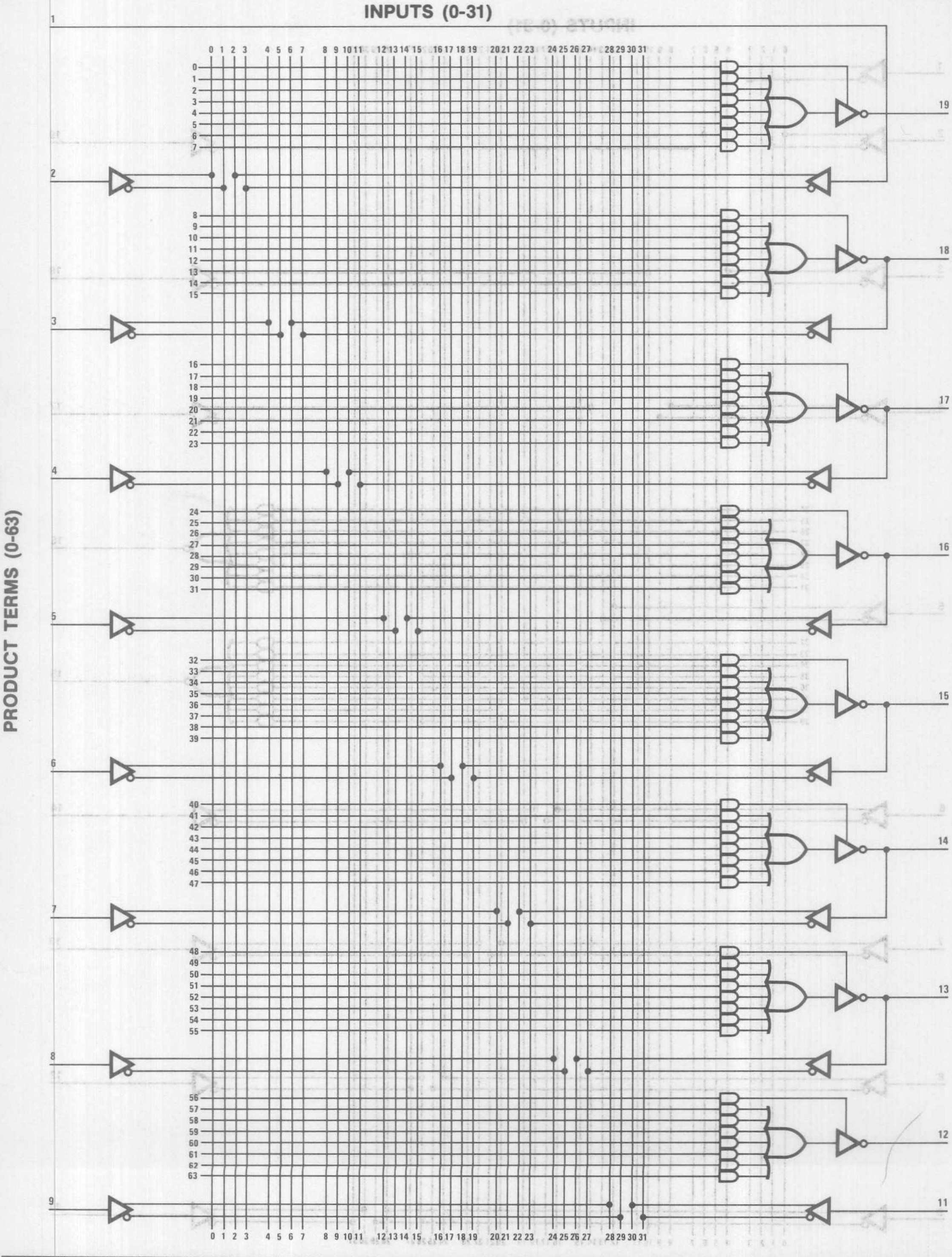
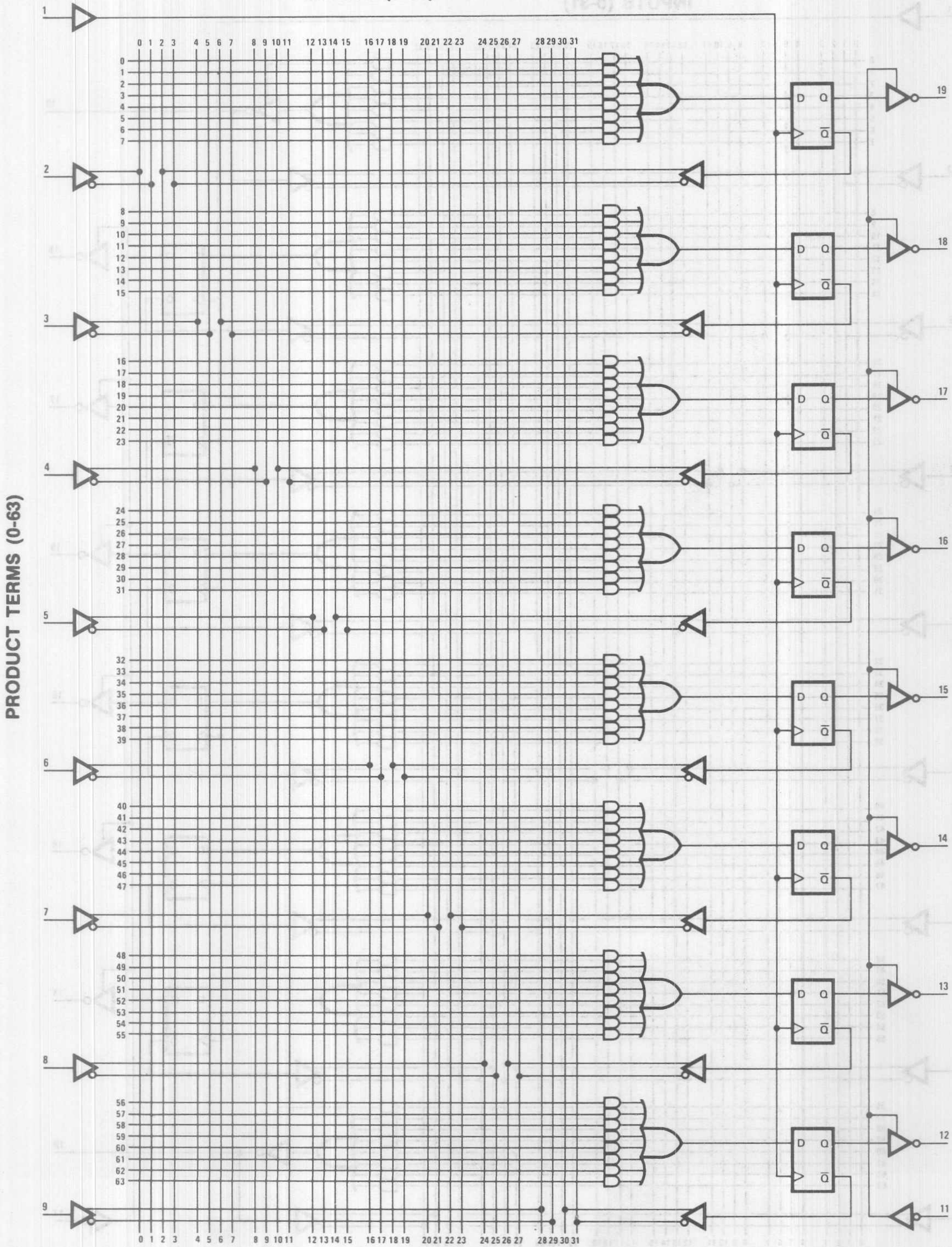
19

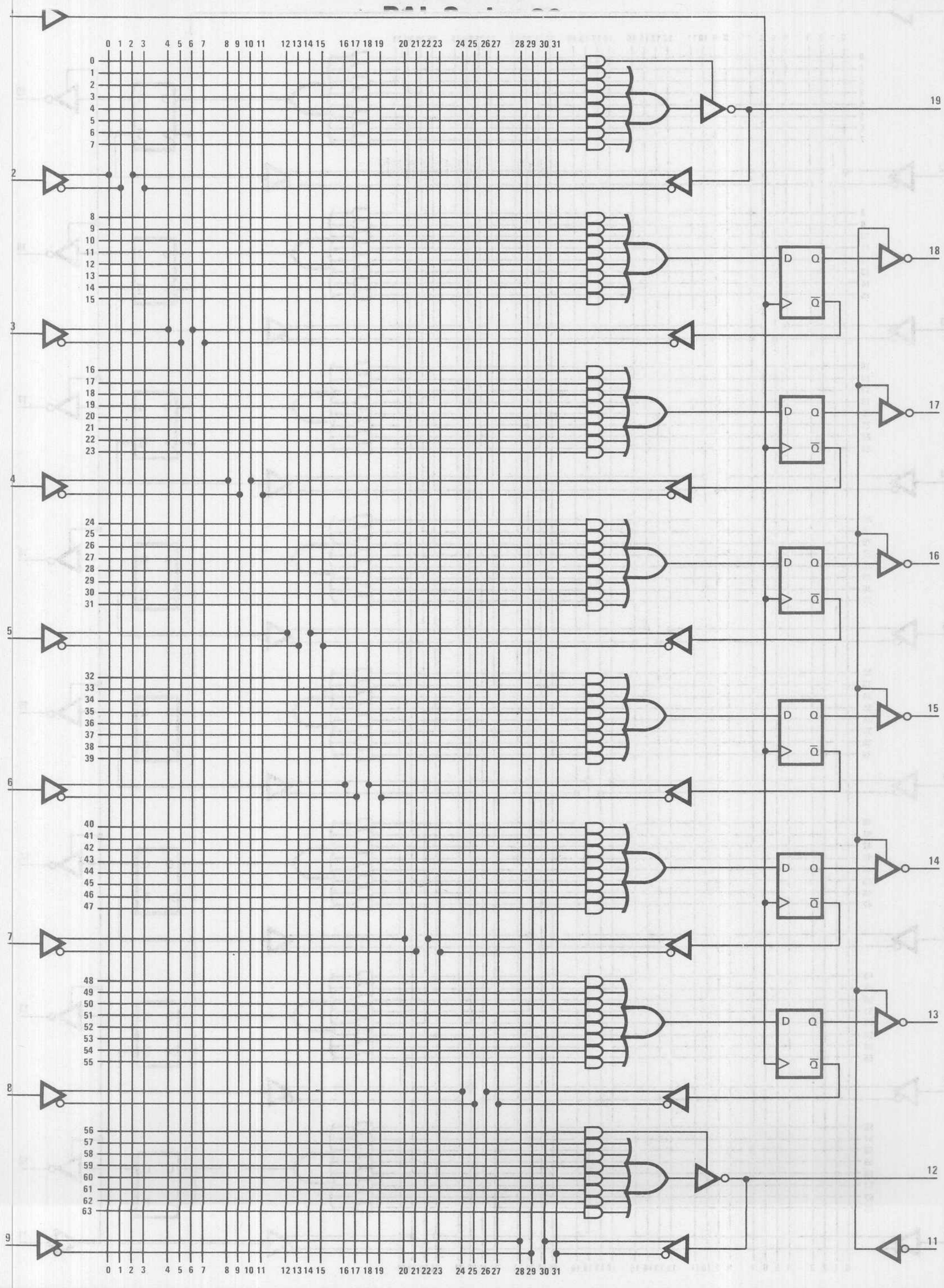
Logic Diagram PAL16L8



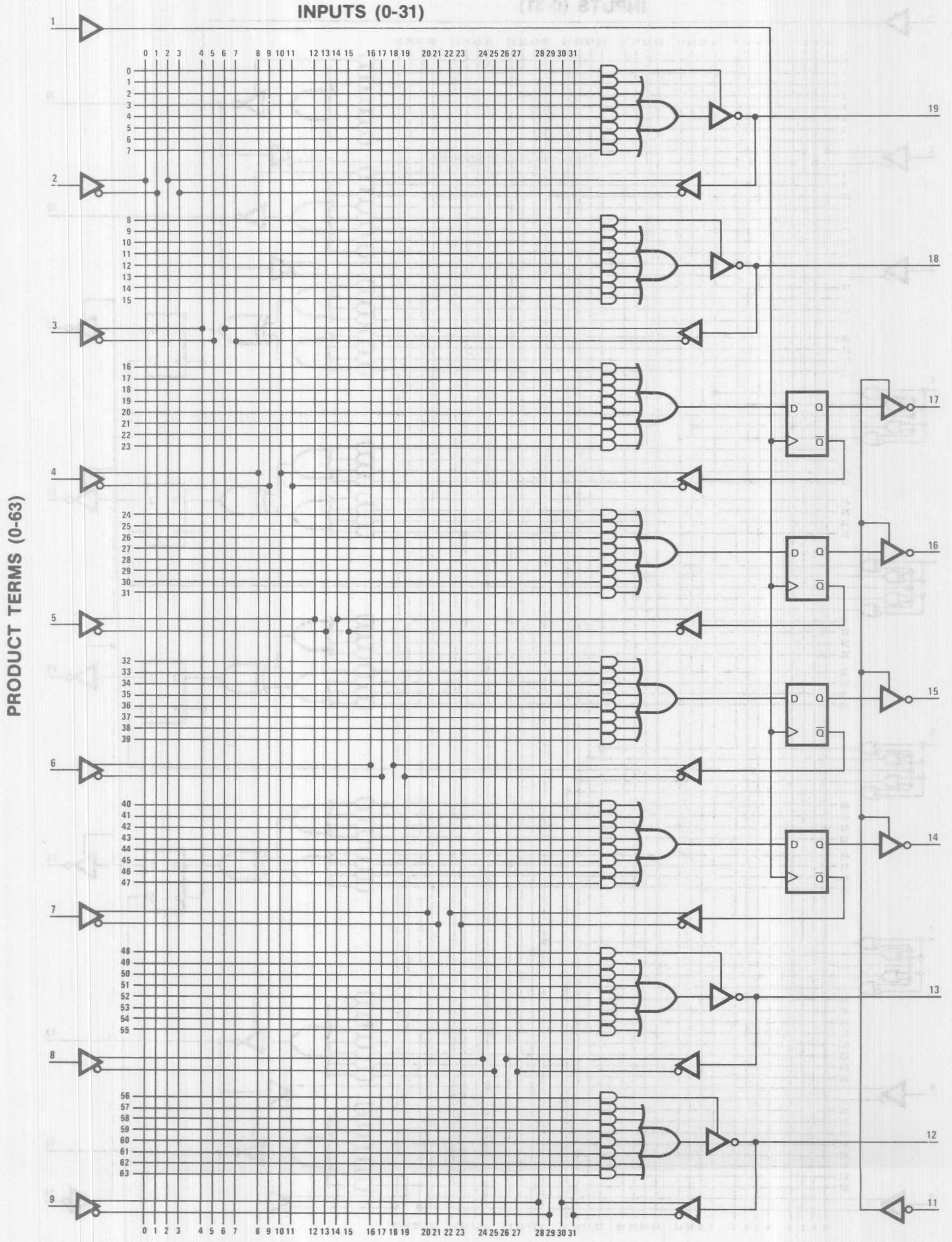
Logic Diagram PAL16R8



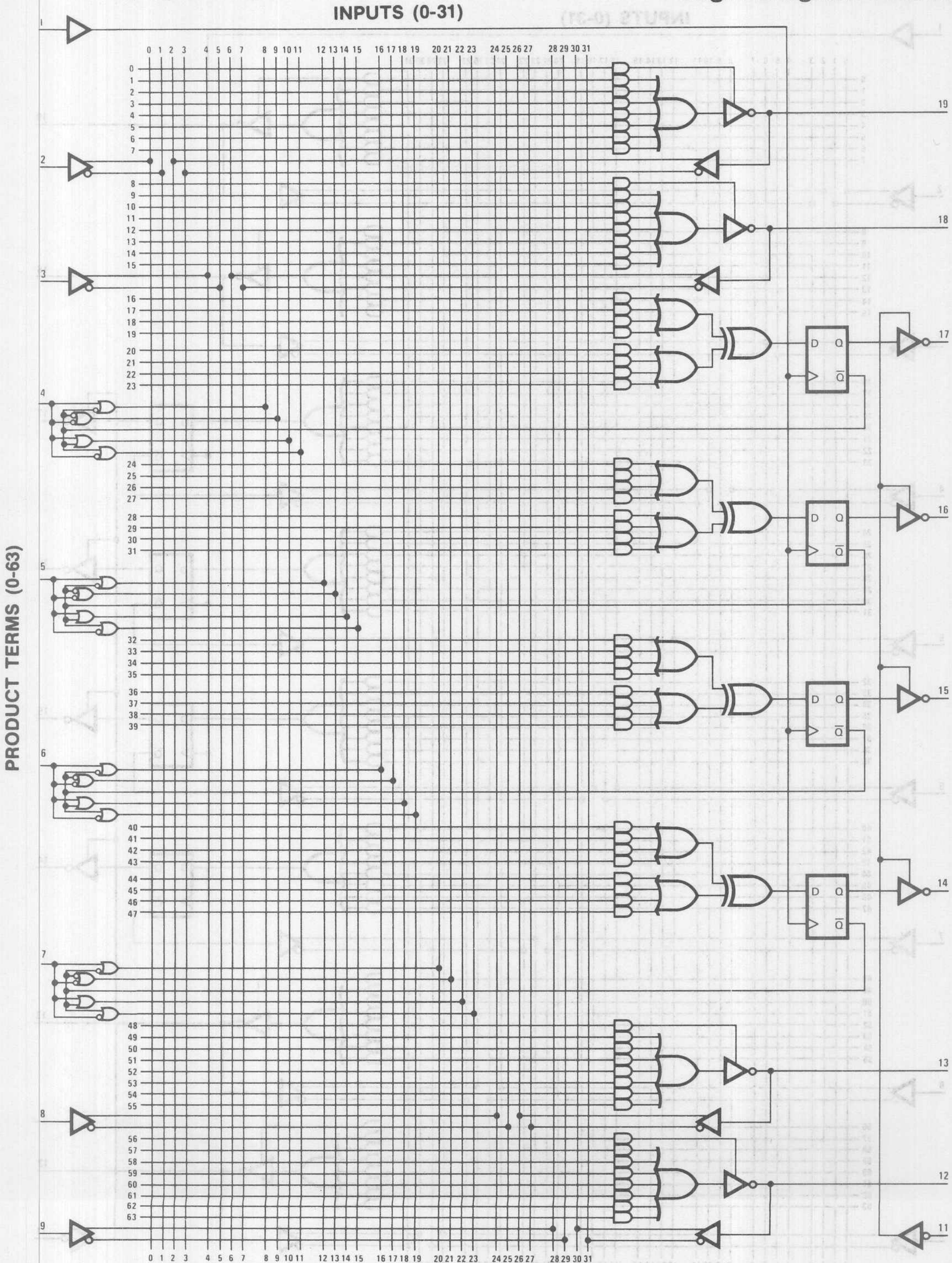
PRODUCT TERMS (0-63)



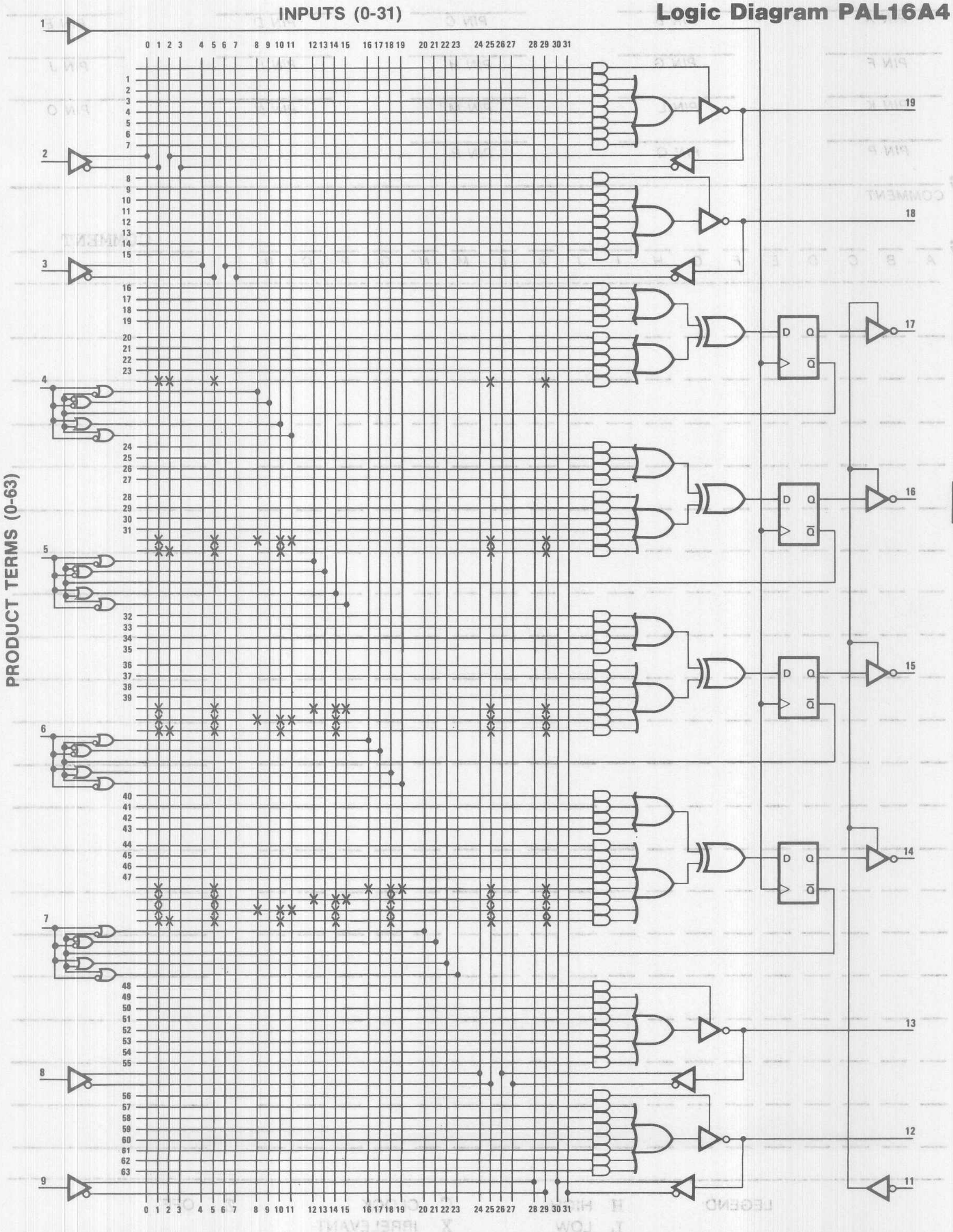
Logic Diagram PAL16R4



Logic Diagram PAL16X4



Logic Diagram PAL16A4



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PIN F | PIN G | PIN H | PIN I | PIN J

PIN K | PIN L | PIN M | PIN N | PIN O

PIN P | PIN Q | PIN R

; COMMENT

; A B C D E F G H I J K L M N O P Q R — COMMENT

LEGEND:

H HIGH C CLOCK Z OFF

L LOW X IRRELEVANT

TITLE

COMPANY, CITY, STATE

PIN 1	PIN 2	PIN 3	PIN 4	PIN 5 GND
PIN 6	PIN 7	PIN 8	PIN 9	PIN 10
PIN 11	PIN 12	PIN 13	PIN 14	PIN 15 VCC
PIN 16	PIN 17	PIN 18	PIN 19	PIN 20

EQUATIONS

Description

LEGEND: = EQUAL + OR :+: XOR / COMPLEMENT

:= REPLACED BY * AND :*: XNOR ( ) THREE-STATE

F 110

Programmable Array Logic Family

PAL® Series 24

U.S. Patent 4124899

Features/Benefits

- **Programmable replacement for conventional TTL logic.**
- **Reduces IC inventories substantially and simplifies their control.**
- **Reduces chip count by 5 to 1.**
- **Expedites and simplifies prototyping and board layout.**
- **Saves space with 24-pin SKINNYDIP™ packages.**
- **Programmed on standard PROM programmers.**
- **Programmable three-state outputs.**
- **Special feature reduces possibility of copying by competitors.**

PART NUMBER	PKG	DESCRIPTION
PAL12L10	J,N	Deca 12 Input And-Or-Invert Gate Array
PAL14L8	J,N	Octal 14 Input And-Or-Invert Gate Array
PAL16L6	J,N	Hex 16 Input And-Or-Invert Gate Array
PAL18L4	J,N	Quad 18 Input And-Or-Invert Gate Array
PAL20L2	J,N	Dual 20 Input And-Or-Invert Gate Array
PAL20C1	J,N	20 Input And-Or/And-Or Invert Gate Array
PAL20L10	J,N	Deca 20 Input And-Or-Invert Gate Array
PAL20X10	J,N	Deca 20 Input Registered And-Or-Xor Gate Array
PAL20X8	J,N	Octal 20 Input Registered And-Or-Xor Gate Array
PAL20X4	J,N	Quad 20 Input Registered And-Or-Xor Gate Array

Description

The PAL Series 24 family complements the PAL Series 20 family by providing two additional inputs and two additional outputs, allowing more complex functions in a single package. This new family is made feasible by the Monolithic Memories new and revolutionary 24-pin SKINNYDIP™.

In addition to providing more logic function per chip, 24 pins allows for many natural functions which were previously unavailable in skinny 300 mil-wide packages. Examples include:

- 8-bit parallel-in parallel-out counters
- 8-bit parallel-in parallel-out shift registers
- 16-Line-to-1-Line Multiplexors
- Dual 8-Line-to-1-Line Multiplexors
- Quad 4-Line-to-1-Line Multiplexors

These natural functions provide twice the density of traditional 16-pin packages.

The PAL family utilizes an advanced Schottky TTL process and the Bipolar PROM fusible link technology to provide user programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The family lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production.

The PAL transfer function is the familiar sum of products. Like the PROM, the PAL has a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array). In addition the PAL provides these options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops which are loaded on the low to high transition of the clock. PAL Logic Diagrams are shown with all fuses blown, enabling the designer use of the diagrams as coding sheets.

To design a PAL, the user writes the logic equations using PAL DESIGN SPECIFICATION standard format (F108). This specification may be submitted to Monolithic Memories where it is computer processed and assigned a bit pattern number, eg P0123. Monolithic Memories accepts the PAL DESIGN SPECIFICATION in one of the three forms:

1. Computer generated listings.
2. Typed or hand-written forms F107 and F108.
3. Direct on line data transmission to Monolithic Memories Timeshare computer system via telephone (local telephone network to major U.S. cities, London and Paris) or TWX online Boston TWX No.).

The entire PAL family is programmed on inexpensive conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

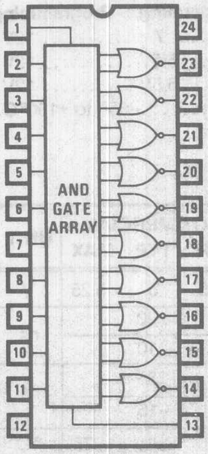
Ordering Information

PROGRAMMABLE ARRAY LOGIC FAMILY
NUMBER OF ARRAY INPUTS
OUTPUT TYPE
L = ACTIVE LOW
C = COMPLEMENTARY
X = EXCLUSIVE OR REGISTERED
R = REGISTERED
NUMBER OF OUTPUTS
TEMPERATURE RANGE
C = 0C TO +75C
M = -55C TO +125C
PACKAGE
N = PLASTIC DIP
J = CERAMIC DIP
HI-REL SCREENING LEVEL SEE "SCREENING OPTIONS

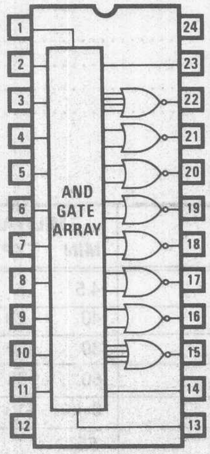
PAL20X8CJ 883B

SKINNYDIP is a registered trademark of Monolithic Memories

PAL12L10



PAL14L8



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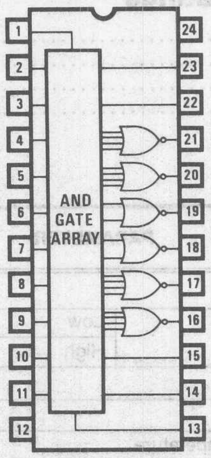
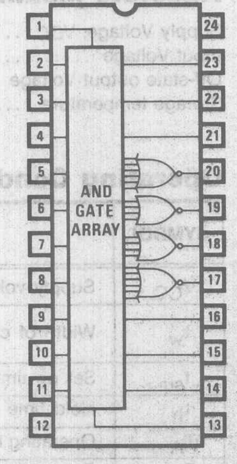
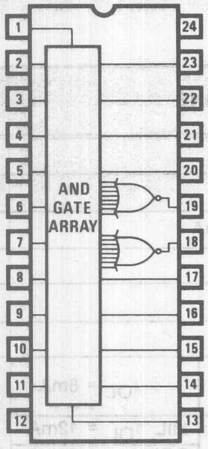


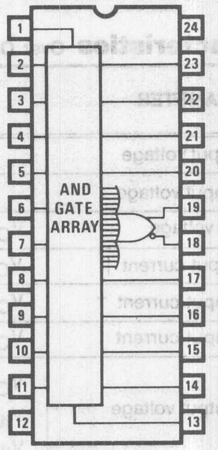
PAL18L4



PAL20L2



PAL20C1



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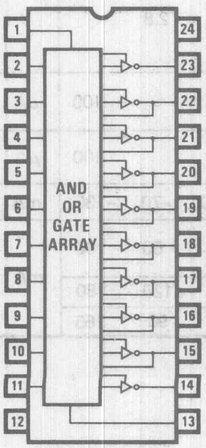
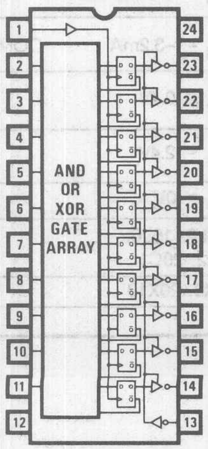
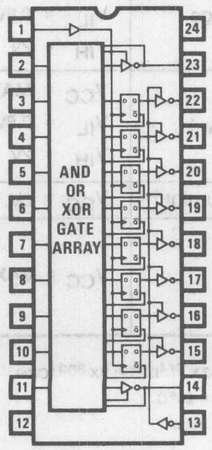
PAL20L10



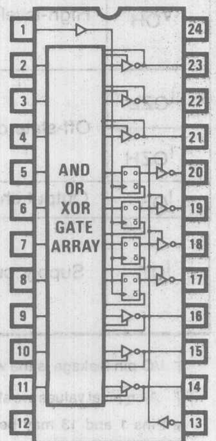
PAL20X10



PAL20X8



PAL20X4



Input Voltage .... 5.5V 12V*
Off-state output Voltage .... 5.5V 12V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	40	20		35	20		ns
		High	30	10		25	10		ns
t_{su}	Set up time		60	38		50	38		ns
t_h	Hold time		0	−15		0	−15		ns
T_A	Operating free air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP††	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−0.8	−1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX	V_I = 0.4V			−0.02	−0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	12L10, 14L8, 16L6, 18L4, 20L2, 20C1	I_{OL} = 8mA		0.3	0.5	V
			20L10, 20X10, 20X8, 20X4	MIL I_{OL} = 12mA				
				COM I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −2mA	MIL	2.4	2.8		V
			I_{OH} = −3.2mA	COM				
I_{OZL}	Off-state output current †	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.4V				−100	μA
I_{OZH}			V_O = 2.4V				100	μA
I_{OS}	Output short-circuit current **	V_{CC} = 5V	V_O = 0V		−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX	12L10, 14L8, 16L6, 18L4, 20L2, 20C1			60	100	mA
			20X4, 20X8, 20X10			120	180	mA
			20L10			90	165	mA

† I/O pin leakage is the worst case of I_{OZX} or I_{IX} e.g. I_{IX} and I_{OZH}

†† All typical values are at V_{CC} = 5V, T_A = 25°C.

* Pins 1 and 13 may be raised to 22V max.

** Only one output shorted at a time.

Switching Characteristics

Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input to output	12L10, 14L8, 16L6, 18L4, 20L2, 20C1	$R_1 = 560\Omega$ $R_2 = 1.1k\Omega$		25	45		25	40	ns
t_{PD}	Input or feedback to output		20L10, 20X10 20X8, 20X4 $R_1 = 200\Omega$ $R_2 = 390\Omega$		35	60		35	50	ns
t_{CLK}	Clock to output or feedback				20	35		20	30	ns
t_{PZX}	Pin 13 to output enable				20	45		20	35	ns
t_{PXZ}	Pin 13 to output disable				20	45		20	35	ns
t_{PZX}	Input to output enable				35	55		35	45	ns
t_{PXZ}	Input to output disable				35	55		35	45	ns
f_{MAX}	Maximum frequency			10.5	16		12.5	16		MHz

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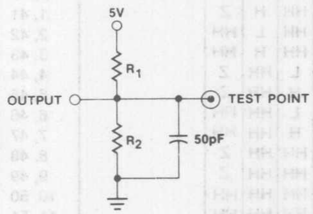
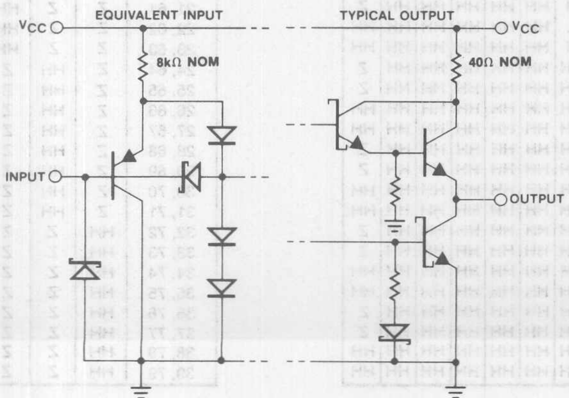
Test Load



Schematic of Inputs and Outputs



Programming

PAL fuses are programmed using a low-voltage linear-select procedure which is common to all PAL types. The array is divided into two groups, products 0 thru 39 and products 40 thru 79, for which pin identifications are shown in Pin Configurations below. To program a particular fuse, both an input line and a product line are selected according to the following procedure:

Step 1 Raise Output Disable, OD, to V_{IHH}.

Step 2 Select an input line by specifying I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7, I_8, I_9 and L/R as shown in Table 1.

Step 3 Select a product line by specifying A_0, A_1 and A_2 one-of-eight select as shown in Table 2.

Step 4 Raise V_{CC} (pin 24) to V_{IHH}.

Step 5 Program the fuse by pulsing the output pins, O, of the selected product group to V_{IHH} as shown in Programming Waveform.

Step 6 Lower V_{CC} (pin 24) to 6.0 V.

Step 7 Pulse the CLOCK pin and verify the output pin, O, to be Low for active Low PAL types or High for active High PAL types.

Step 8 Lower V_{CC} (pin 24) to 4.5 V and repeat step 7.

Step 9 Should the output not verify, repeat steps 1 thru 8 up to five (5) times.

This procedure is repeated for all fuses to be blown (see Programming Waveforms).

To prevent further verification, two last fuses may be blown by raising pin 1 and pin 13 to V_P. V_{CC} is not required during this operation.

Voltage Legend

L = Low-level input voltage, V_{IL}
H = High-level input voltage, V_{IH}
HH = High-level program voltage, V_{IHH}
Z = High impedance (e.g. 10K Ω to 5.0V)

INPUT LINE NUMBER	PIN IDENTIFICATION										
	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	L/R
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH
28	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	Z
29	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	Z
30	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	HH
31	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	HH
32	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	Z
33	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	Z
34	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	HH
35	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	HH
36	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
37	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
38	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH
39	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH

Table 1 Input Line Select

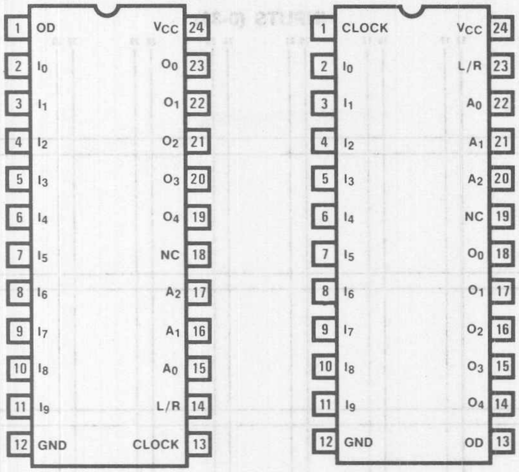
PRODUCT LINE NUMBER	PIN IDENTIFICATION							
	O_4	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0, 40	Z	Z	Z	Z	HH	Z	Z	Z
1, 41	Z	Z	Z	Z	HH	Z	Z	HH
2, 42	Z	Z	Z	Z	HH	Z	HH	Z
3, 43	Z	Z	Z	Z	HH	Z	HH	HH
4, 44	Z	Z	Z	Z	HH	HH	Z	Z
5, 45	Z	Z	Z	Z	HH	HH	Z	HH
6, 46	Z	Z	Z	Z	HH	HH	HH	Z
7, 47	Z	Z	Z	Z	HH	HH	HH	HH
8, 48	Z	Z	Z	HH	Z	Z	Z	Z
9, 49	Z	Z	Z	HH	Z	Z	Z	HH
10, 50	Z	Z	Z	HH	Z	Z	HH	Z
11, 51	Z	Z	Z	HH	Z	Z	HH	HH
12, 52	Z	Z	Z	HH	Z	HH	Z	Z
13, 53	Z	Z	Z	HH	Z	HH	Z	HH
14, 54	Z	Z	Z	HH	Z	HH	HH	Z
15, 55	Z	Z	Z	HH	Z	HH	HH	HH
16, 56	Z	Z	HH	Z	Z	Z	Z	Z
17, 57	Z	Z	HH	Z	Z	Z	Z	HH
18, 58	Z	Z	HH	Z	Z	Z	HH	Z
19, 59	Z	Z	HH	Z	Z	Z	HH	HH
20, 60	Z	Z	HH	Z	Z	HH	Z	Z
21, 61	Z	Z	HH	Z	Z	HH	Z	HH
22, 62	Z	Z	HH	Z	Z	HH	HH	Z
23, 63	Z	Z	HH	Z	Z	HH	HH	HH
24, 64	Z	HH	Z	Z	Z	Z	Z	Z
25, 65	Z	HH	Z	Z	Z	Z	Z	HH
26, 66	Z	HH	Z	Z	Z	Z	HH	Z
27, 67	Z	HH	Z	Z	Z	Z	HH	HH
28, 68	Z	HH	Z	Z	Z	HH	Z	Z
29, 69	Z	HH	Z	Z	Z	HH	Z	HH
30, 70	Z	HH	Z	Z	Z	HH	HH	Z
31, 71	Z	HH	Z	Z	Z	HH	HH	HH
32, 72	HH	Z	Z	Z	Z	Z	Z	Z
33, 73	HH	Z	Z	Z	Z	Z	Z	HH
34, 74	HH	Z	Z	Z	Z	Z	HH	Z
35, 75	HH	Z	Z	Z	Z	Z	HH	HH
36, 76	HH	Z	Z	Z	Z	HH	Z	Z
37, 77	HH	Z	Z	Z	Z	HH	Z	HH
38, 78	HH	Z	Z	Z	Z	HH	HH	Z
39, 79	HH	Z	Z	Z	Z	HH	HH	HH

Table 2 Product Line Select

Pin Configurations

PRODUCTS 0 THRU 39

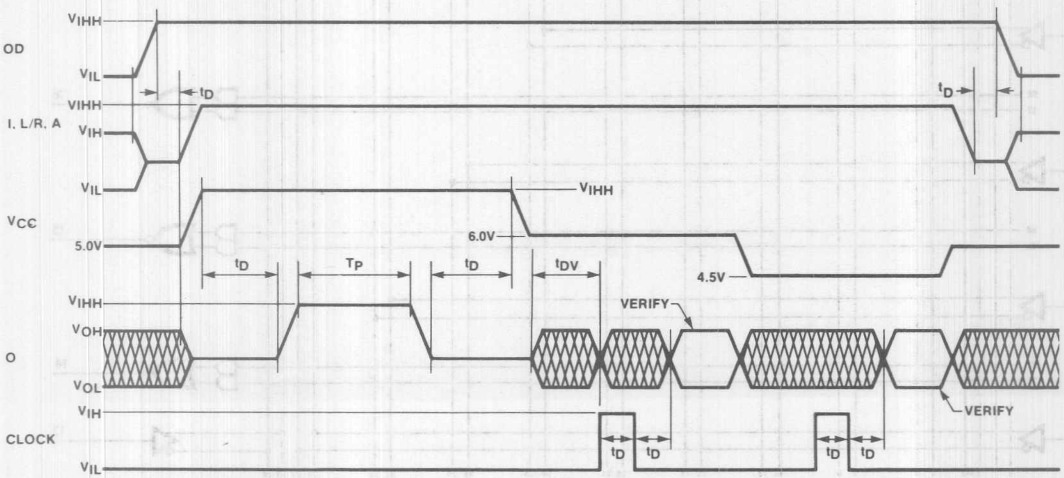
PRODUCTS 40 THRU 79

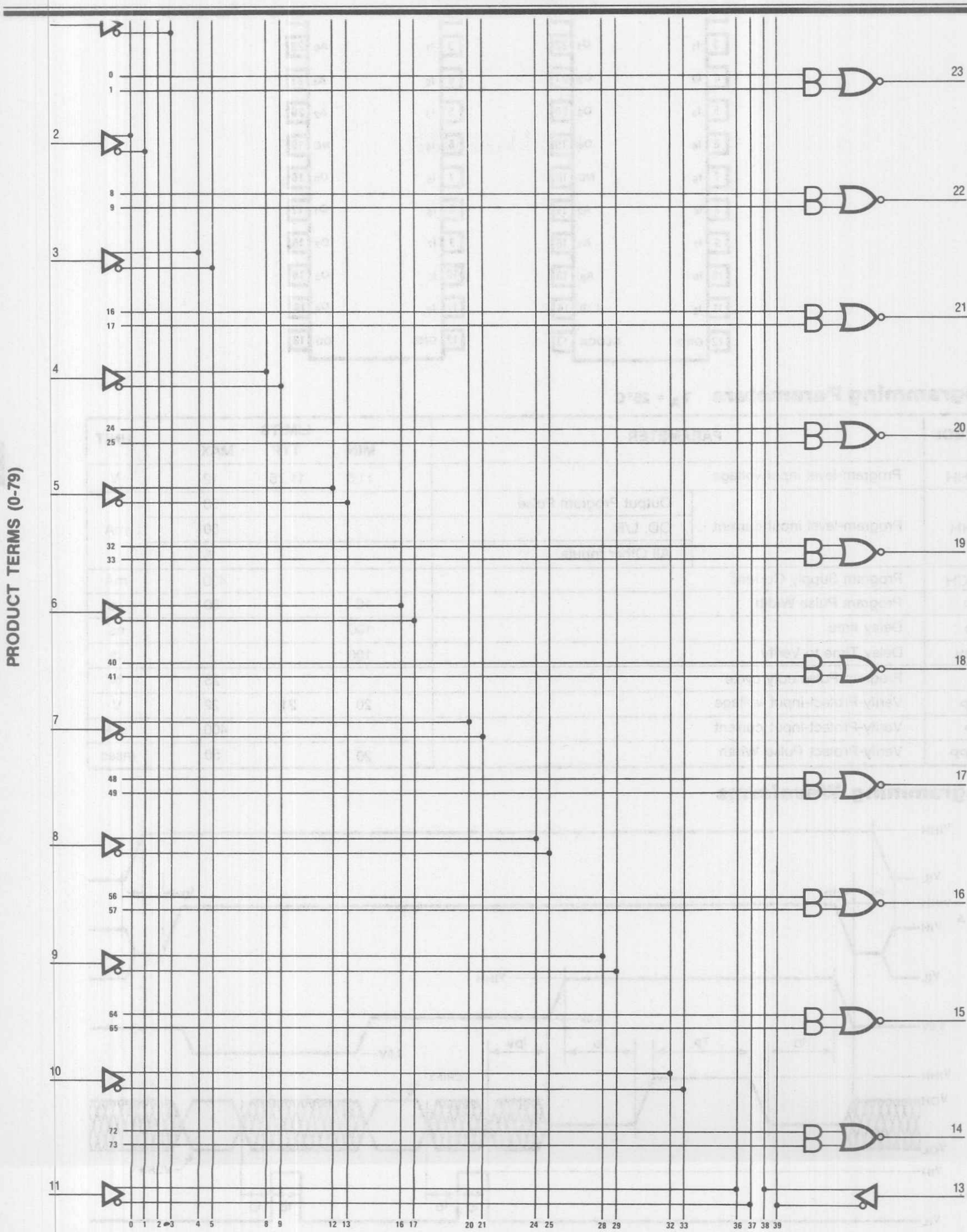


Programming Parameters $T_A = 25°C$

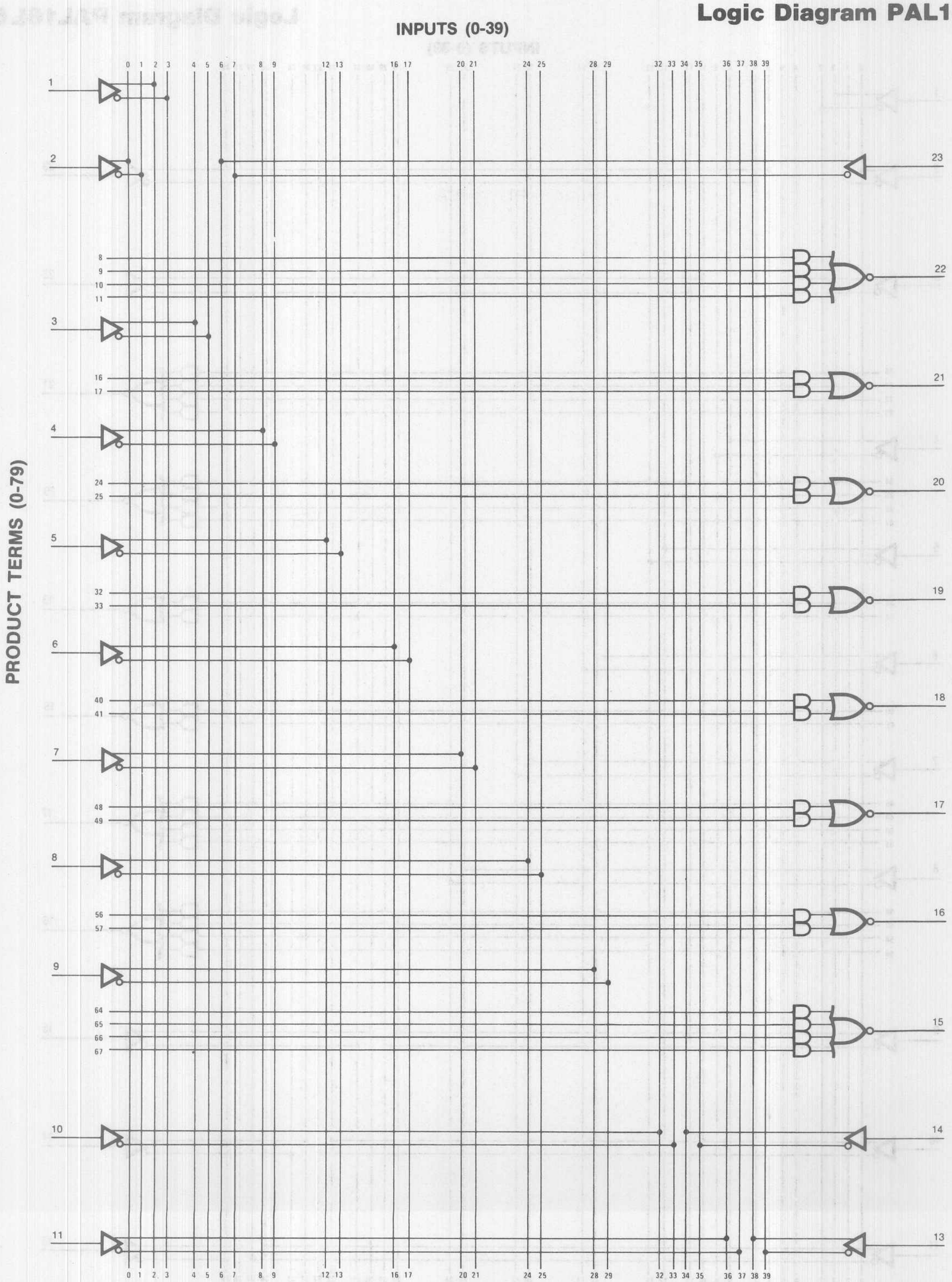
SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNIT
V_{IHH}	Program-level input voltage		11.5	11.75	12	V
I_{IHH}	Program-level input current	Output Program Pulse			50	mA
		OD, L/R			50	
		All Other Inputs			5	
I_{CCH}	Program Supply Current				400	mA
T_P	Program Pulse Width		10		50	μs
t_D	Delay time		100			ns
t_{DV}	Delay Time to Verify		100			μs
	Program Pulse duty cycle				25	%
V_P	Verify-Protect-input voltage		20	21	22	V
I_P	Verify-Protect-input current				400	mA
T_{PP}	Verify-Protect Pulse Width		20		50	msec

Programming Waveforms

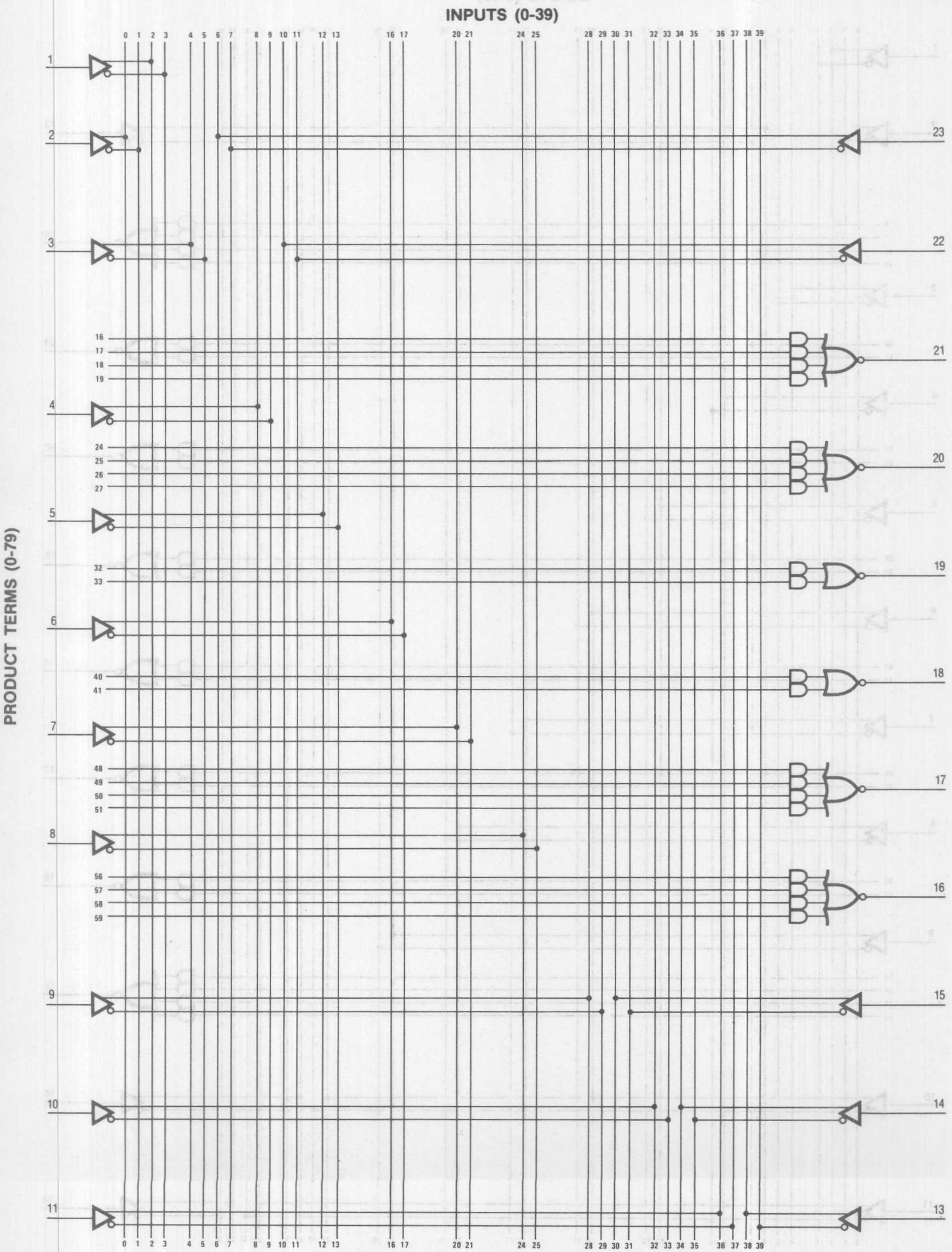



PRODUCT TERMS (0-79)
2
3
4
5
6
7
8
9
10
11
0
1
8
9
16
17
24
25
32
33
40
41
48
49
56
57
64
65
72
73
23
22
21
20
19
18
17
16
15
14
13
0 1 2 3 4 5 8 9 12 13 16 17 20 21 24 25 28 29 32 33 36 37 38 39

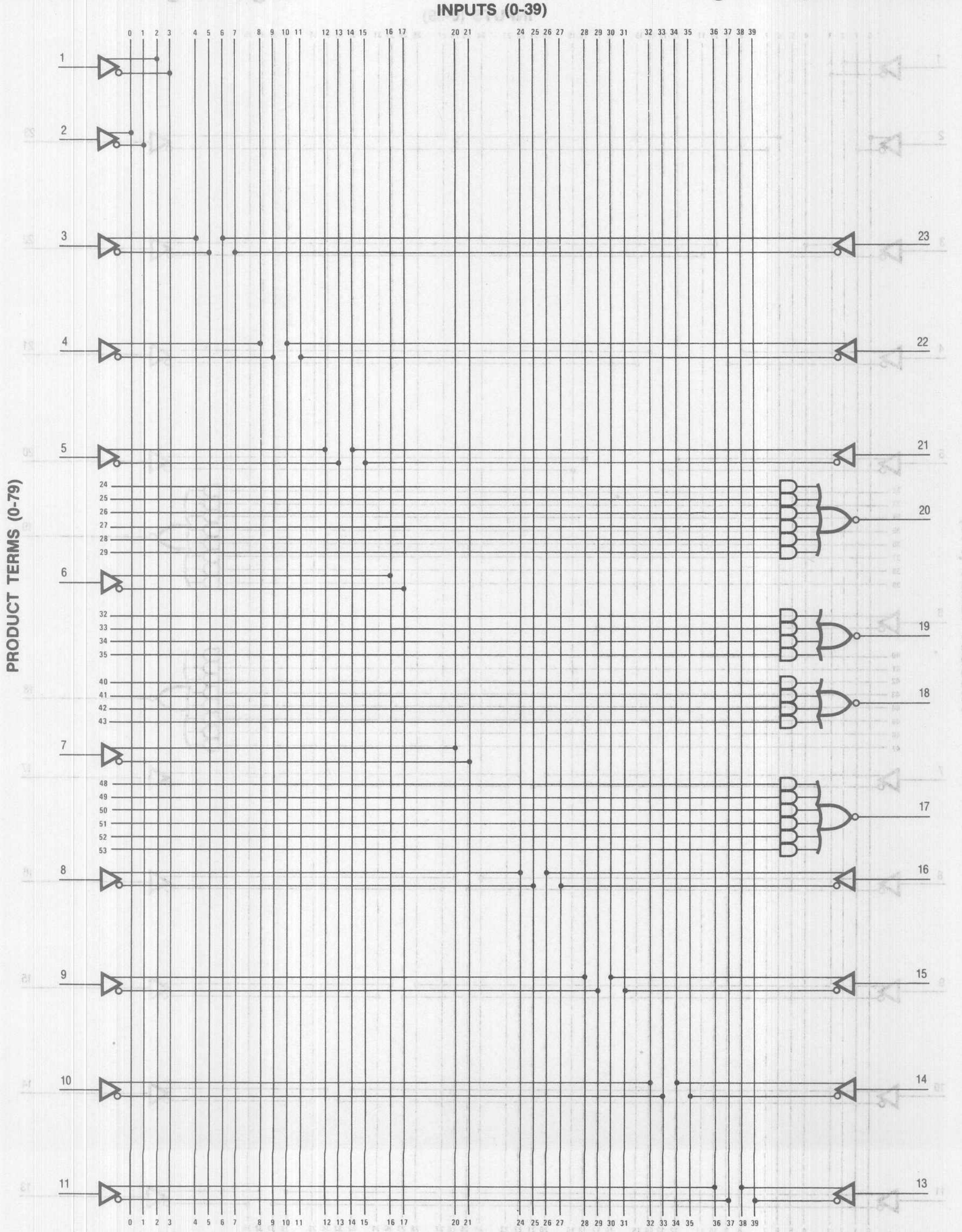
Logic Diagram PAL14L8

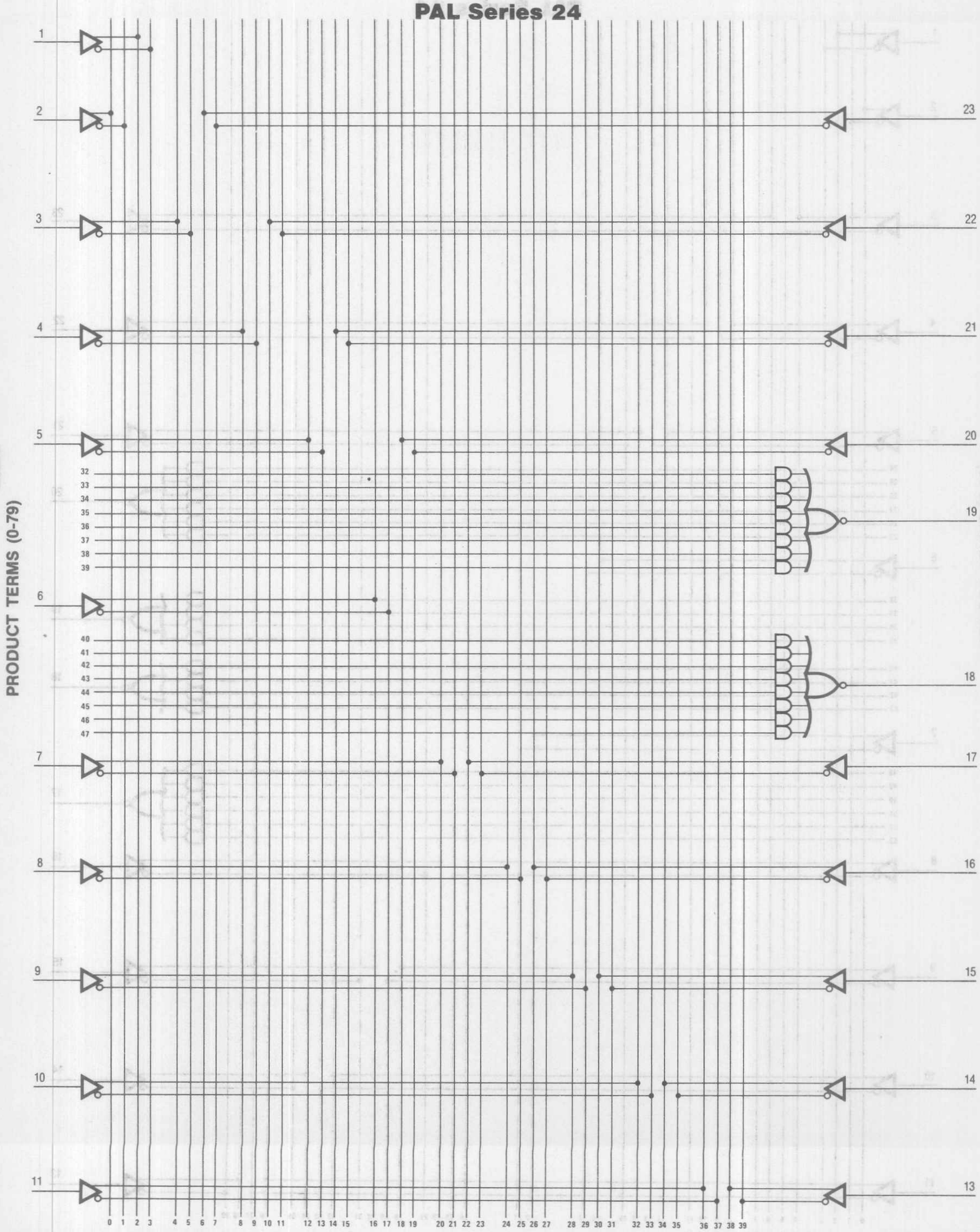


Logic Diagram PAL16L6

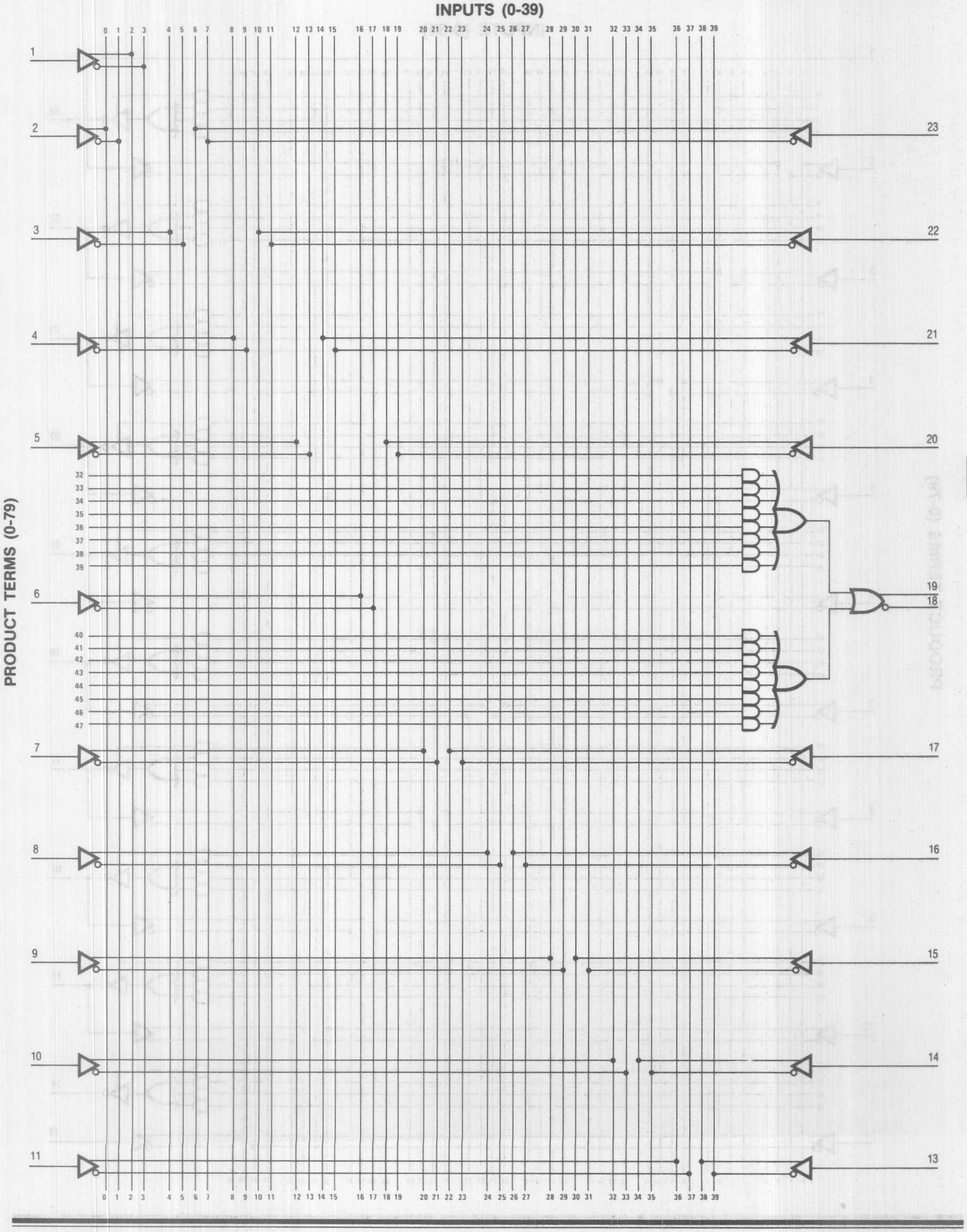


Logic Diagram PAL18L4

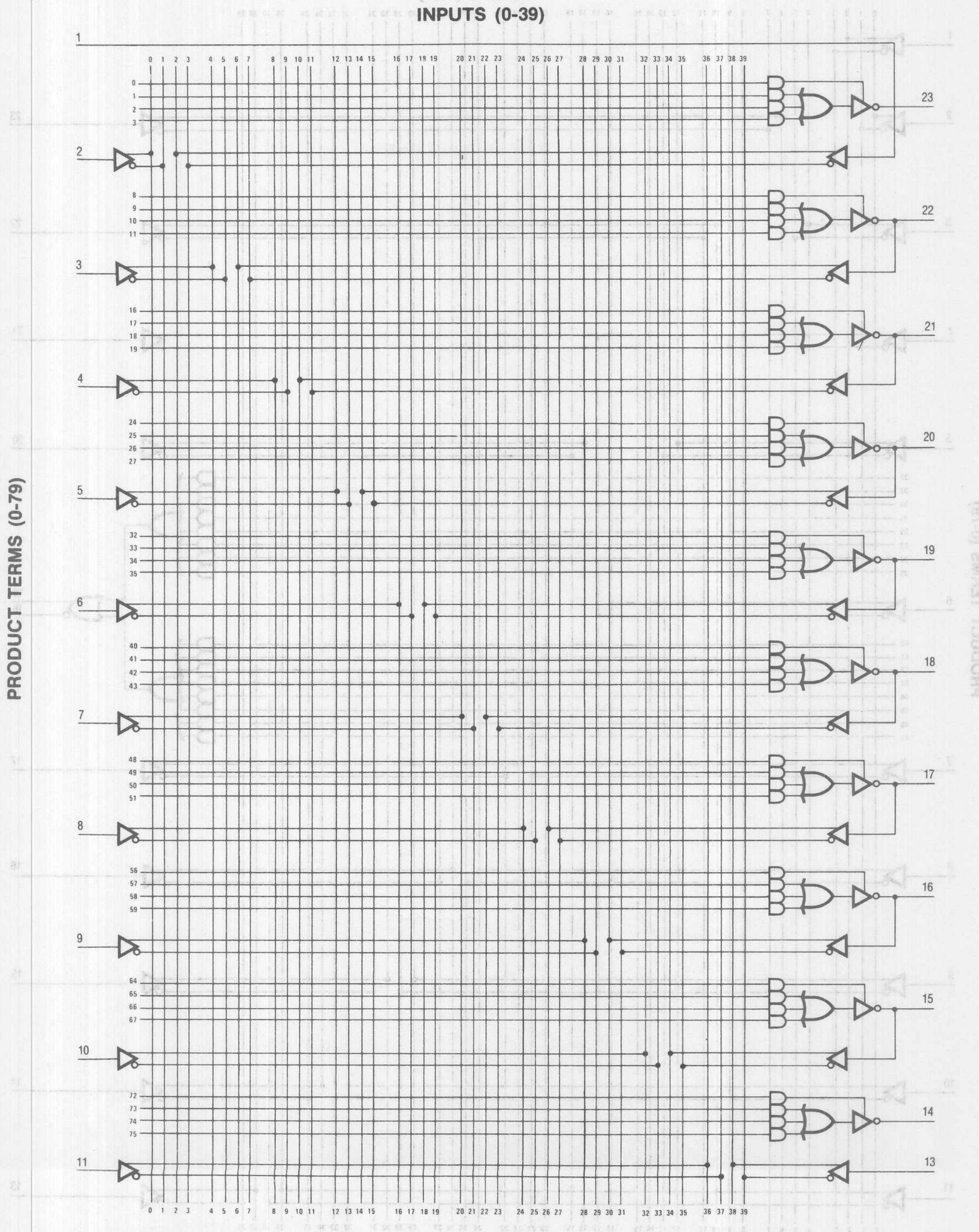



PRODUCT TERMS (0-79)
1
2
3
4
5
6
7
8
9
10
11
23
22
21
20
19
18
17
16
15
14
13
32 33 34 35 36 37 38 39
40 41 42 43 44 45 46 47
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39

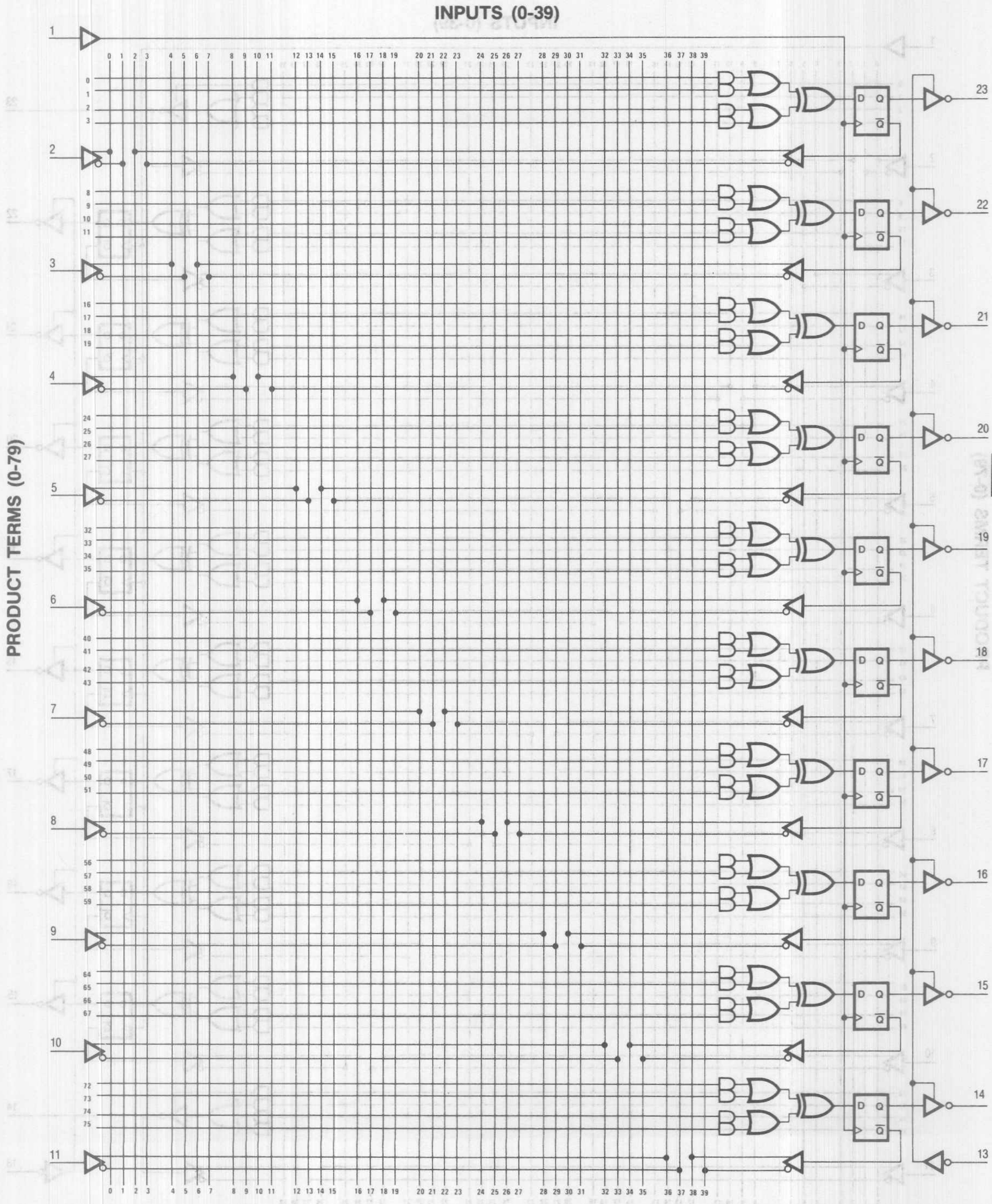
Logic Diagram PAL20C1



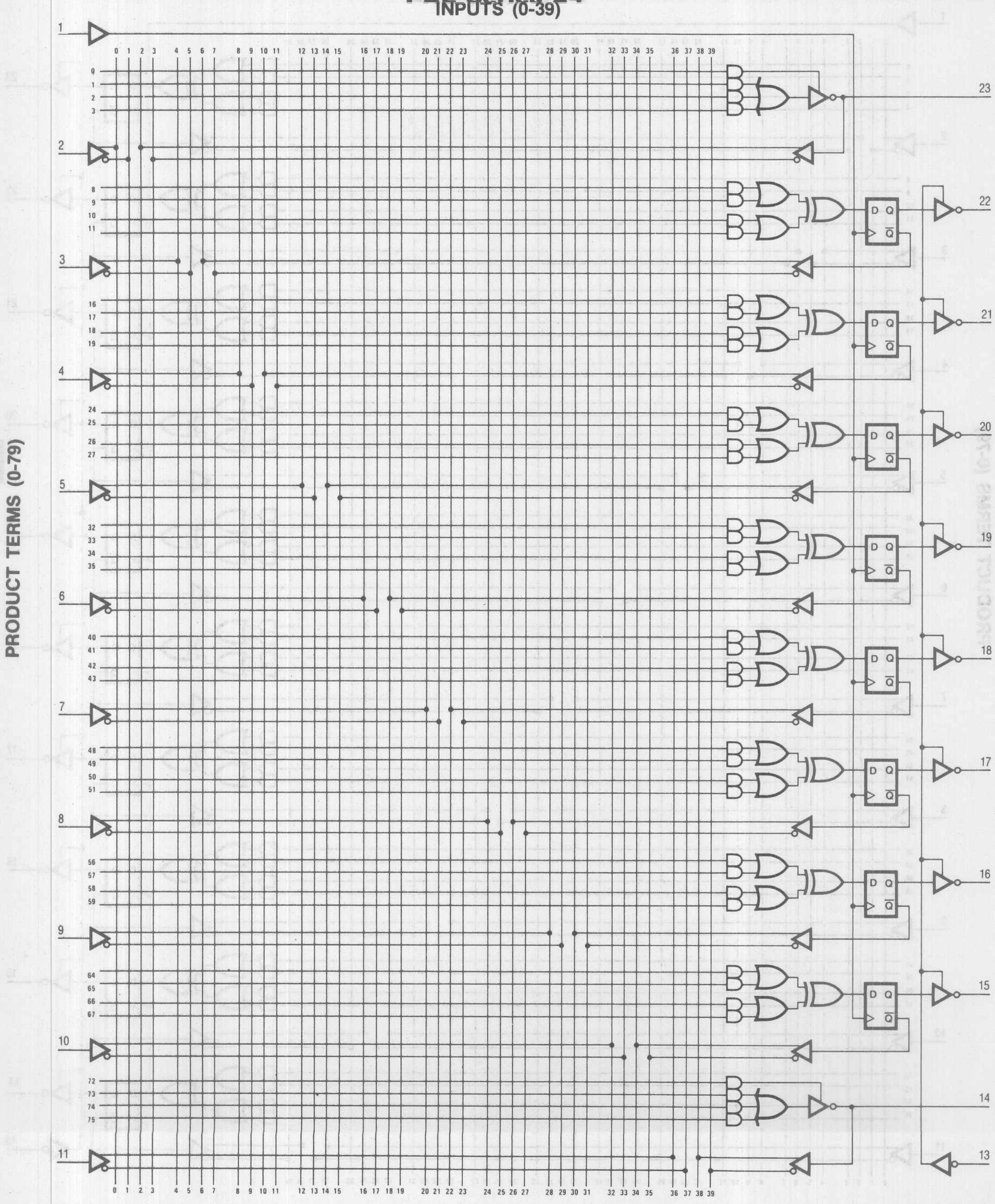
Logic Diagram PAL20L10



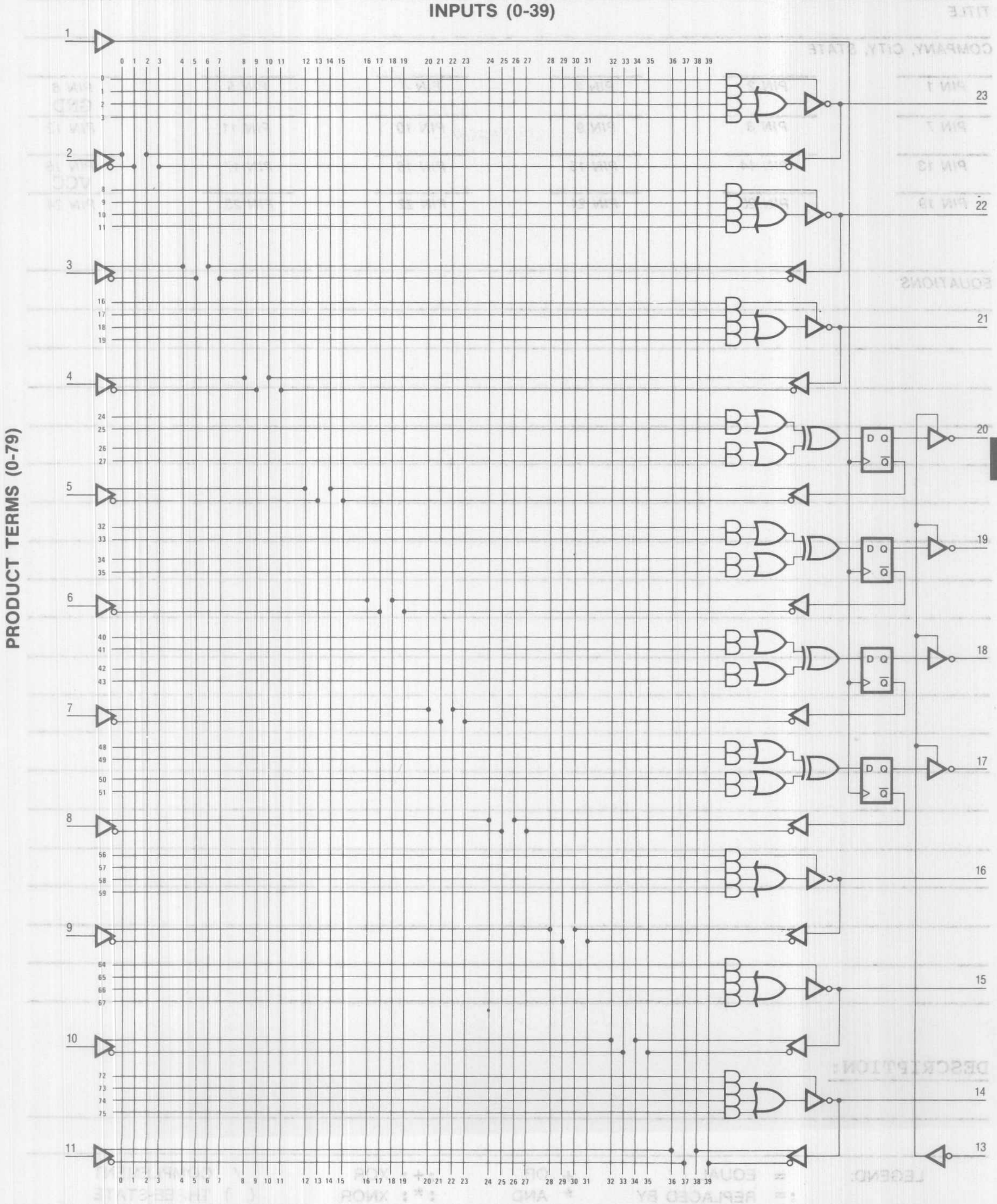
Logic Diagram PAL20X10



PAL Series 24



Logic Diagram PAL20X4



PAL

PAL DESIGN SPECIFICATION

PART NUMBER

USER'S PART NUMBER REV NAME / / DATE

TITLE

COMPANY, CITY, STATE

PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	GND PIN 6
PIN 7	PIN 8	PIN 9	PIN 10	PIN 11	PIN 12
PIN 13	PIN 14	PIN 15	PIN 16	PIN 17	VCC PIN 18
PIN 19	PIN 20	PIN 21	PIN 22	PIN 23	PIN 24

EQUATIONS

DESCRIPTION:

LEGEND: = EQUAL + OR :+: XOR / COMPLEMENT

:= REPLACED BY * AND :*: XNOR ( ) THREE-STATE

F 108

FUNCTION TABLE

PIN A　PIN B　PIN C　PIN D　PIN E　PIN F

PIN G　PIN H　PIN I　PIN J　PIN K　PIN L

PIN M　PIN N　PIN O　PIN P　PIN Q　PIN R

PIN S　PIN T　PIN U　PIN V

;
COMMENT

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	COMMENT

LEGEND: H HIGH　C CLOCK　Z OFF
L LOW　X IRRELEVANT

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Notes

Hard Array Logic Family

HAL Series 20 Data Sheet

Features/Benefits

- Gate array equivalent of up to 200 gates.
- Semi-custom solution
- Reduces SSI/MSI chip count greater than 4 to 1.
- Prototype using field-programmable version — PAL.
- Cost savings up to 40% compared to PAL.
- Security link disabled for design secrecy.
- Test and simulation made simple with PALASM Function Table.
- Saves space with 20-pin SKINNYDIP™ packages.
- Power consumption is directly proportional to logic complexity.

Description

The HAL family utilizes standard Low-Power Schottky TTL process and automated mask pattern generation directly from logic equations to provide a semi-custom gate array for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The family lets the systems engineer "design his own chip" by AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production.

The HAL transfer function is the familiar sum of products. Like the ROM, the HAL has a single array of selectable gates. Unlike the ROM, the HAL is a selectable AND array driving a fixed OR array (the ROM is a fixed AND array driving a selectable OR array). In addition the HAL provides these options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback
- Arithmetic capability

Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops which are loaded on the low-to-high transition of the clock. HAL Logic Diagrams are shown with all fuses blown, enabling the designer to use the diagrams as coding sheets.

To design a HAL, the user first programs and debugs a PAL using PALASM and the "PAL DESIGN SPECIFICATION" standard format. This specification is submitted to Monolithic Memories where it is computer processed and assigned a bit pattern number, e.g. P01234.

PART NUMBER	PKG	DESCRIPTION
HAL10H8	J,N,F	Octal 10 Input And-Or Gate Array
HAL12H6	J,N,F	Hex 12 Input And-Or Gate Array
HAL14H4	J,N,F	Quad 14 Input And-Or Gate Array
HAL16H2	J,N,F	Dual 16 Input And-Or Gate Array
HAL16C1	J,N,F	16 Input And-Or/And-Or-Invert Gate Array
HAL10L8	J,N,F	Octal 10 Input And-Or-Invert Gate Array
HAL12L6	J,N,F	Hex 12 Input And-Or-Invert Gate Array
HAL14L4	J,N,F	Quad 14 Input And-Or-Invert Gate Array
HAL16L2	J,N,F	Dual 16 Input And-Or-Invert Gate Array
HAL16L8	J,N,F	Octal 16 Input And-Or-Invert Gate Array
HAL16R8	J,N,F	Octal 16 Input Registered And-Or Gate Array
HAL16R6	J,N,F	Hex 16 Input Registered And-Or Gate Array
HAL16R4	J,N,F	Quad 16 Input Registered And-Or Gate Array
HAL16X4	J,N,F	Quad 16 Input Registered And-Or-Xor Gate Array
HAL16A4	J,N,F	Quad 16 Input Registered And-Carry-Or-Xor Gate

Monolithic Memories accepts the PAL DESIGN SPECIFICATION in one of three forms:

1. Computer generated listing.
2. Typed or hand-written forms F109 and F110. See example on pages 6-7 and forms on pages 23-24.
3. Direct online data transmission to Monolithic Memories Timeshare computer system via telephone (local telephone network to major US cities, London and Paris) or TWX (online Boston TWX no.).

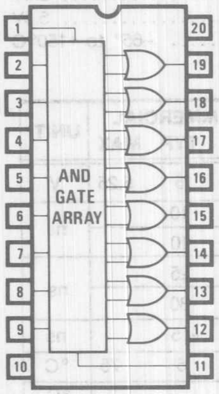
Monolithic Memories will provide a PAL sample for customer qualification. The user then submits a purchase order for a HAL of the specified bit pattern number, e.g. HAL14L4 P01234. See Ordering Information below.

Ordering Information

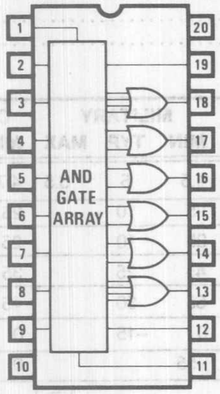
HARD ARRAY LOGIC FAMILY
NUMBER OF ARRAY INPUTS
OUTPUT YPE
H = ACTIVE HIGH
L = ACTIVE LOW
C = COMPLEMENTARY
R = REGISTERED
X = EXCLUSIVE-OR REGISTERED
A = ARITHMETIC REGISTERED
NUMBER OF OUTPUTS
TEMPERATURE RANGE
C = 0C TO +75C
M = -55C TO +125C
PACKAGE
N = PLASTIC DIP
J = CERAMIC DIP
F = FLAT PACK
OPTIONAL HI-REL PROCESSING
883 = MIL-STD-883, METHOD 5004 & 5005 LEVEL B
883C = MIL-STD-883, METHOD 5004 & 5005 LEVEL C
B = MIL-STD-883, METHOD 5004 EQUIVALENT
C = MIL-STD-883, METHOD 5004 EQUIVALENT
BIT PATTERN NUMBER

HAL14 L4 CJ 883B P01234

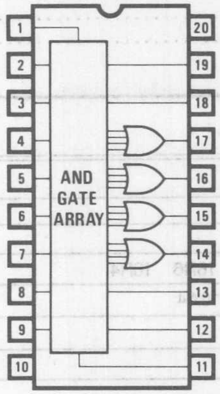
HAL10H8



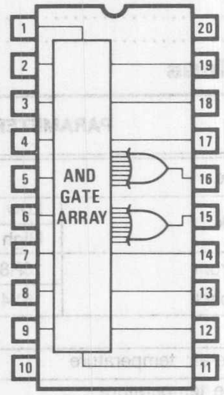
HAL12H6



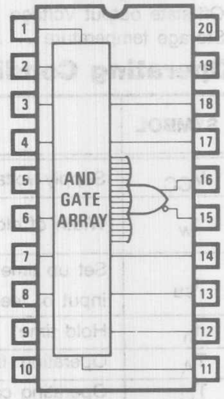
HAL14H4



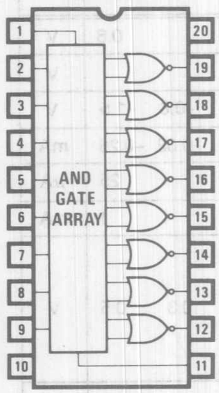
HAL16H2



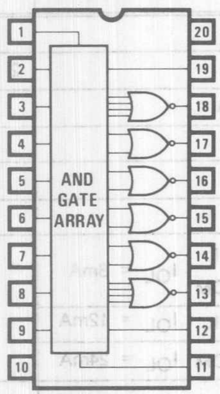
HAL16C1



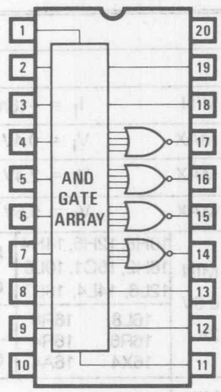
HAL10L8



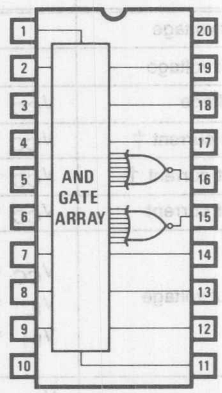
HAL12L6



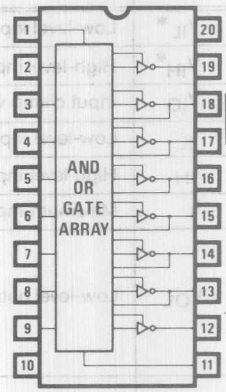
HAL14L4



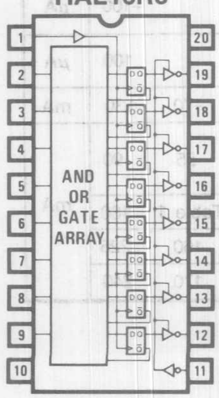
HAL16L2



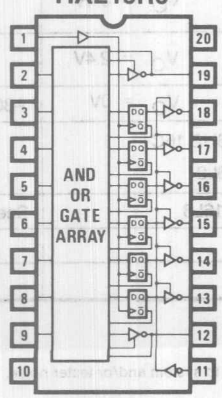
HAL16L8



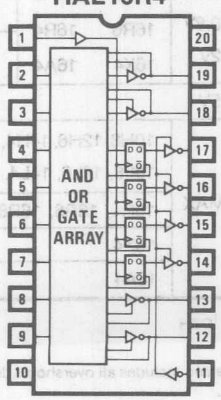
HAL16R8



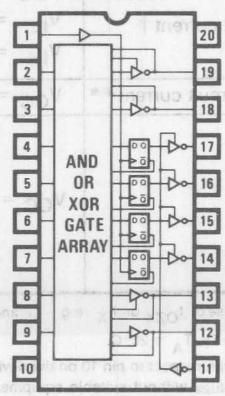
HAL16R6



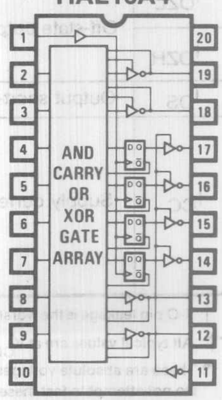
HAL16R4



HAL16X4



HAL16A4



Storage temperature .... –65 to +150 °C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	25	10		25	10		ns
		High	25	10		25	10		
t_{su}	Set up time from input or feedback	16R8 16R6 16R4	45	25		35	25		ns
		16X4 16A4	55	30		45	30		
t_h	Hold time		0	–15		0	–15		ns
T_A	Operating free-air temperature		–55			0	5	75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP ††	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = –18mA		–0.8	–1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX		V_I = 0.4V		–0.02	–0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	10H8, 12H6, 14H4, 16H2, 16C1, 10L8, 12L6, 14L4, 16L2	MIL / COM: I_{OL} = 8mA		0.3	0.5	V
			16L8 16R8 16R6 16R4 16X4 16A4	MIL: I_{OL} = 12mA				
				COM: I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OH} = –2mA	2.4	2.8		V
			COM	I_{OH} = –3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	16L8 16R8 16R6 16R4 16X4 16A4	V_O = 0.4V			–100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current **	V_{CC} = 5V		V_O = 0V	–30	–70	–130	mA
I_{CC}	Supply current	V_{CC} = MAX	10H8, 12H6, 14H4, 16H2, 16C1, 10L8, 12L6, 14L4, 16L2			55	90	mA
			16R4, 16R6, 16R8, 16L8			See Table 1	180	
			16X4			160	225	
			16A4			170	240	

† I/O pin leakage is the worst case of I_{OZX} or I_{IX} e.g., I_{IL} and I_{OZH}

†† *All typical values are at V_{CC} = 5V, T_A = 25°C.*

* These are absolute voltages with respect to pin 10 on the device and includes all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

** Only one output shorted at a time.

Switching Characteristics

Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input to output	10H8 12H6 14H4 16H2 10L8 12L6 14L4 16L2	$R_1 = 560\Omega$ $R_2 = 1.1k\Omega$		25	45		25	35	ns
		16C1			25	45		25	40	
t_{PD}	Input or feed-back to output	16R6 16R4 16L8	$R_1 = 200\Omega$ $R_2 = 390\Omega$		25	45		25	35	ns
		16X4 16A4			30	45		30	40	
t_{CLK}	Clock to output or feedback				15	25		15	25	ns
t_{PZY}	Pin 11 to output enable				15	25		15	25	ns
t_{PXZ}	Pin 11 to output disable				15	25		15	25	ns
t_{PZX}	Input to output enable	16R6 16R4 16L8			25	45		25	35	ns
		16X4 16A4			30	45		30	40	
t_{PXZ}	Input to output disable	16R6 16R4 16L8			25	45		25	35	ns
		16X4 16A4			30	45		30	40	
f_{MAX}	Maximum frequency	16R8 16R6 16R4		14	25		16	25		MHz
		16X4 16A4		12	22		14	22		

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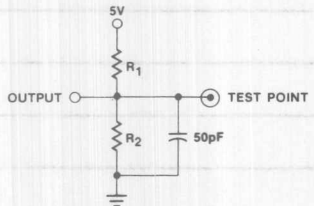
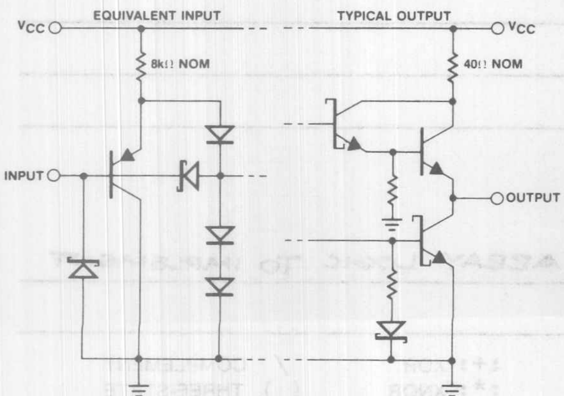
Test Load



Schematic of Inputs and Outputs



NUMBER OF PRODUCT TERMS	HAL16L8, 16R4 16R6, 16R8	HAL16X4	HAL16A4
0	99	97	108
1-4	101	101	113
5-8	104	106	117
9-12	106	110	122
13-16	108	115	126
17-20	110	119	131
21-24	113	124	135
25-28	115	128	140
29-32	117	133	144
33-36	119	137	149
37-40	122	142	153
41-44	124	146	158
45-48	126	151	162
49-52	128	155	167
53-56	131	160	171
57-60	133	164	176
61-64	135	169	180

Table 1. Typical I_{CC} vs. Number of Products Used

HAL 1246 | HAL DESIGN SPECIFICATION
PART NUMBER

PN 1234	A	KAZMI	2/6/81
USER'S PART NUMBER	REV	NAME	DATE

BASIC GATES EXAMPLE
TITLE
MONOLITHIC MEMORIES, CALIFORNIA
COMPANY, CITY, STATE

C	D	F	G	M
PIN 1	PIN 2	PIN 3	PIN 4	PIN 5
N	P	Q	I	GND
PIN 6	PIN 7	PIN 8	PIN 9	PIN 10
J	K	L	R	O
PIN 11	PIN 12	PIN 13	PIN 14	PIN 15
H	E	B	A	VCC
PIN 16	PIN 17	PIN 18	PIN 19	PIN 20

EQUATIONS

```
B = /A                   ; INVERTER
E = C * D                ; AND GATE
H = F + G                ; OR GATE
L = /I + /J + /K         ; NAND GATE
O = /M * /N              ; NOR GATE
R = P * /Q + /P * Q      ; XOR GATE
```

DESCRIPTION

THIS EXAMPLE ILLUSTRATES ARRAY LOGIC TO IMPLEMENT BASIC GATES.

LEGEND:	= EQUAL	+ OR	:+: XOR	/ COMPLEMENT
	:= REPLACED BY	* AND	:*: XNOR	( ) THREE-STATE

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FUNCTION TABLE

A	B	C	D	E
PIN A	PIN B	PIN C	PIN D	PIN E
F	G	H	I	J
PIN F	PIN G	PIN H	PIN I	PIN J
K	L	M	N	O
PIN K	PIN L	PIN M	PIN N	PIN O
P	Q	R		
PIN P	PIN Q	PIN R		

; INV AND OR NAND NOR XOR
COMMENT

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	COMMENT
L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	INVERTER
H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	INVERTER
X	X	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	AND
X	X	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	AND
X	X	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	AND
X	X	H	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	AND
X	X	X	X	X	L	L	L	X	X	X	X	X	X	X	X	X	X	OR
X	X	X	X	X	L	H	H	X	X	X	X	X	X	X	X	X	X	OR
X	X	X	X	X	H	L	H	X	X	X	X	X	X	X	X	X	X	OR
X	X	X	X	X	H	H	H	X	X	X	X	X	X	X	X	X	X	OR
X	X	X	X	X	X	X	X	L	L	L	H	X	X	X	X	X	X	NAND
X	X	X	X	X	X	X	X	L	L	H	H	X	X	X	X	X	X	NAND
X	X	X	X	X	X	X	X	L	H	L	H	X	X	X	X	X	X	NAND
X	X	X	X	X	X	X	X	H	L	L	H	X	X	X	X	X	X	NAND
X	X	X	X	X	X	X	X	H	H	H	L	X	X	X	X	X	X	NAND
X	X	X	X	X	X	X	X	X	X	X	X	L	L	H	X	X	X	NOR
X	X	X	X	X	X	X	X	X	X	X	X	L	H	L	X	X	X	NOR
X	X	X	X	X	X	X	X	X	X	X	X	H	L	L	X	X	X	NOR
X	X	X	X	X	X	X	X	X	X	X	X	H	H	L	X	X	X	NOR
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L	L	XOR

LEGEND: H HIGH, L LOW, C CLOCK, X IRRELEVANT, Z OFF

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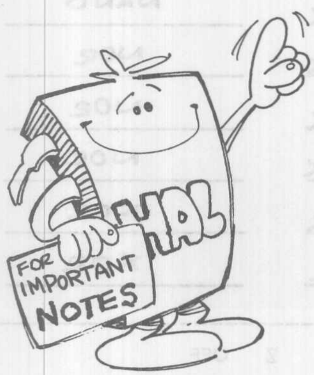
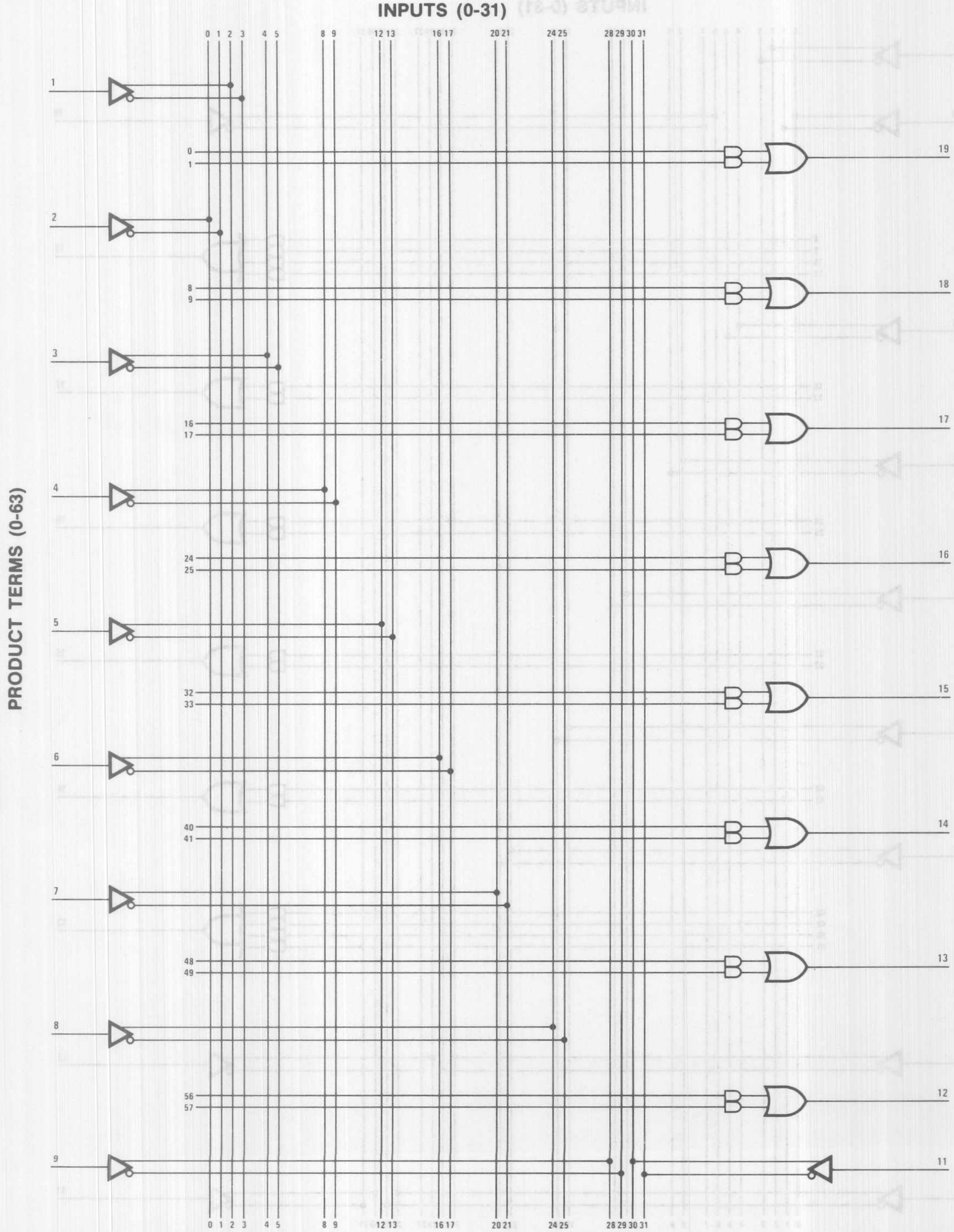
Notes



Logic Diagram HAL10H8



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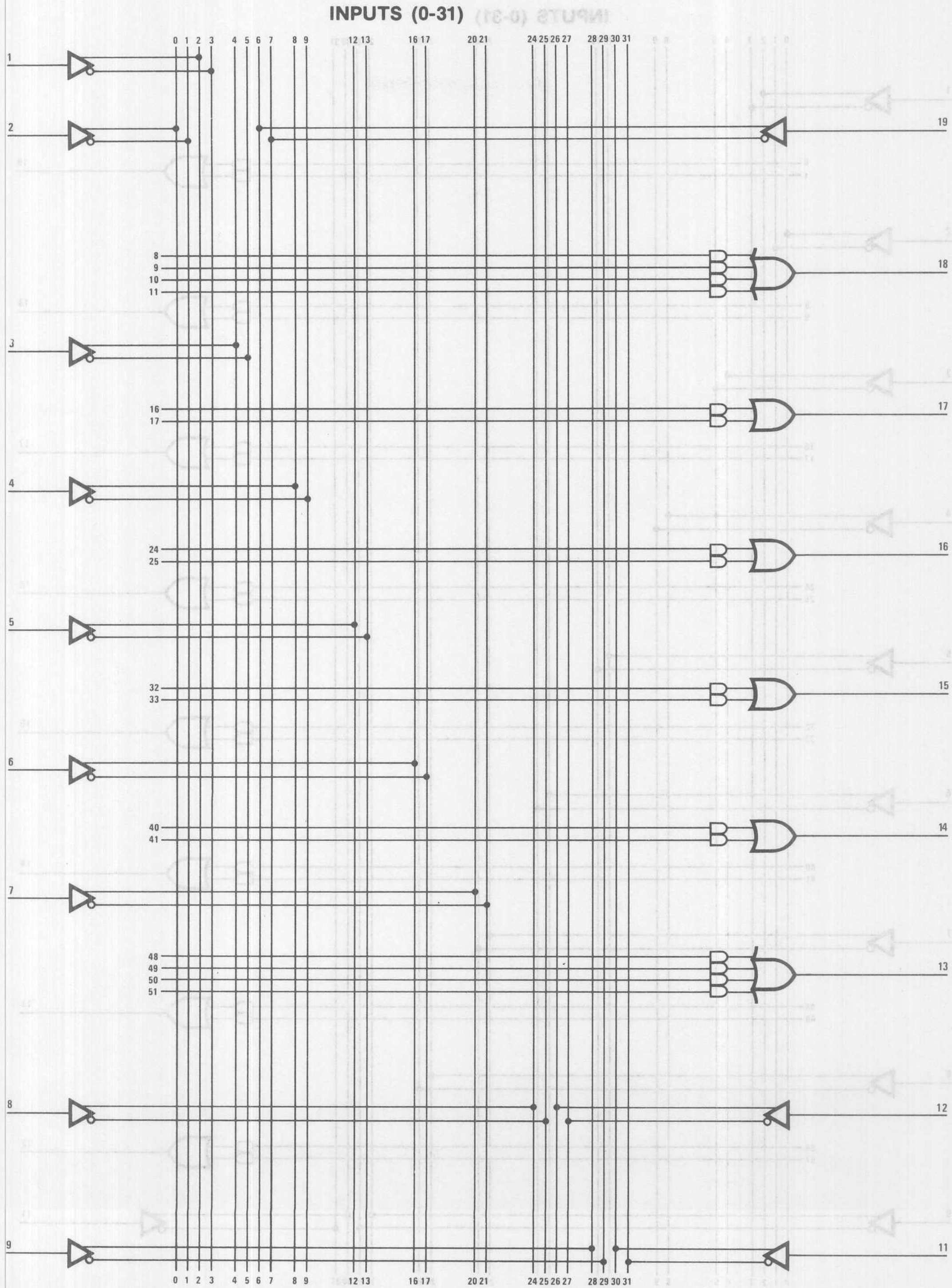
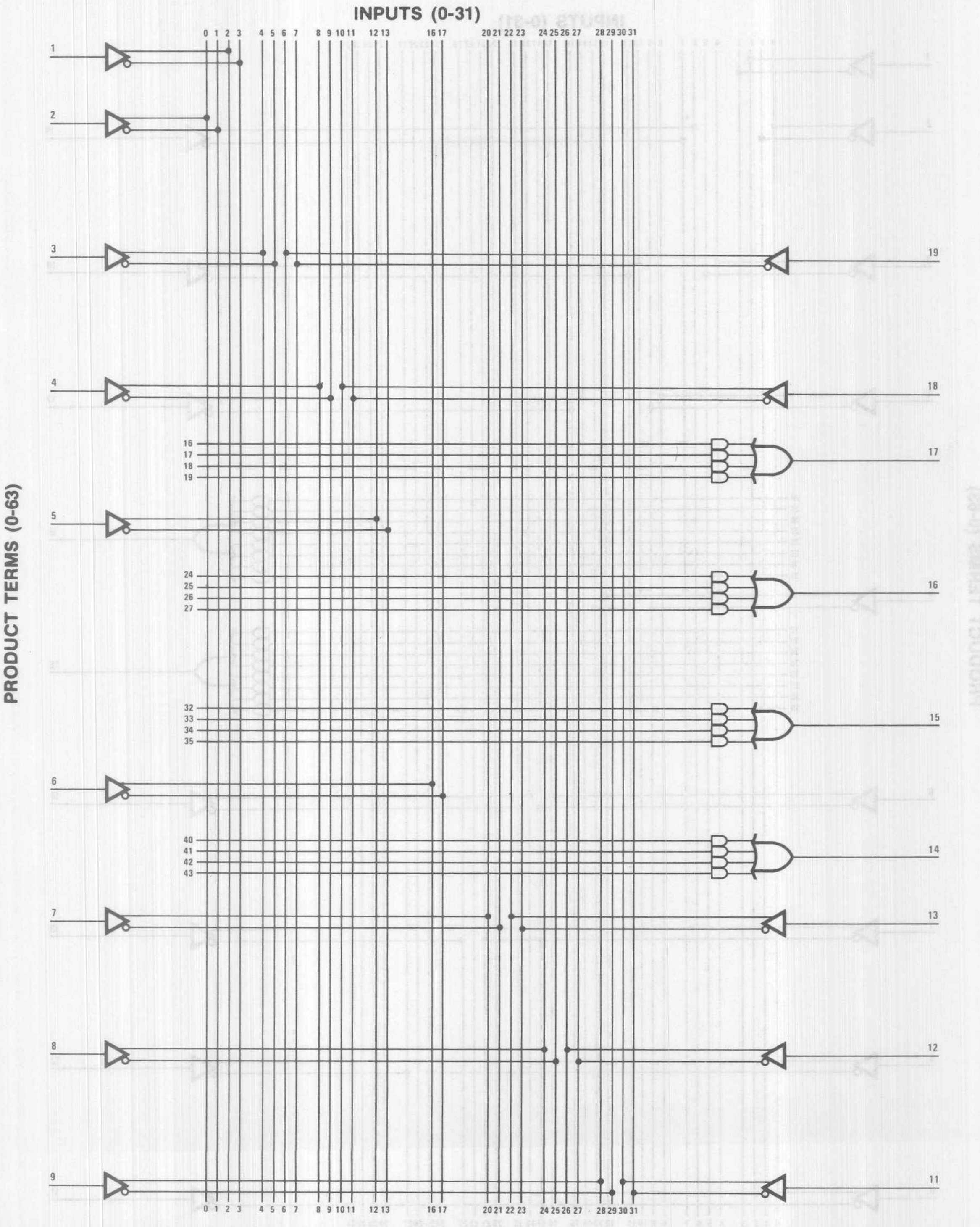
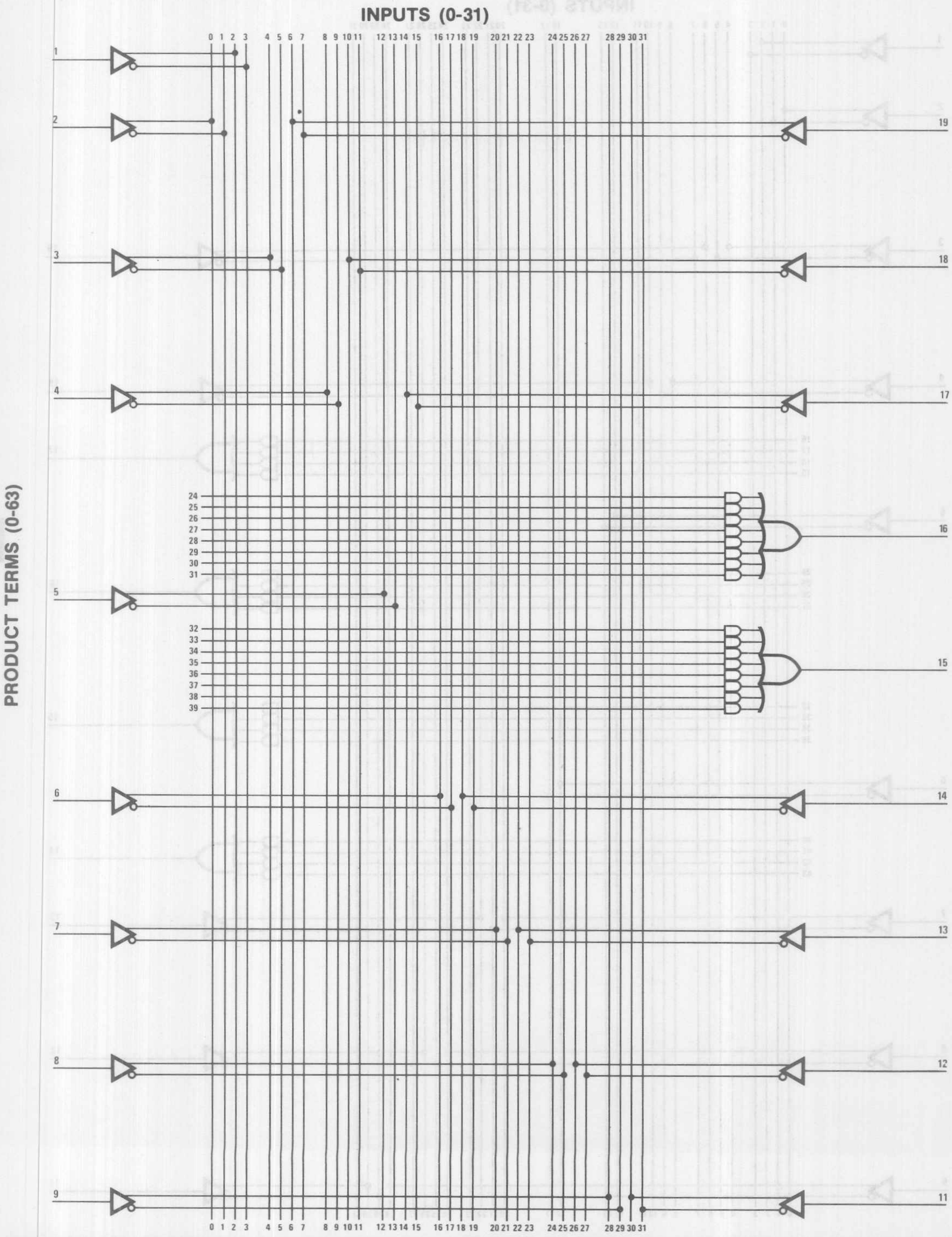
Logic Diagram HAL12H6



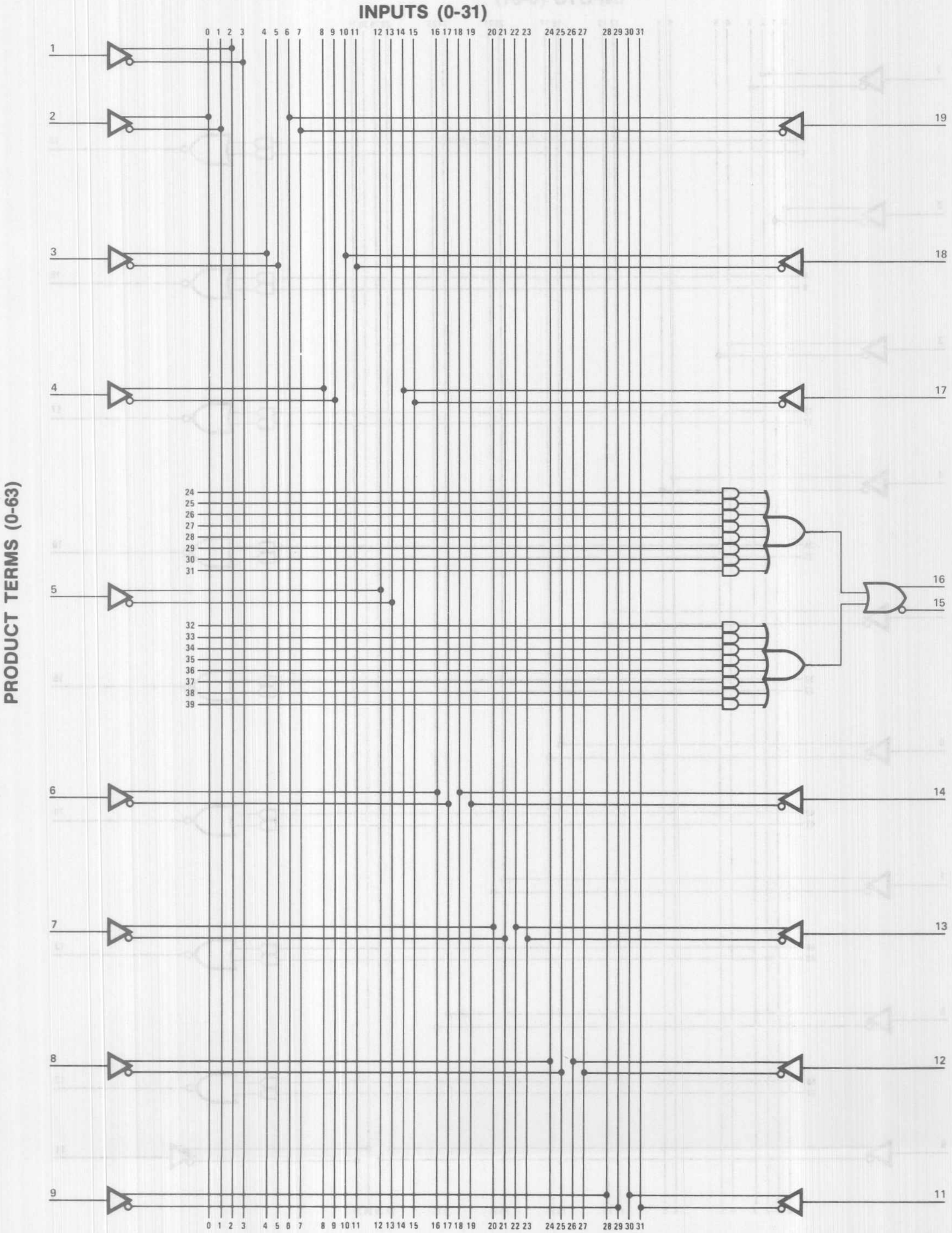
Logic Diagram HAL14H4



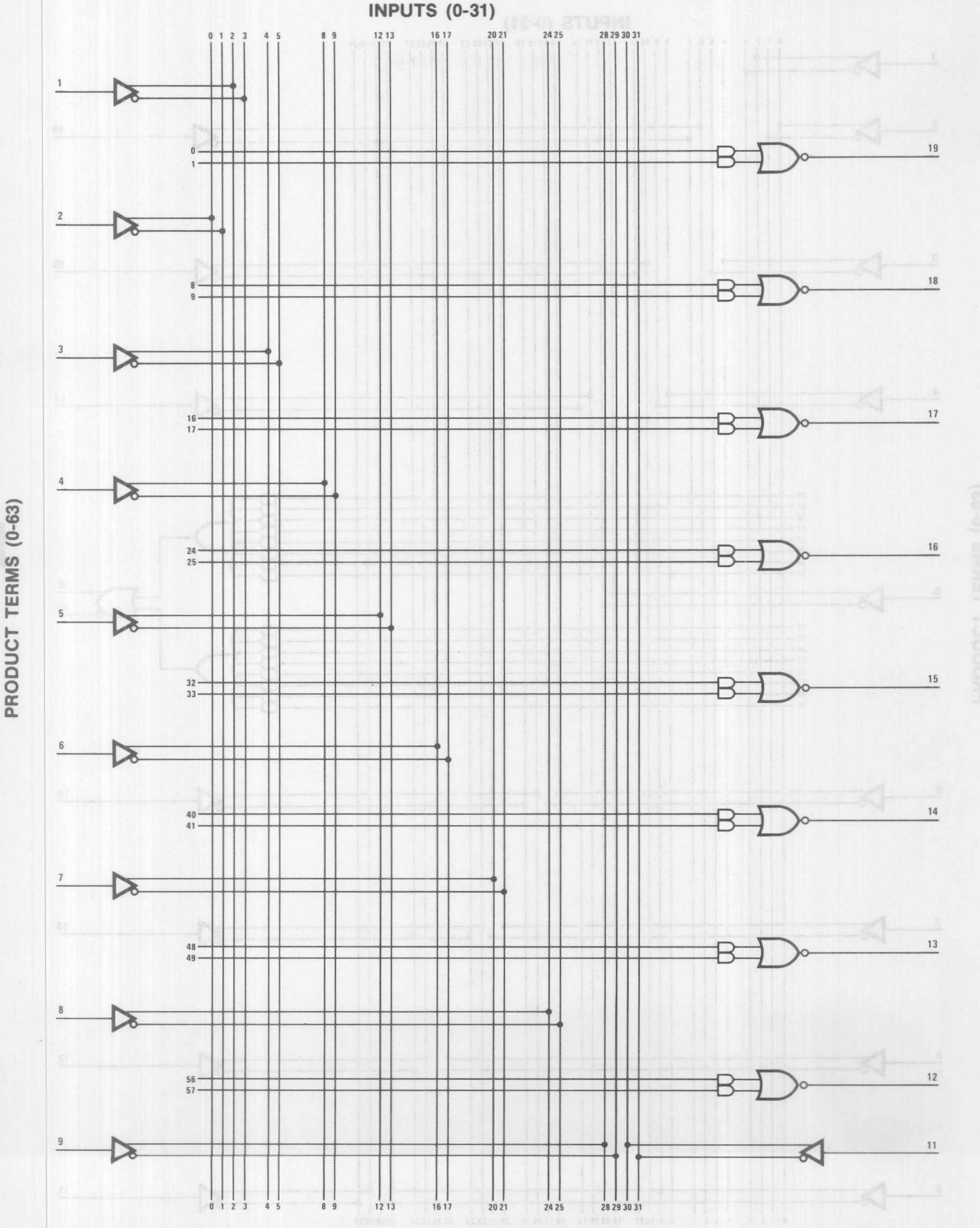
Logic Diagram HAL16H2



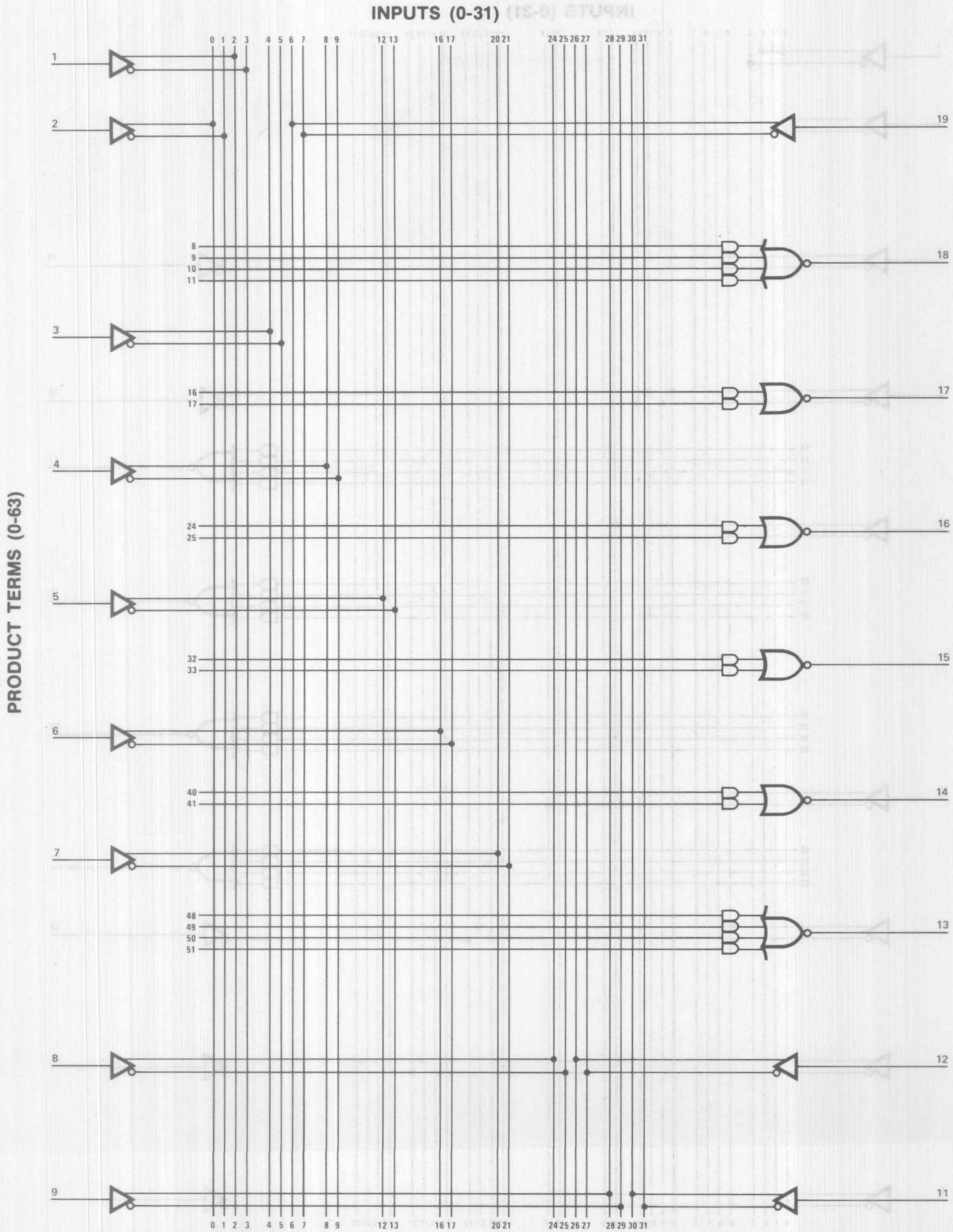
Logic Diagram HAL16C1

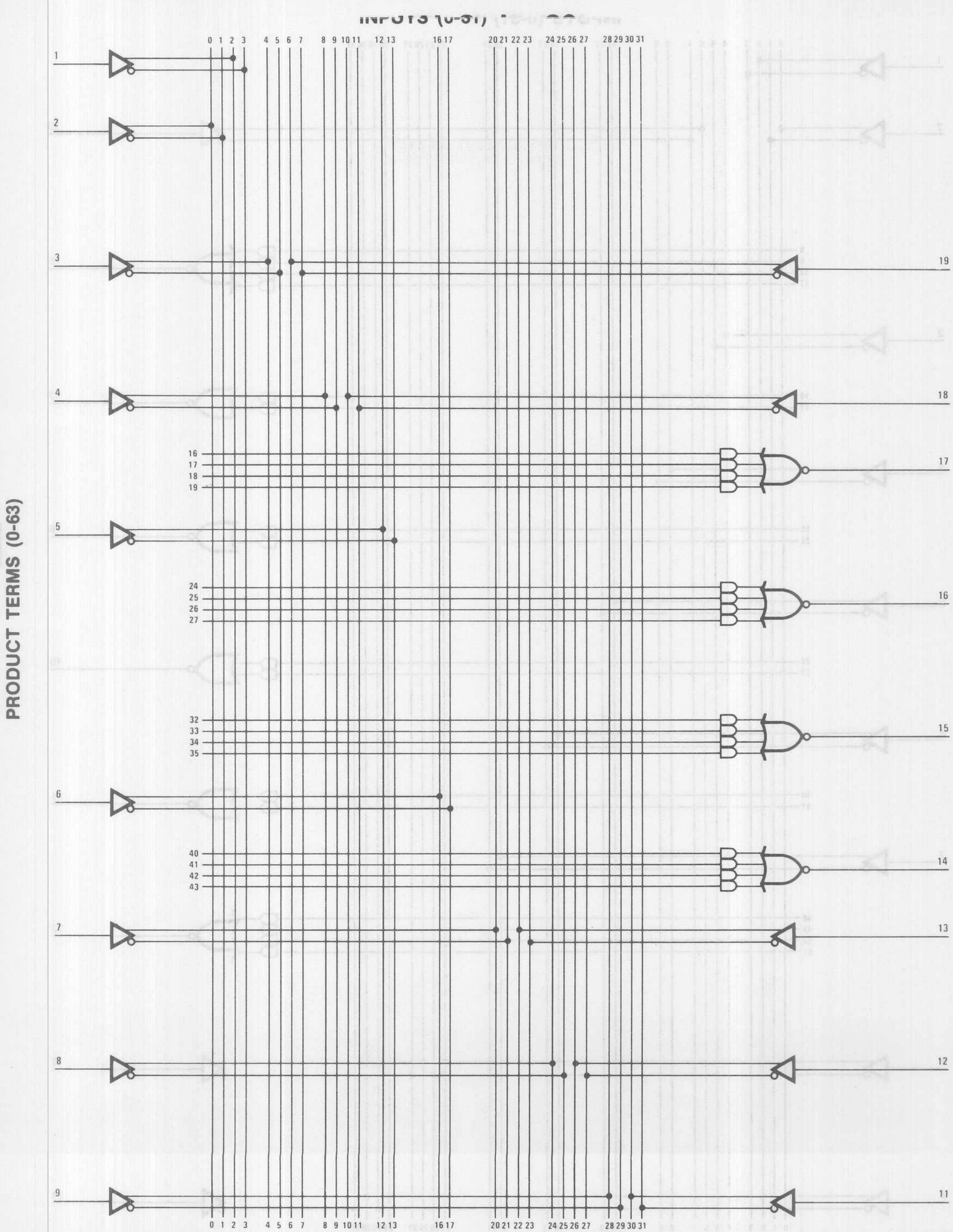


Logic Diagram HAL10L8



Logic Diagram HAL12L6




INPUTS (0-31)
PRODUCT TERMS (0-63)
0 1 2 3 4 5 6 7 8 9 10 11 12 13 16 17 20 21 22 23 24 25 26 27 28 29 30 31
1
2
3
4
5
6
7
8
9
19
18
17
16
15
14
13
12
11
16
17
18
19
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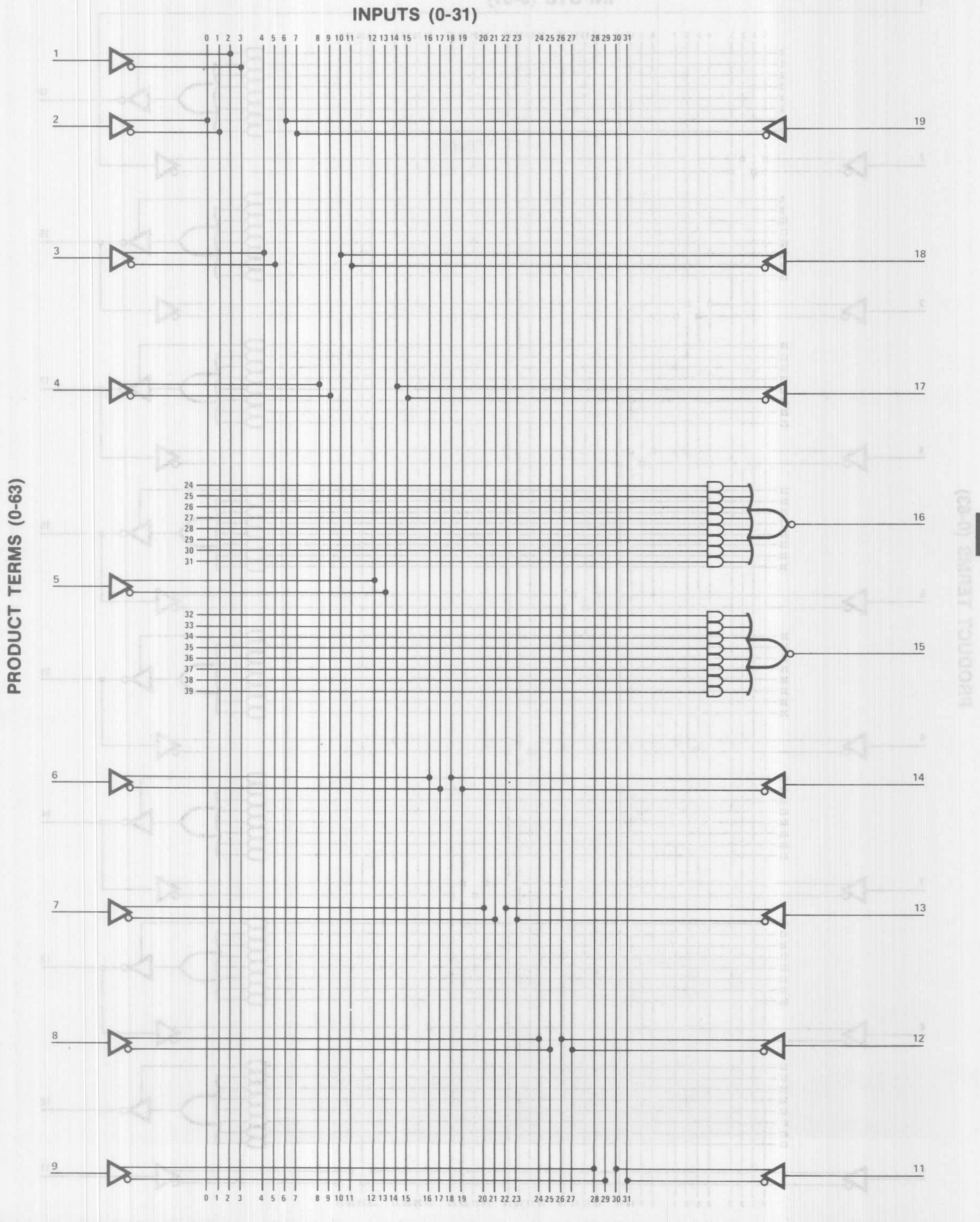
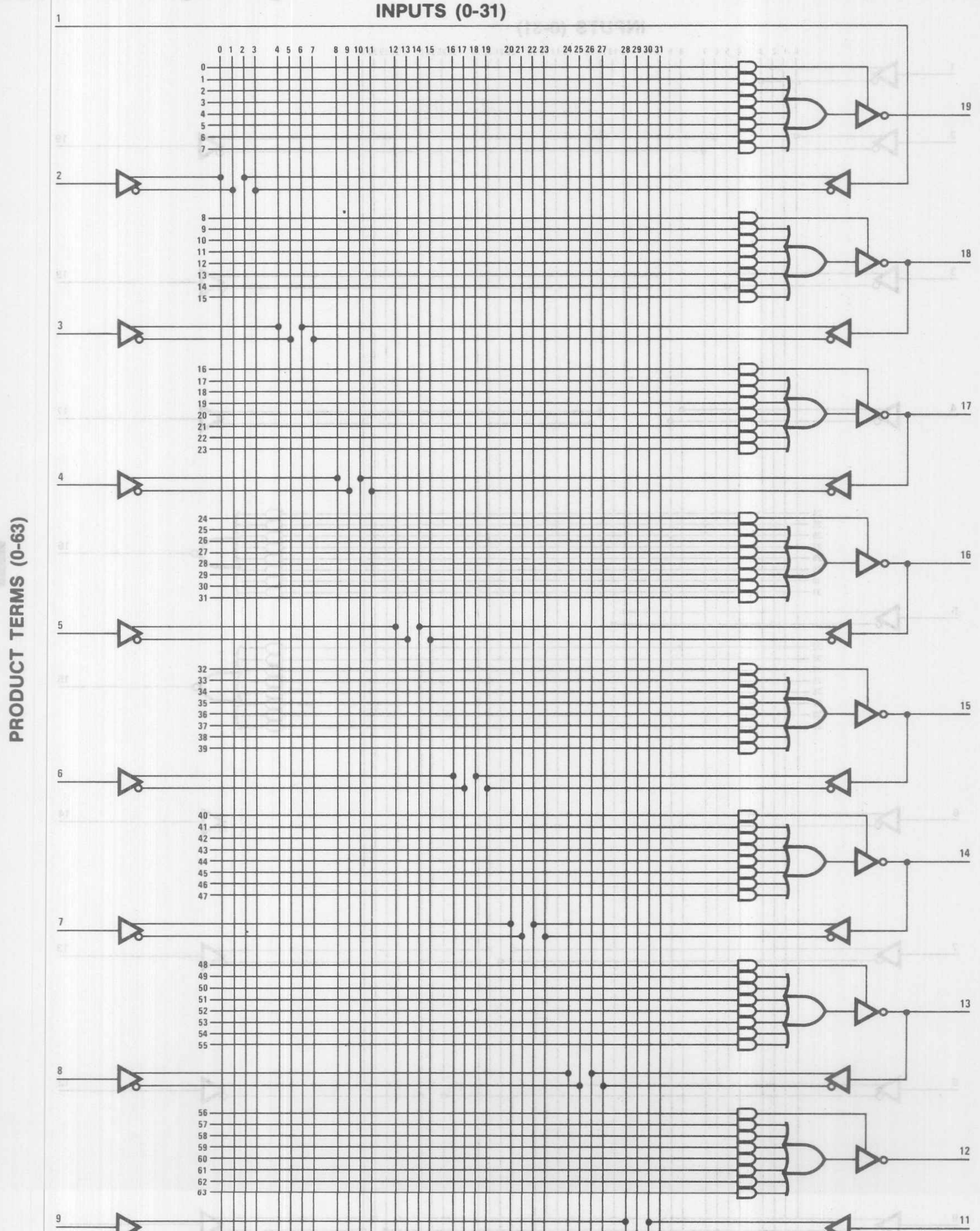
42
43

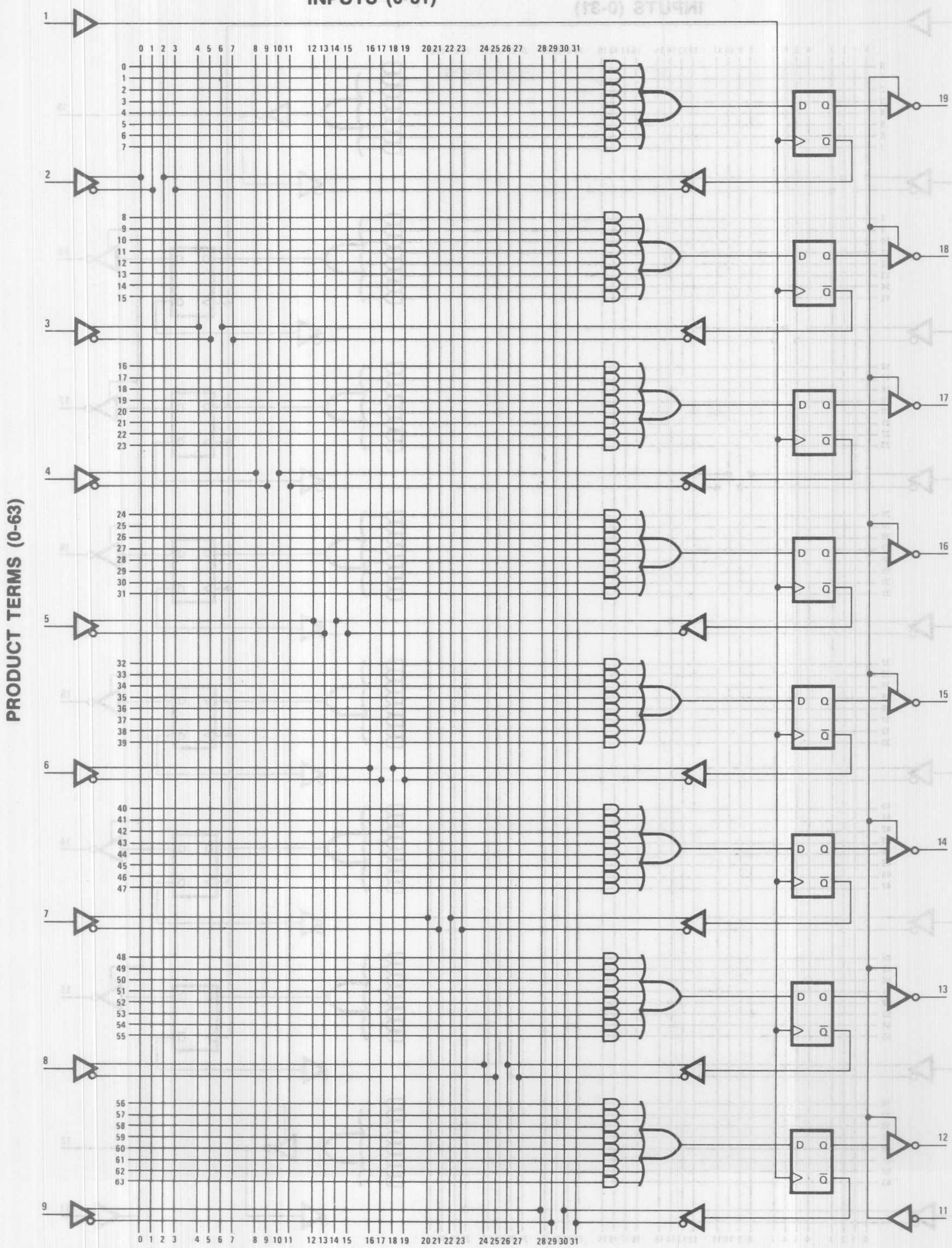
Logic Diagram HAL16L2

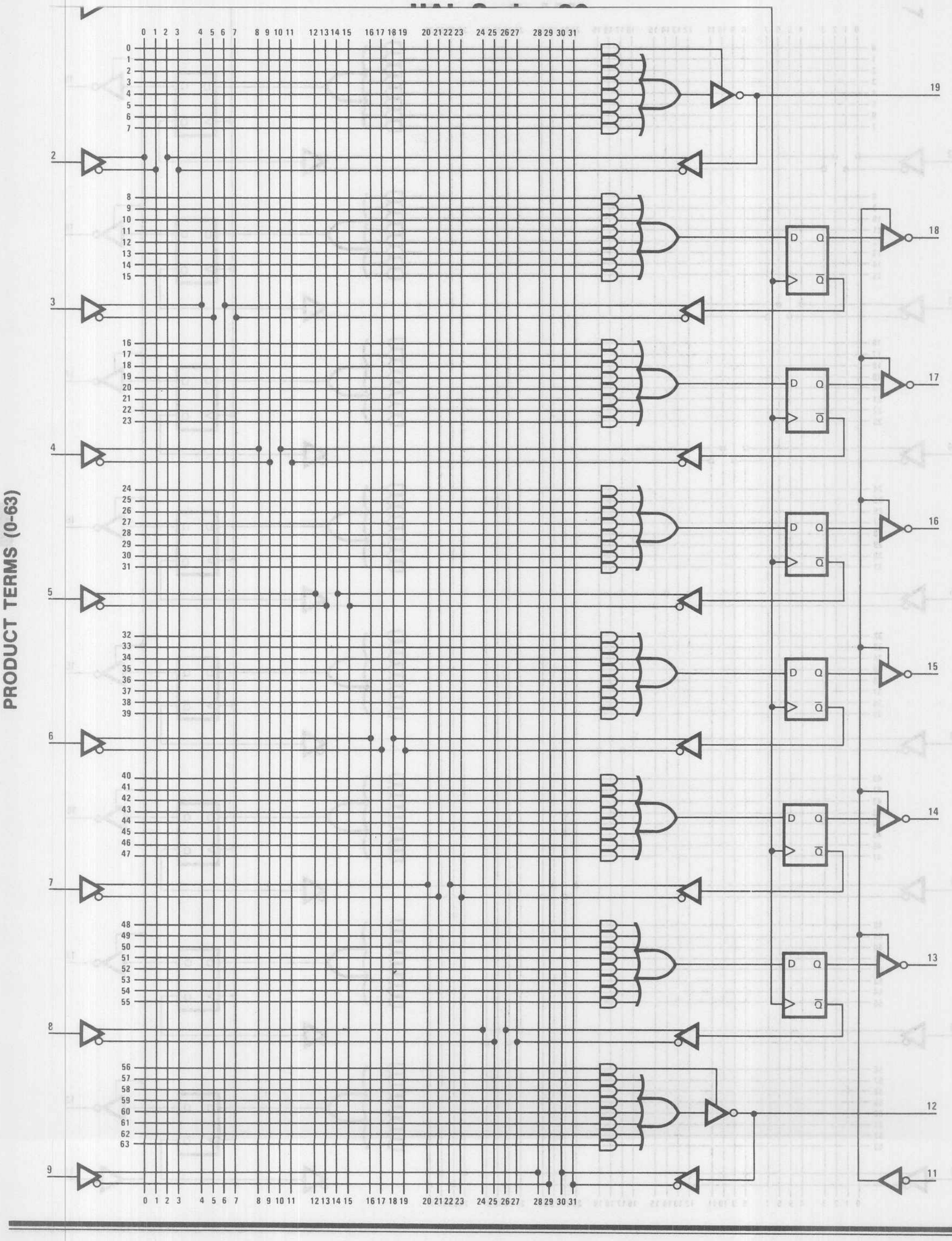


Logic Diagram HAL16L8



Logic Diagram HAL16R8




PRODUCT TERMS (0-63)
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
19
18
17
16
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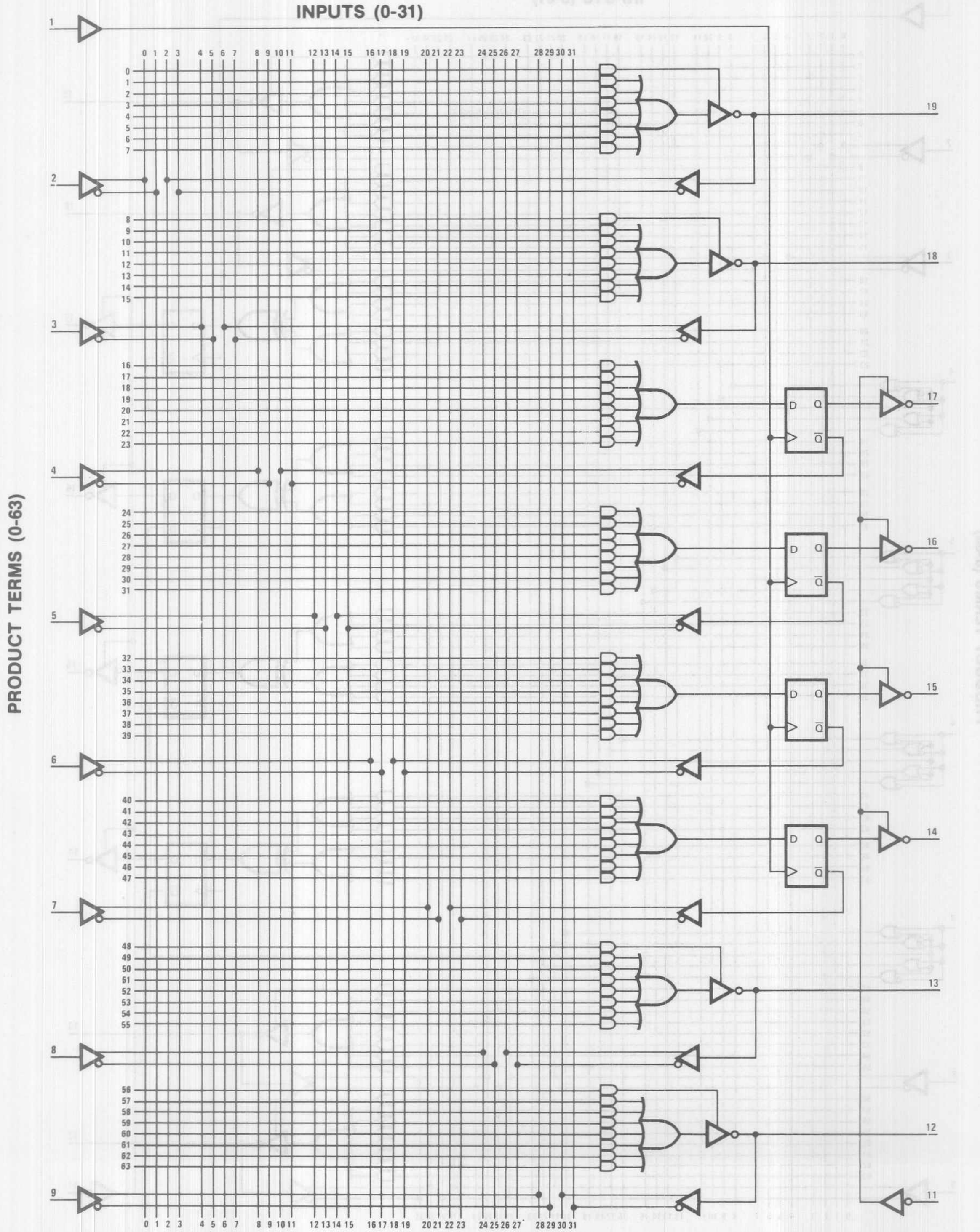
14
13
12
11
2
3
4
5
6
7
8
9
D Q
Q̄

Logic Diagram HAL16R4



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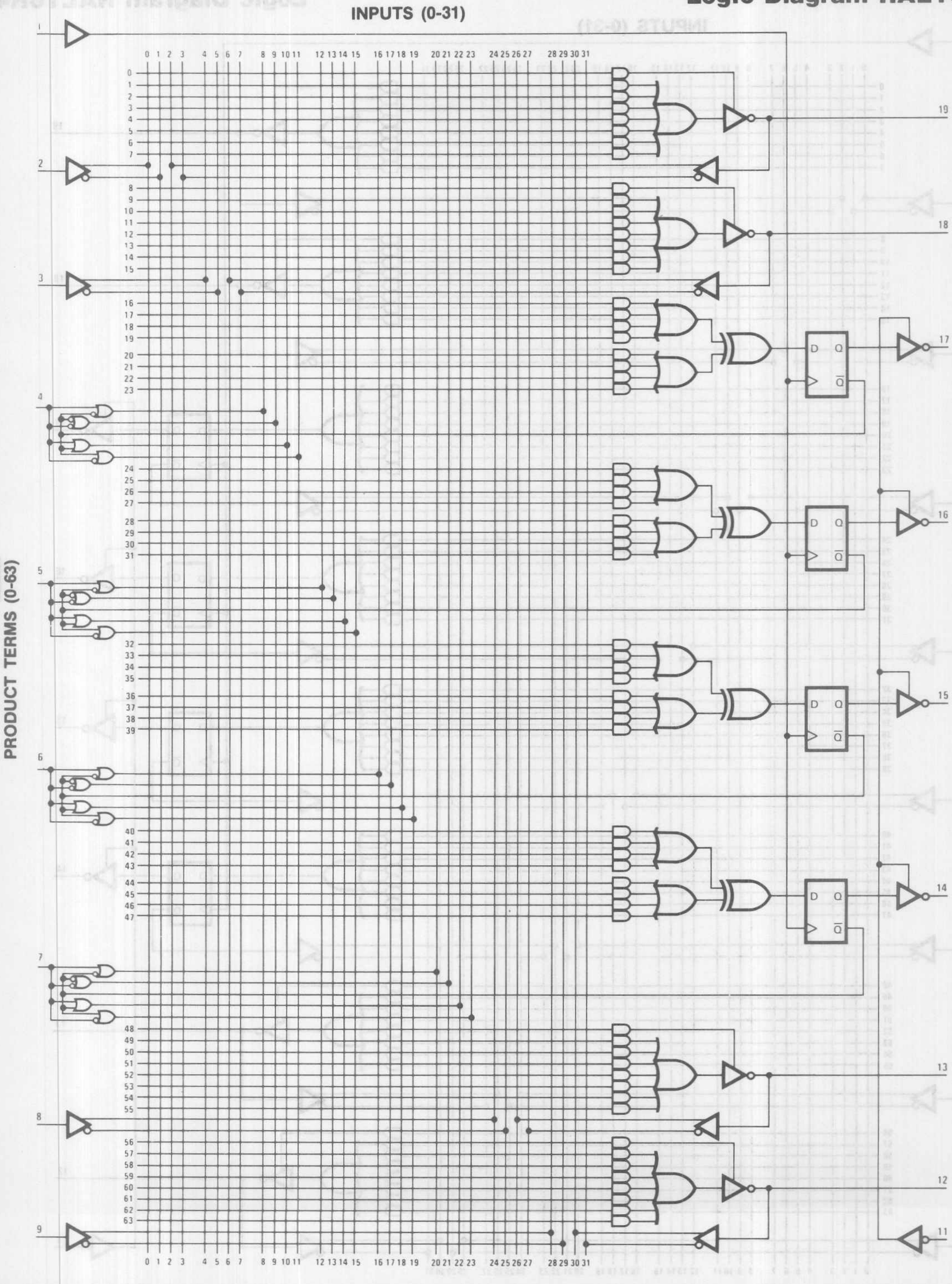
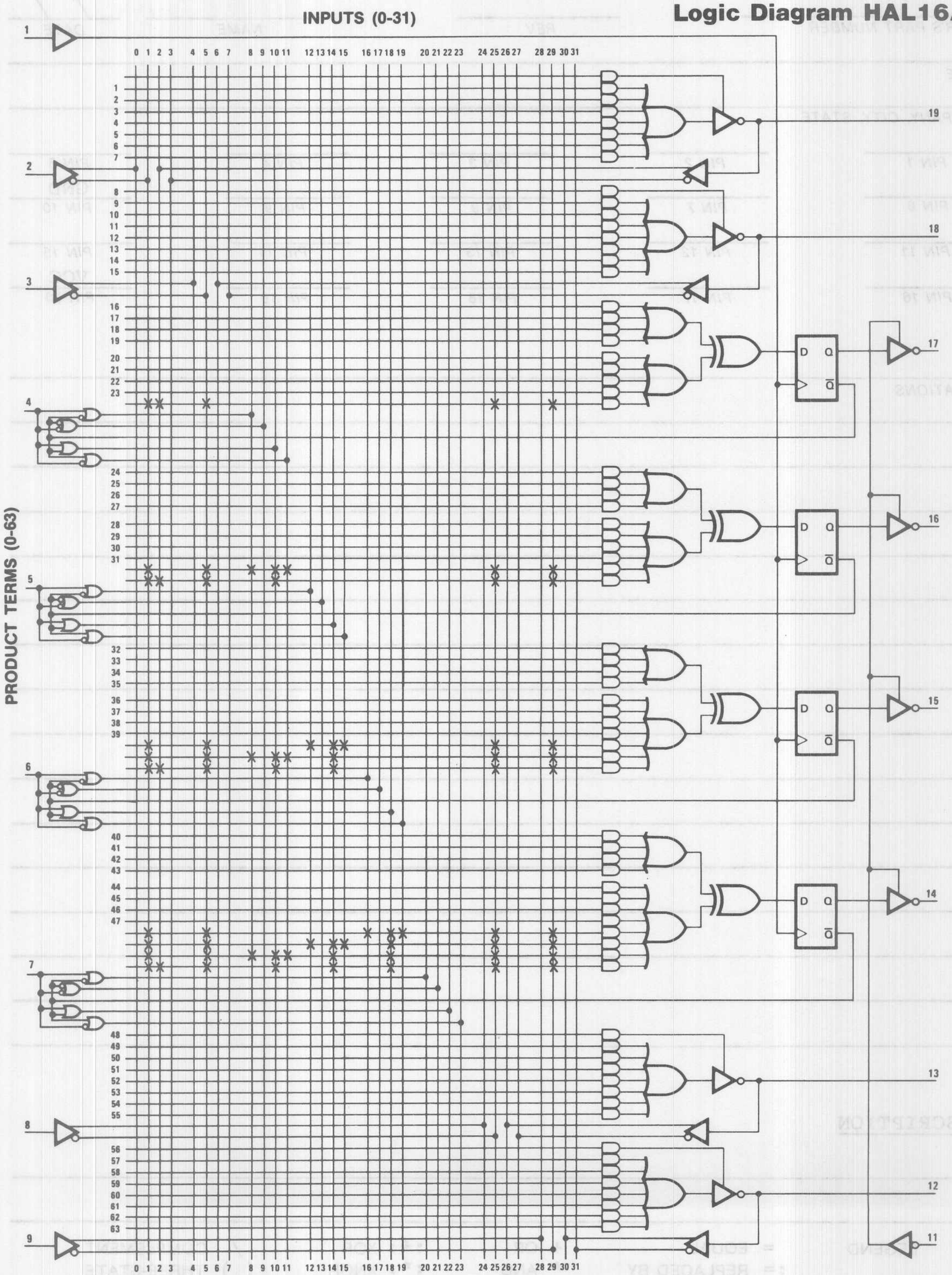
Logic Diagram HAL16X4



Logic Diagram HAL16A4



7

TITLE

COMPANY, CITY, STATE

PIN 1	PIN 2	PIN 3	PIN 4	PIN 5
PIN 6	PIN 7	PIN 8	PIN 9	GND PIN 10
PIN 11	PIN 12	PIN 13	PIN 14	PIN 15
PIN 16	PIN 17	PIN 18	PIN 19	VCC PIN 20

EQUATIONS

DESCRIPTION

LEGEND:				
= EQUAL	+ OR	:+: XOR	/ COMPLEMENT	
:= REPLACED BY	* AND	:*: XNOR	( ) THREE-STATE	

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FUNCTION TABLE

PIN A	PIN B	PIN C	PIN D	PIN E
PIN F	PIN G	PIN H	PIN I	PIN J
PIN K	PIN L	PIN M	PIN N	PIN O
PIN P	PIN Q	PIN R		

; COMMENT

; A B C D E F G H I J K L M N O P Q R COMMENT

LEGEND: H HIGH C CLOCK Z OFF
L LOW X IRRELEVANT

Hard Array Logic Family
HAL Series 24 Data Sheet

Features/Benefits

- Gate array equivalent of up to 300 gates.
- Semi-custom solution
- Reduces SSI/MSI chip count greater than 5 to 1
- Prototype using field-programmable version — PAL.
- Cost savings up to 40% compared to PAL
- Security link disabled for design secrecy.
- Test and simulation made simple with PALASM Function Table
- Saves space with 24-pin SKINNYDIP™ packages

Description

The HAL family utiizes standard Low-Power Schottky TTL process and automated mask pattern generation directly from logic equations to provide a semi-custom gate array for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The family lets the systems engineer "design his own chip" by AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production.

The HAL transfer function is the familiar sum of products. Like the ROM, the HAL has a single array of selectable gates. Unlike the ROM, the HAL is a selectable AND array driving a fixed OR array (the ROM is a fixed AND array driving a selectable OR array). In addition the HAL provides thee options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback
- Exclusive-OR gates

Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops which are loaded on the low-to-high transition of the clock. HAL Logic Diagrams are shown with all fuses blown, enabling the designer to use the diagrams as coding sheets.

PART NUMBER	PKG	DESCRIPTION
HAL12L10	J,N,F	Deca 12 Input And-Or-Invert Gate Array
HAL14L8	J,N,F	Octal 14 Input And-Or-Invert Gate Array
HAL16L6	J,N,F	Hex 16 Input And-Or-Invert Gate Array
HAL18L4	J,N,F	Quad 18 Input And-Or-Invert Gate Array
HAL20L2	J,N,F	Dual 20 Input And-Or-Invert Gate Array
HAL20C1	J,N,F	20 Input And-Or/And-Or Invert Gate Array
HAL20L10	J,N,F	Deca 20 Input And-Or-Invert Gate Array
HAL20X10	J,N,F	Deca 20 Input Registered And-Or-Xor Gate Array
HAL20X8	J,N,F	Octal 20 Input Registered And-Or-Xor Gate Array
HAL20X4	J,N,F	Quad 20 Input Registered And-Or-Xor Gate Array

To design a HAL, the user first programs and debugs a PAL using PALASM and the "PAL DESIGN SPECIFICATION" standard format. This specification is submitted to Monolithic Memories where it is computer processed and assigned a bit pattern number, e.g., P01234. Monolithic Memories accepts the PAL DESIGN SPECIFICATION in one of three forms:

1. Computer generated listing.
2. Typed or hand-written forms F107 and F108. See example on pages 7-30, 7-31 and forms on pages 7-42 and 7-43.
3. Direct online data transmission to Monolithic Memories Timeshare computer system via telephone (local telephone network to major US cities, London and Paris) or TWX (online Boston TWX no.).

Monolithic Memories will provide a PAL sample for customer qualification. The user then submits a purchase order for a HAL of the specified bit pattern number, e.g., HAL18L4 P01234. See Ordering Information below.

Ordering Information

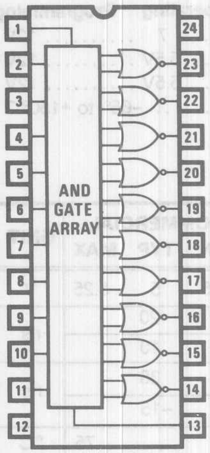
HARD ARRAY LOGIC FAMILY
NUMBER OF ARRAY INPUTS
OUTPUT TYPE
L = ACTIVE LOW
C = COMPLEMENTARY
X = EXCLUSIVE-OR REGISTERED

NUMBER OF OUTPUTS
TEMPERATURE RANGE
C = 0C TO +75C
M = -55C TO +125C
PACKAGE
N = PLASTIC DIP
J = CERAMIC DIP
F = FLAT PACK
OPTIONAL HI-REL PROCESSING
883B = MIL-STD-883, METHOD 5004 & 5005 LEVEL B
883C = MIL-STD-883, METHOD 5004 & 5005 LEVEL C
B = MIL-STD-883, METHOD 5004 EQUIVALENT
C = MIL-STD-883, METHOD 5004 EQUIVALENT
BIT PATTERN NUMBER

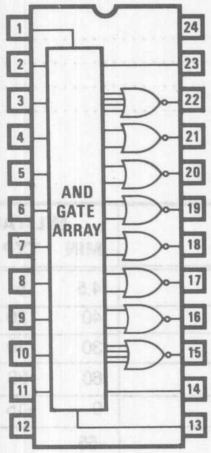
HAL 18 L4 CJ 883B P01234

SKINNYDIP is a registered trademark of Monolithic Memories

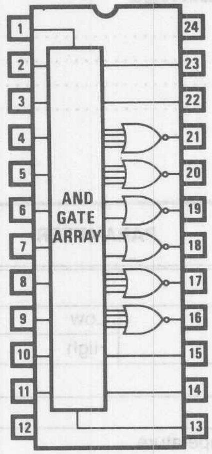
HAL12L10



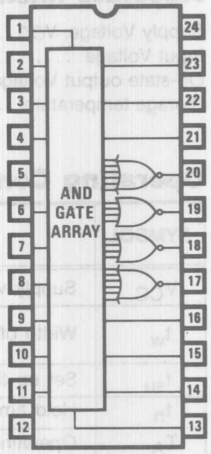
HAL14L8



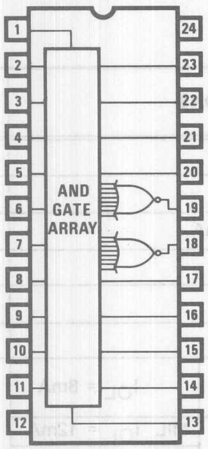
HAL16L6



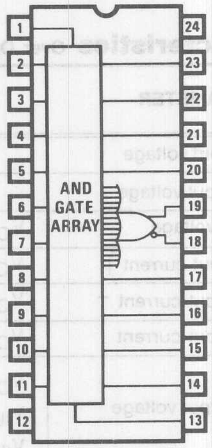
HAL18L4



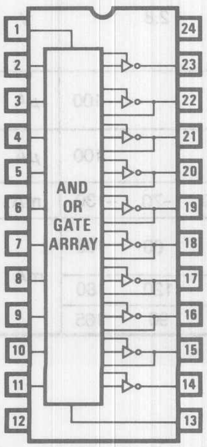
HAL20L2



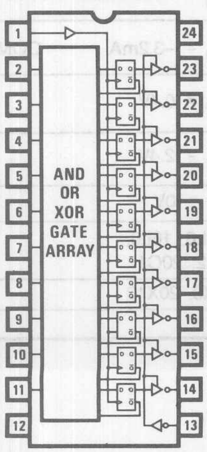
HAL20C1



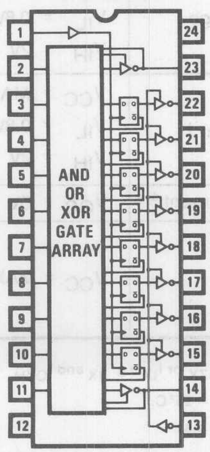
HAL20L10



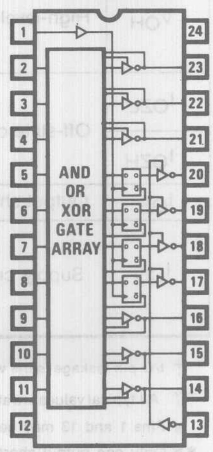
HAL20X10



HAL20X8



HAL20X4



Input Voltage .... 5.5V 12V*
Off-state output Voltage .... 5.5V 12V
Storage temperature .... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	40	20		35	20		ns
		High	30	10		25	10		ns
t_{su}	Set up time		60	38		50	38		ns
t_h	Hold time		0	−15		0	−15		ns
T_A	Operating free air temperature		-55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP††	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			-0.8	−1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX	V_I = 0.4V			-0.02	−0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	12L10, 14L8, 16L6, 18L4, 20L2, 20C1	I_{OL} = 8mA		0.3	0.5	V
			20L10, 20X10, 20X8, 20X4	MIL I_{OL} = 12mA				
				COM I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −2mA	MIL	2.4	2.8		V
			I_{OH} = −3.2mA	COM				
I_{OZL}	Off-state output current †	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.4V				−100	μA
I_{OZH}			V_O = 2.4V				100	μA
I_{OS}	Output short-circuit current **	V_{CC} = 5V	V_O = 0V		-30	-70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX	12L10, 14L8, 16L6, 18L4, 20L2, 20C1			60	100	mA
			20X4, 20X8, 20X10			120	180	mA
			20L10			90	165	mA

† I/O pin leakage is the worst case of I_{OZX} or I_{IX} e.g. I_{IX} and I_{OZH}

†† All typical values are at V_{CC} = 5V, T_A = 25°C.

* Pins 1 and 13 may be raised to 22V max.

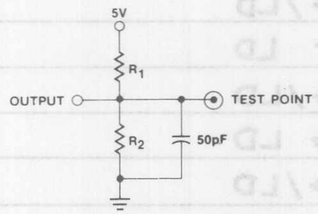
** Only one output shorted at a time.

Switching Characteristics

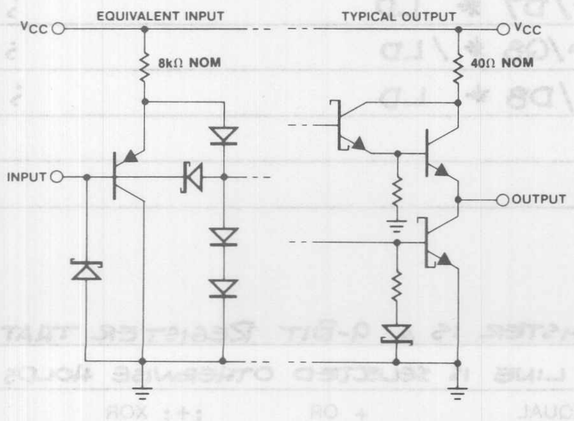
Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input to output: 12L10, 14L8, 16L6, 18L4, 20L2, 20C1	R_1 = 560Ω, R_2 = 1.1kΩ		25	45		25	40	ns
t_{PD}	Input or feedback to output	20L10, 20X10, 20X8, 20X4, R_1 = 200Ω, R_2 = 390Ω		35	60		35	50	ns
t_{CLK}	Clock to output or feedback			20	35		20	30	ns
t_{PZX}	Pin 13 to output enable			20	45		20	35	ns
t_{PXZ}	Pin 13 to output disable			20	45		20	35	ns
t_{PZX}	Input to output enable			35	55		35	45	ns
t_{PXZ}	Input to output disable			35	55		35	45	ns
f_{MAX}	Maximum frequency		10.5	16		12.5	16		MHz

Test Load



Schematic of Inputs and Outputs



HAL 20X10

HAL DESIGN SPECIFICATION

PART NUMBER: INT 8C2

USER'S PART NUMBER

REV: 0

NAME: BIRKNER

DATE: 2/28/81

TITLE: NONAL REGISTER

COMPANY, CITY, STATE: MMI SUNNYVALE, CA

CK	D0	D1	D2	D3	D4
PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6
D5	D6	D7	D8	/LD	GND
PIN 7	PIN 8	PIN 9	PIN 10	PIN 11	PIN 12
IOE	NC	Q8	Q7	Q7	Q5
PIN 13	PIN 14	PIN 15	PIN 16	PIN 17	PIN 18
Q4	Q3	Q2	Q1	Q0	VCC
PIN 19	PIN 20	PIN 21	PIN 22	PIN 23	PIN 24

EQUATIONS

```
/Q0 := / Q0 * /LD      ; HOLD Q0
     + /D0 * LD        ; LOAD D0
/Q1 := /Q1 * /LD       ; HOLD Q1
     + / D1 * LD       ; LOAD D1
/Q2 := / Q2 * /LD      ; HOLD Q2
     + / D2 * LD       ; LOAD D2
/Q3 := / Q3 * /LD      ; HOLD Q3
     + / D3 * LD       ; LOAD D3
/Q4 := /Q4 * /LD       ; HOLD Q4
     + / D4 * LD       ; LOAD D4
/Q5 := /Q5 * /LD       ; HOLD Q5
     + / D5 * LD       ; LOAD D5
/Q6 := /Q6 * /LD       ; HOLD Q6
     + /D6 * LD        ; LOAD D6
/Q7 := /Q7 * /LD       ; HOLD Q7
     + /D7 * LD        ; LOAD D7
/Q8 := /Q8 * / LD      ; HOLD Q8
     + /D8 * LD        ; LOAD D8
```

DESCRIPTION:

THE NONAL REGISTER IS A 9-BIT REGISTER THAT LOADS THE DATA INPUTS IF LOAD LINE IS SELECTED OTHERWISE HOLDS THE ORIGINAL DATA.

LEGEND: = EQUAL; := REPLACED BY; + OR; * AND; :+: XOR; :*: XNOR; / COMPLEMENT; ( ) THREE-STATE

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FUNCTION TABLE

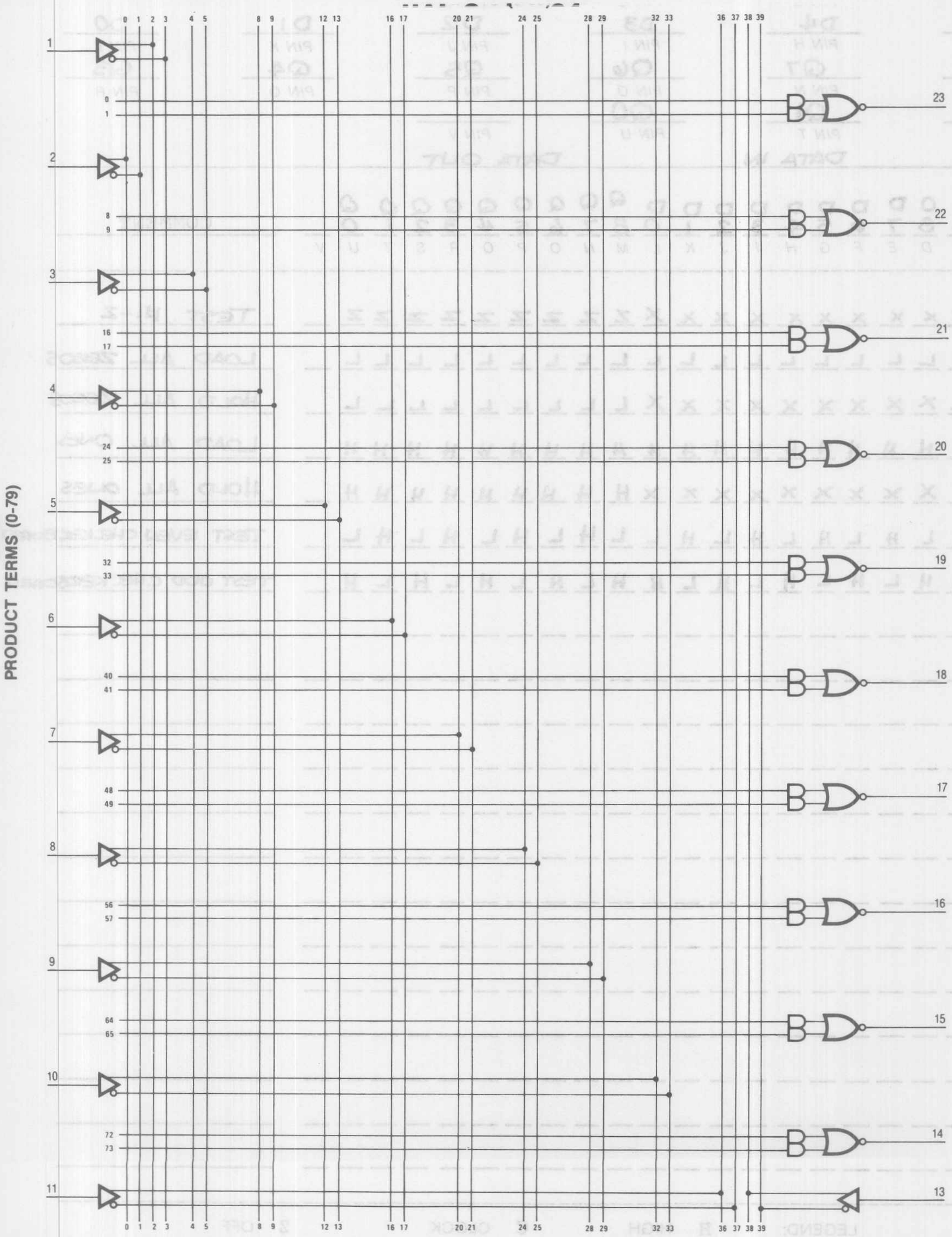
CK	OE	LD	D8	D7	D6
PIN A	PIN B	PIN C	PIN D	PIN E	PIN F
D5	D4	D3	D2	D1	D0
PIN G	PIN H	PIN I	PIN J	PIN K	PIN L
Q8	Q7	Q6	Q5	Q4	Q3
PIN M	PIN N	PIN O	PIN P	PIN Q	PIN R
Q2	Q1	Q0			
PIN S	PIN T	PIN U	PIN V		

; DATA IN DATA OUT

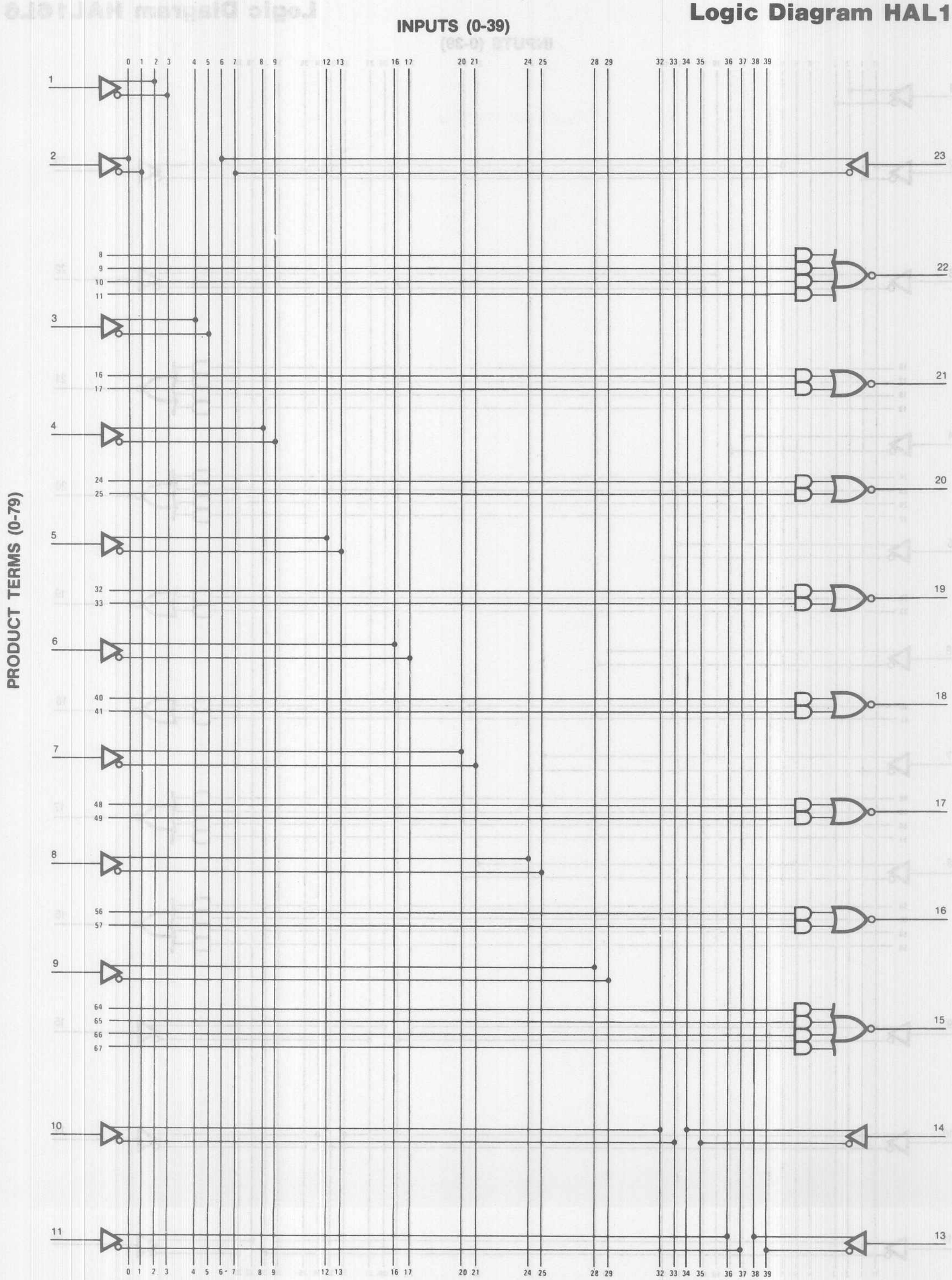
COMMENT

;CK	OE	LD	D8	D7	D6	D5	D4	D3	D2	D1	D0	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0		COMMENT
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	
C	L	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z		TEST HI-Z
C	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L		LOAD ALL ZEROS
C	H	L	X	X	X	X	X	X	X	X	X	L	L	L	L	L	L	L	L	L		HOLD ALL ZEROS
C	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H		LOAD ALL ONES
C	H	L	X	X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	H		HOLD ALL ONES
C	H	H	L	H	L	H	L	H	L	H	L	L	H	L	H	L	H	L	H	L		TEST EVEN CHECKERBOARD
C	H	H	H	L	H	L	H	L	H	L	H	H	L	H	L	H	L	H	L	H		TEST ODD CHECKERBOARD

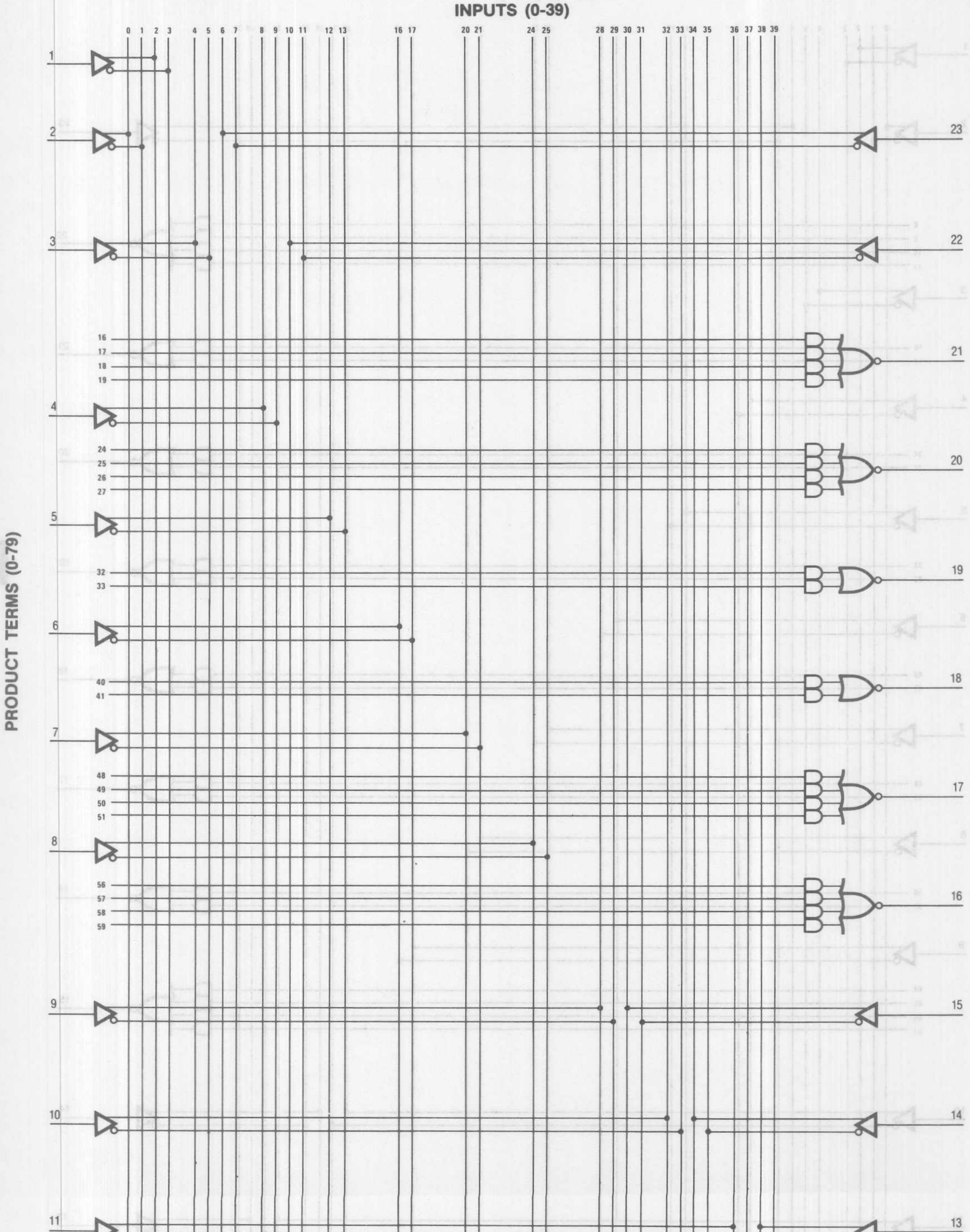
LEGEND: H HIGH, L LOW, C CLOCK, X IRRELEVANT, Z OFF


PRODUCT TERMS (0-79)

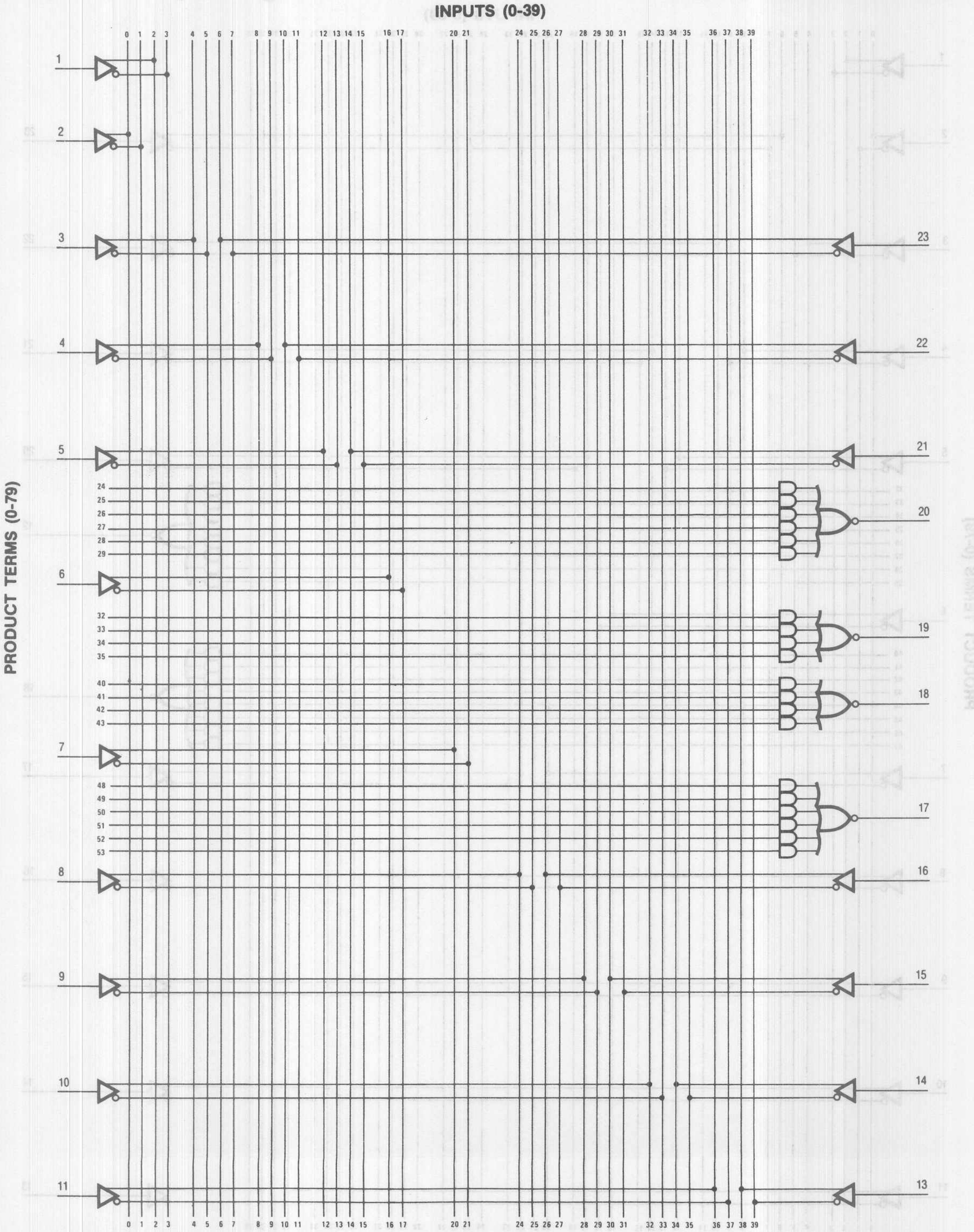
Logic Diagram HAL14L8

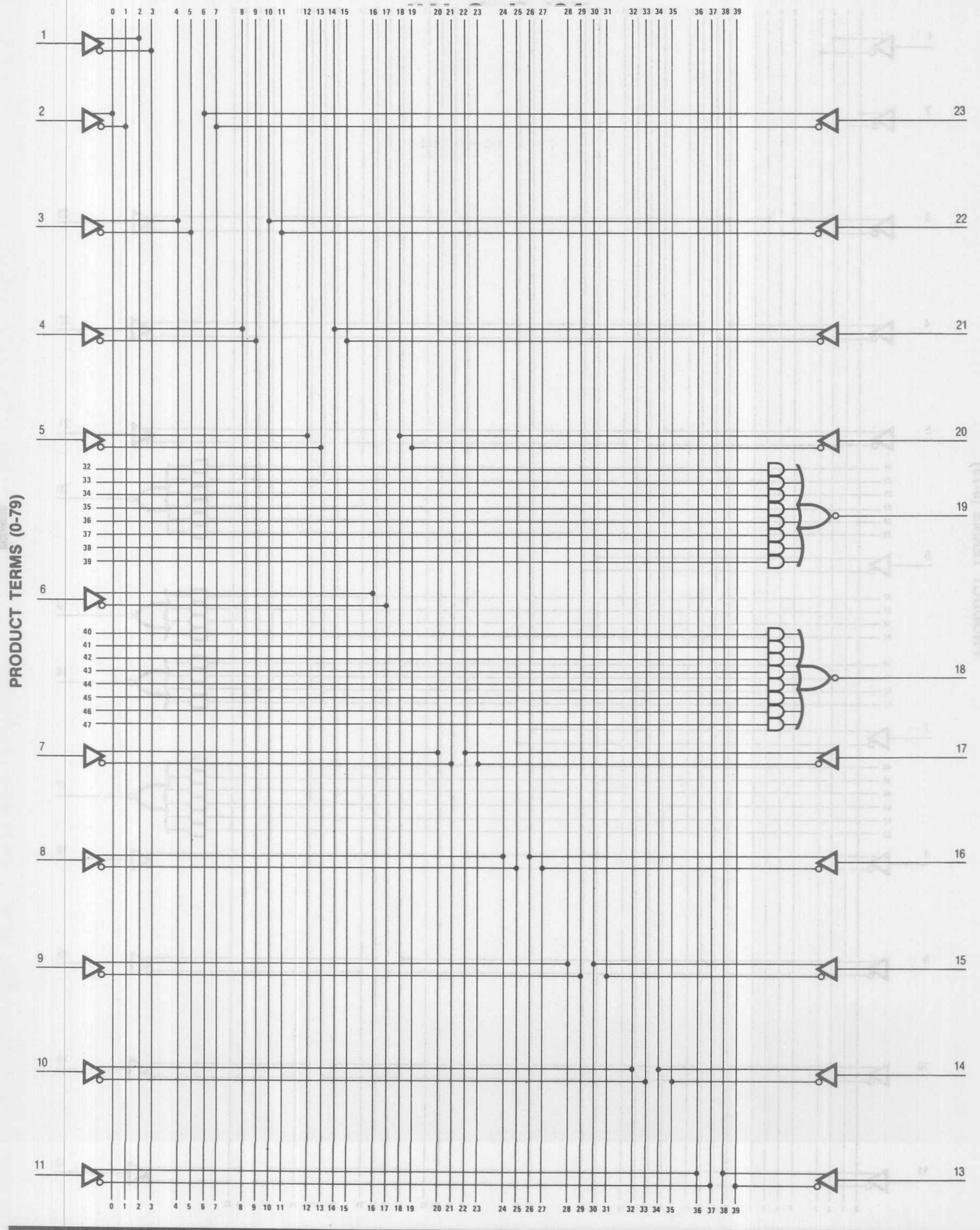


Logic Diagram HAL16L6



Logic Diagram HAL18L4




PRODUCT TERMS (0-79)
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
1
2
3
4
5
6
7
8
9
10
11
23
22
21
20
19
18
17
16
15
14
13
32
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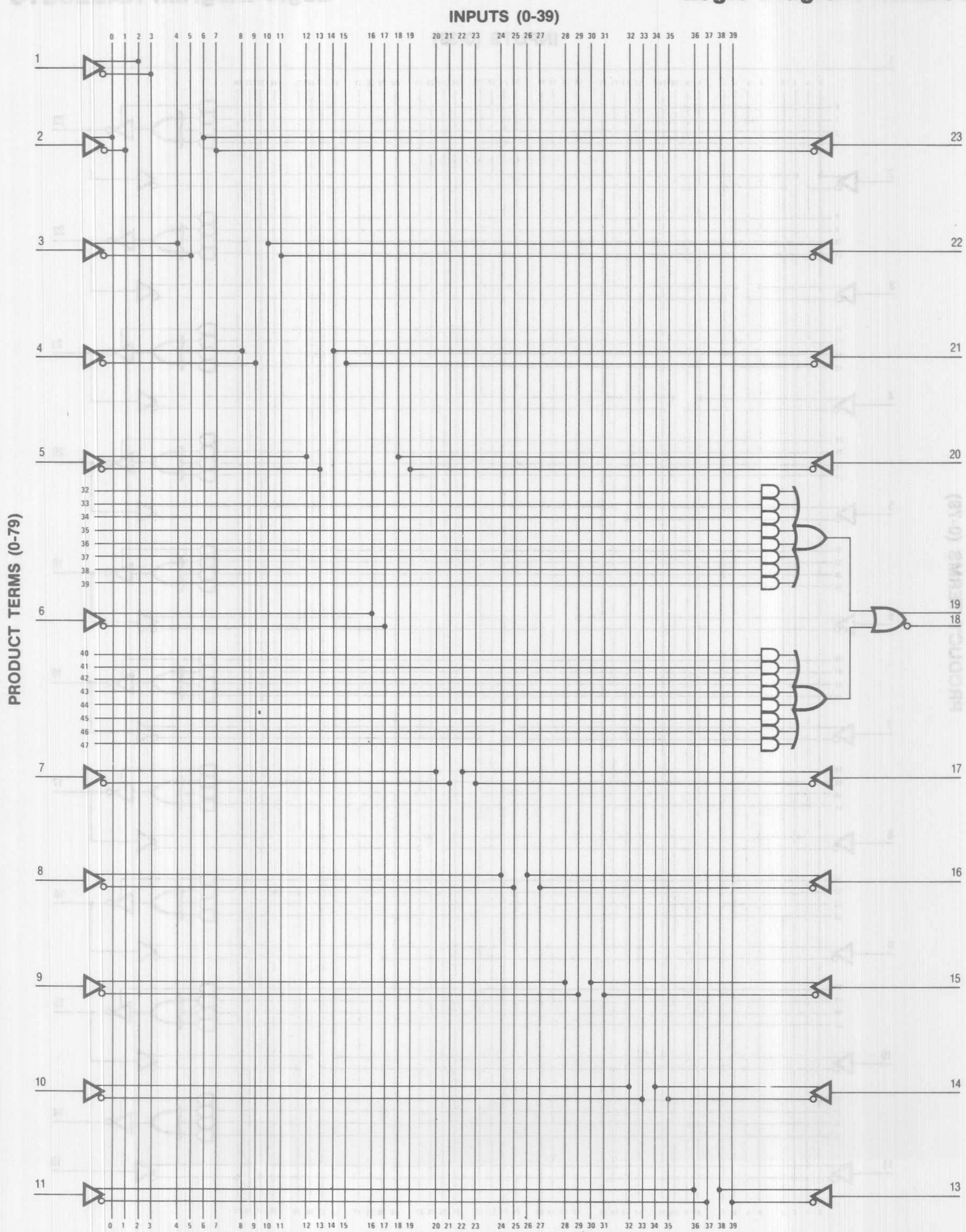
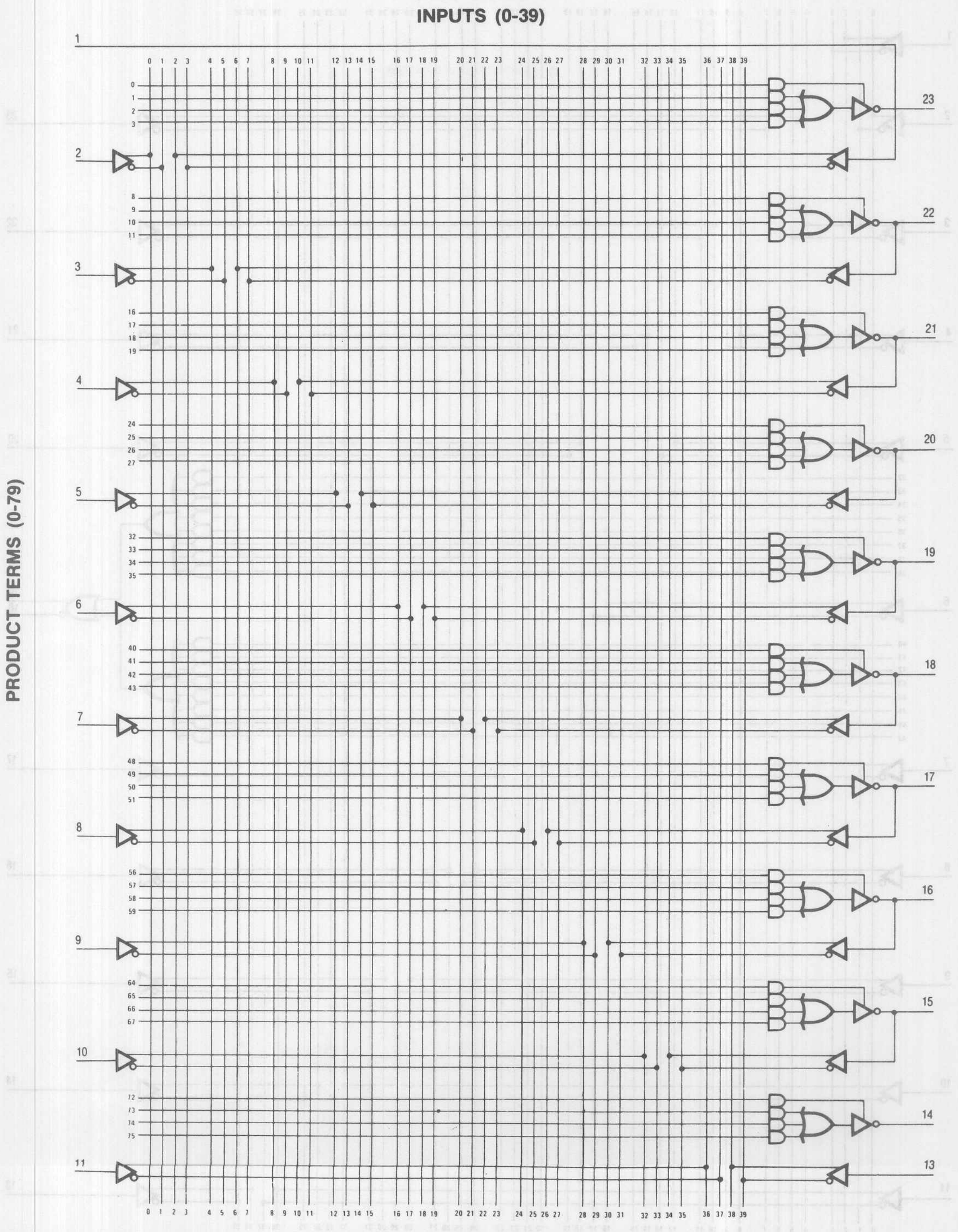
47

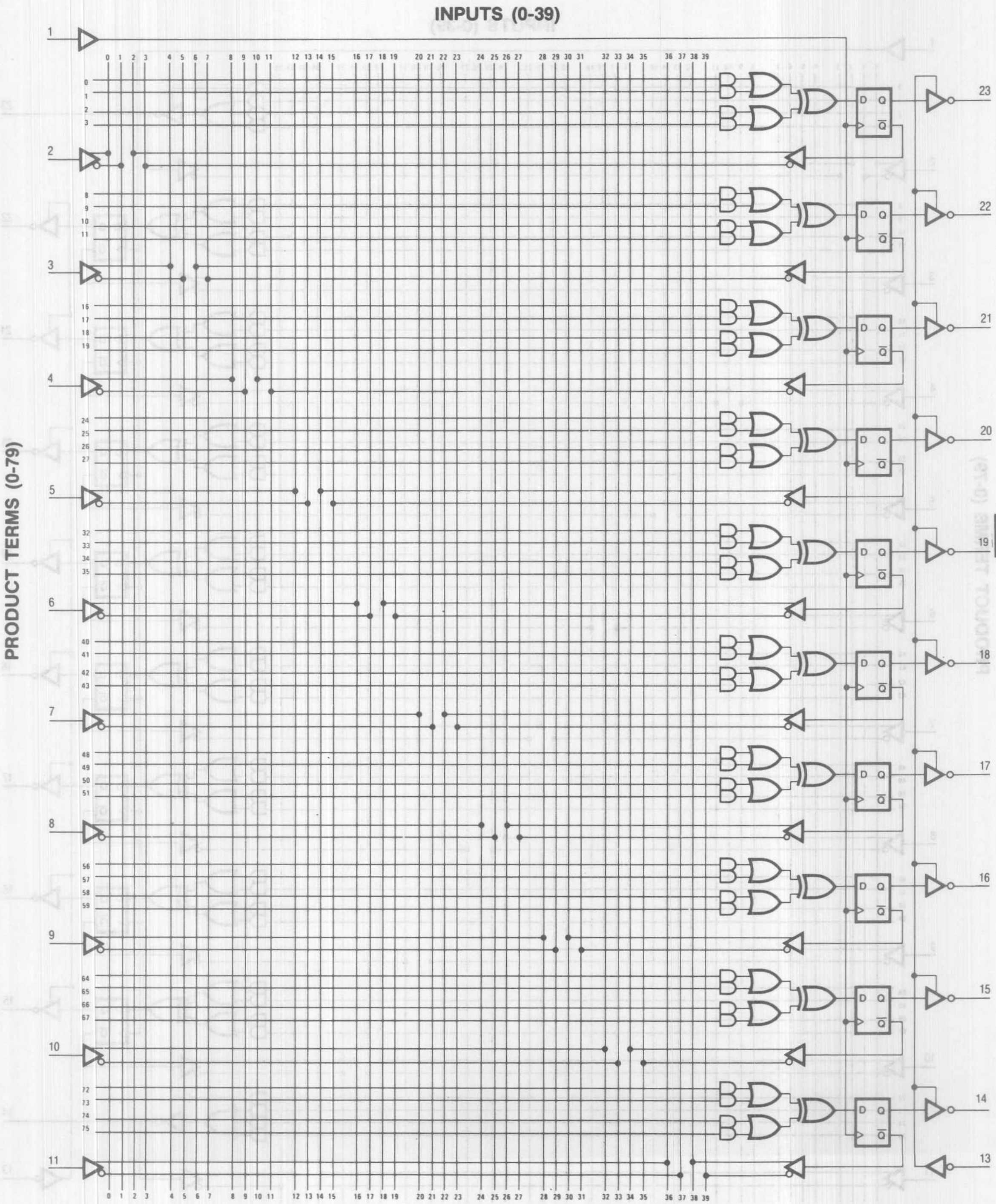
Logic Diagram HAL20C1

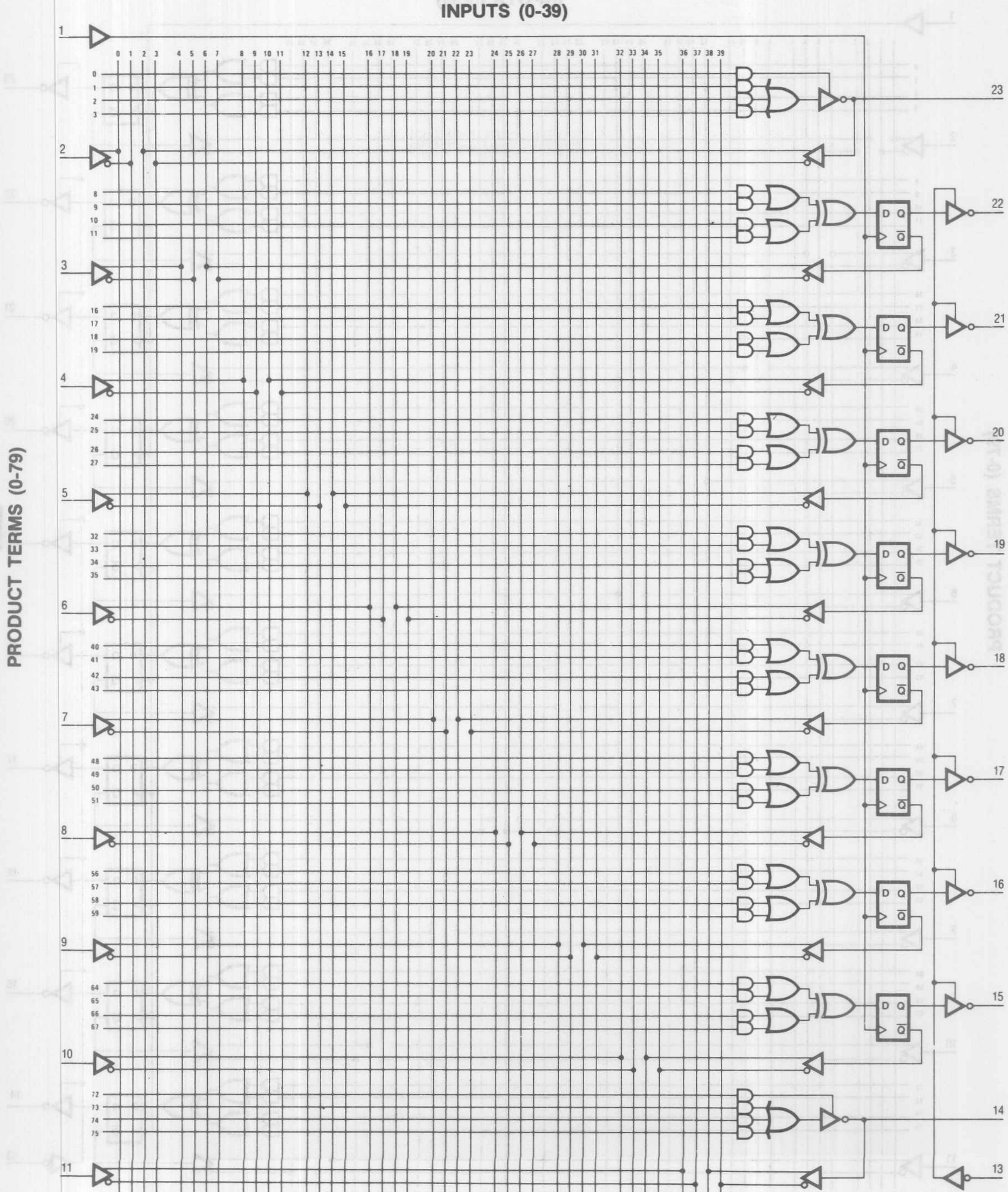


Logic Diagram HAL20L10

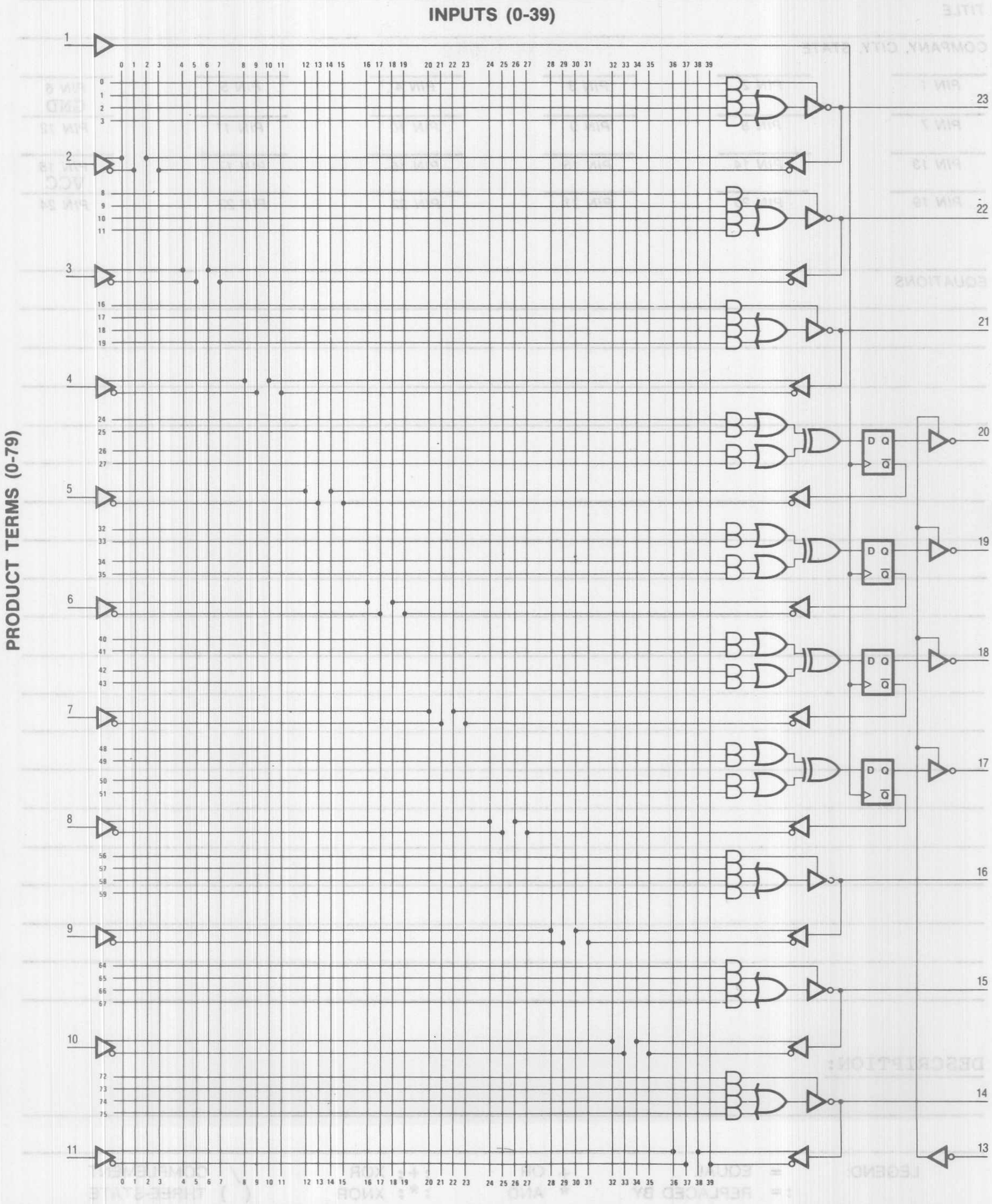


Logic Diagram HAL20X10




INPUTS (0-39)
PRODUCT TERMS (0-79)
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
1
2
3
4
5
6
7
8
9
10
11
23
22
21
20
19
18
17
16
15
14
13
D Q

Logic Diagram HAL20X4



7

HAL

PART NUMBER

HAL DESIGN SPECIFICATION

USER'S PART NUMBER | REV | NAME | DATE / /

TITLE

COMPANY, CITY, STATE

PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6
					GND
PIN 7	PIN 8	PIN 9	PIN 10	PIN 11	PIN 12
PIN 13	PIN 14	PIN 15	PIN 16	PIN 17	PIN 18
					VCC
PIN 19	PIN 20	PIN 21	PIN 22	PIN 23	PIN 24

EQUATIONS

DESCRIPTION:

LEGEND:				
	= EQUAL	+ OR	:+: XOR	/ COMPLEMENT
	:= REPLACED BY	* AND	:*: XNOR	( ) THREE-STATE

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FUNCTION TABLE

PIN A	PIN B	PIN C	PIN D	PIN E	PIN F
PIN G	PIN H	PIN I	PIN J	PIN K	PIN L
PIN M	PIN N	PIN O	PIN P	PIN Q	PIN R
PIN S	PIN T	PIN U	PIN V		

;
COMMENT

; A B C D E F G H I J K L M N O P Q R S T U V COMMENT

LEGEND: H HIGH C CLOCK Z OFF
L LOW X IRRELEVANT

F 107

FUNCTION	PART NUMBER	PAGE	APPENDIX INFORMATION
Octal counter	SN54/74LS461	8-4	8-34
Octal shift register	SN54/74LS498	8-8	8-40
Multifunction register	SN54/74LS380	8-12	8-44
10-bit counter	SN54/74LS491	8-16	8-50
16:1 Mux	SN54/74LS450	8-20	8-54
Dual 8:1 Mux	SN54/74LS451	8-24	8-60
Quad 4:1 Mux	SN54/74LS453	8-28	8-66

Octal Counter
SN54/74LS461

Features/Benefits

- Octal counter for microprogram-counter, DMA controller and general purpose counting applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin Skinny DIP® saves space
- 3-state outputs drive bus lines
- Low current PNP inputs reduce loading
- Expandable in 8-bit increments

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54LS461	JS	MIL
SN74LS461	NS, JS	COM

Description

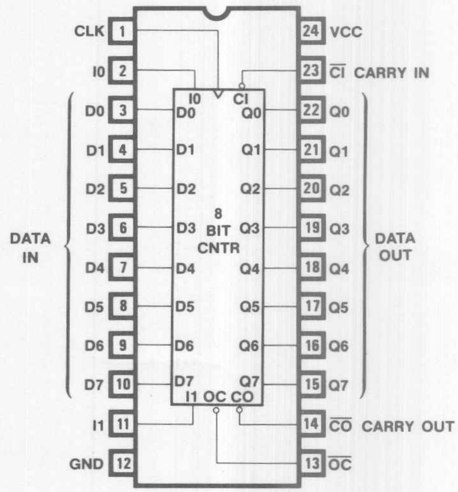
The LS461 is an 8-bit synchronous counter with parallel load, clear, and hold capability. Two function select inputs (I_0, I_1) provide one of four operations which occur synchronously on the rising edge of the clock (CLK).

The LOAD operation loads the inputs (D_7–D_0) into the output register (Q_7–Q_0). The CLEAR operation resets the output register to all LOWs. The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE ($\overline{CI}$ = LOW), otherwise the operation is a HOLD. The carry-out ($\overline{CO}$) is TRUE ($\overline{CO}$ = LOW) when the output register (Q_7–Q_0) is all HIGHs, otherwise FALSE ($\overline{CO}$ = HIGH).

The output register (Q_7–Q_0) is enabled when OC is LOW, and disabled (HI-Z) when $\overline{OC}$ is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

Two or more LS461 octal counters may be cascaded to provide larger counters. The operation codes were chosen such that when I_1 is HIGH, I_0 may be used to select between LOAD and INCREMENT as in a program counter (JUMP/INCREMENT).

Logic Symbol

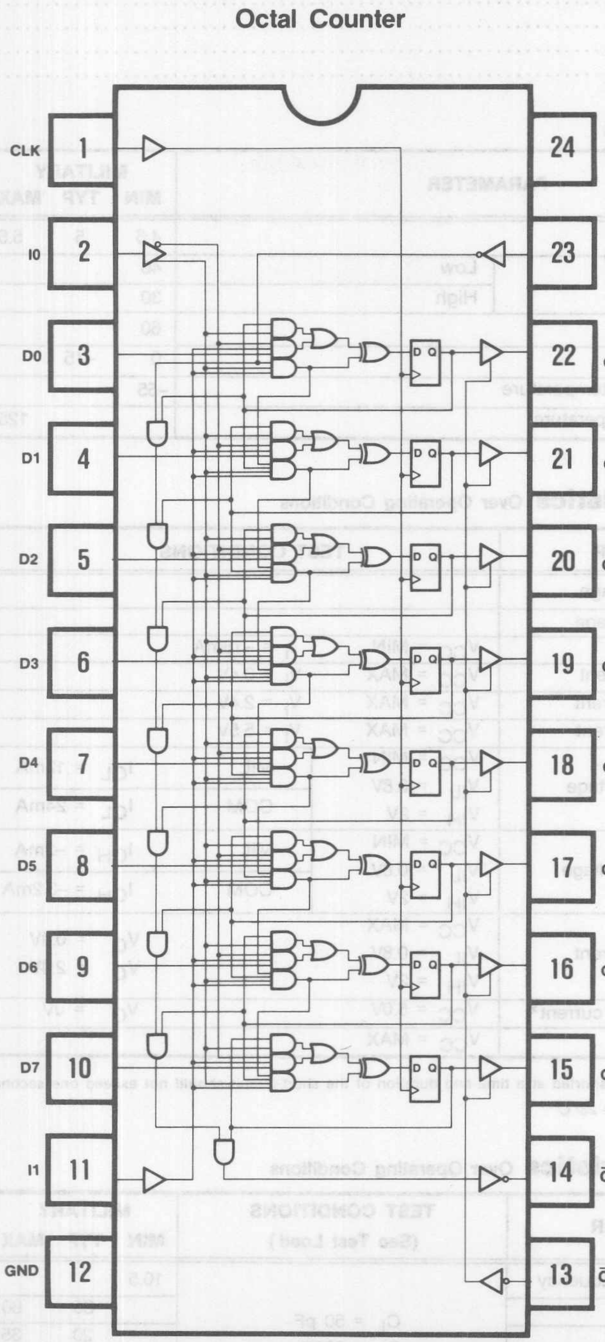


Function Table

$\overline{OC}$	CLK	I_1	I_0	$\overline{CI}$	D_7–D_0	Q_7–Q_0	OPERATION
H	X	X	X	X	X	Z	HI-Z
L	↑	L	L	X	X	L	CLEAR
L	↑	L	H	X	X	Q	HOLD
L	↑	H	L	X	D	D	LOAD
L	↑	H	H	H	X	Q	HOLD
L	↑	H	H	L	X	Q plus 1	INCREMENT

For supplementary information, see appendix, this section.

Logic Diagram



Absolute Maximum Ratings

Supply voltage V_{CC}	7V
Input voltage	5.5V
Off-state output voltage	5.5V
Storage temperature	–65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	40			35			ns
		High	30			25			
t_{su}	Set up time		60			50			ns
t_h	Hold time		0	–15		0	–15		
T_A	Operating free-air temperature		–55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA				–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL	I_{OL} = 12mA			0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL	I_{OH} = –2mA	2.4			V
			COM	I_{OH} = –3.2mA				
I_{OZL}	Off-state output current	V_{CC} = MAX V_{IL} = 0.8V V_{IH} = 2V		V_O = 0.4V			–100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V		V_O = 0V	–30		–130	mA
I_{CC}	Supply current	V_{CC} = MAX				120	180	mA

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

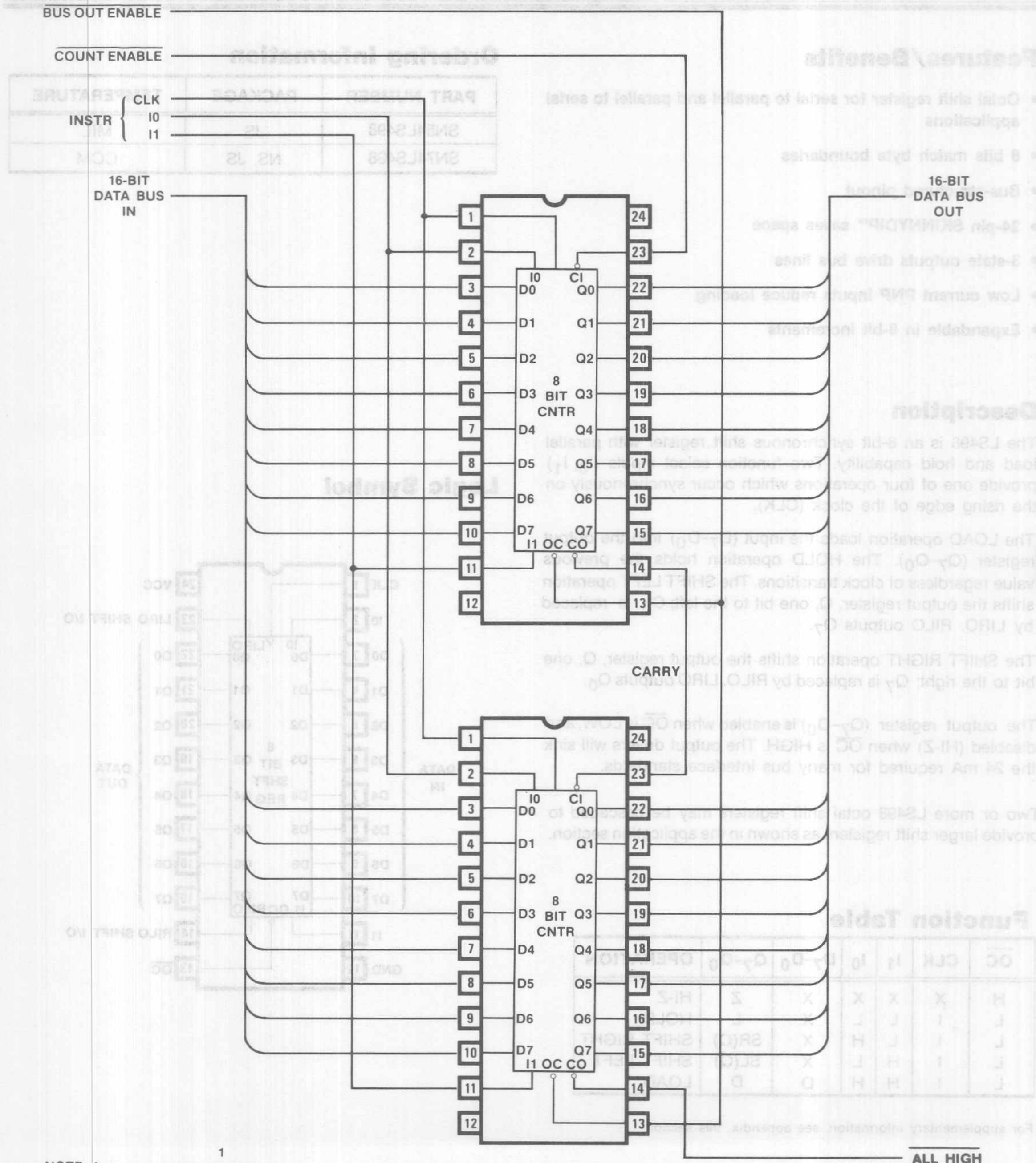
† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 50 pF R_1 = 200Ω R_2 = 390Ω	10.5			12.5			MHz
t_{PD}	$\overline{CI}$ to $\overline{CO}$ delay			35	60		35	50	ns
t_{PD}	Clock to Q			20	35		20	30	ns
t_{PD}	Clock to $\overline{CO}$			55	95		55	80	ns
t_{PZX}	Output enable delay			35	55		35	45	ns
t_{PXZ}	Output disable delay			35	55		35	45	ns

Application

16-Bit Counter



NOTE: $f_{MAX} = \frac{1}{t_{PD\ CLK\ TO\ CO} + t_{SU}}$

Octal Shift Register
SN54/74LS498

Features/Benefits

- Octal shift register for serial to parallel and parallel to serial applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP™ saves space
- 3-state outputs drive bus lines
- Low current PNP inputs reduce loading
- Expandable in 8-bit increments

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54LS498	JS	MIL
SN74LS498	NS, JS	COM

Description

The LS498 is an 8-bit synchronous shift register with parallel load and hold capability. Two function select inputs (I_0, I_1) provide one of four operations which occur synchronously on the rising edge of the clock (CLK).

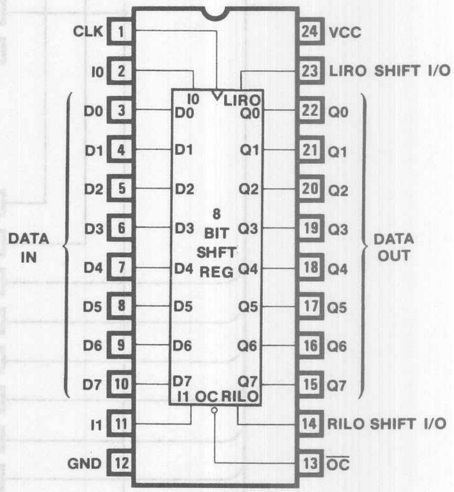
The LOAD operation loads the input (D_7–D_0) into the output register (Q_7–Q_0). The HOLD operation holds the previous value regardless of clock transitions. The SHIFT LEFT operation shifts the output register, Q, one bit to the left; Q_0 is replaced by LIRO. RILO outputs Q_7.

The SHIFT RIGHT operation shifts the output register, Q, one bit to the right; Q_7 is replaced by RILO. LIRO outputs Q_0.

The output register (Q_7–Q_0) is enabled when $\overline{OC}$ is LOW, and disabled (HI-Z) when $\overline{OC}$ is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

Two or more LS498 octal shift registers may be cascaded to provide larger shift registers as shown in the application section.

Logic Symbol



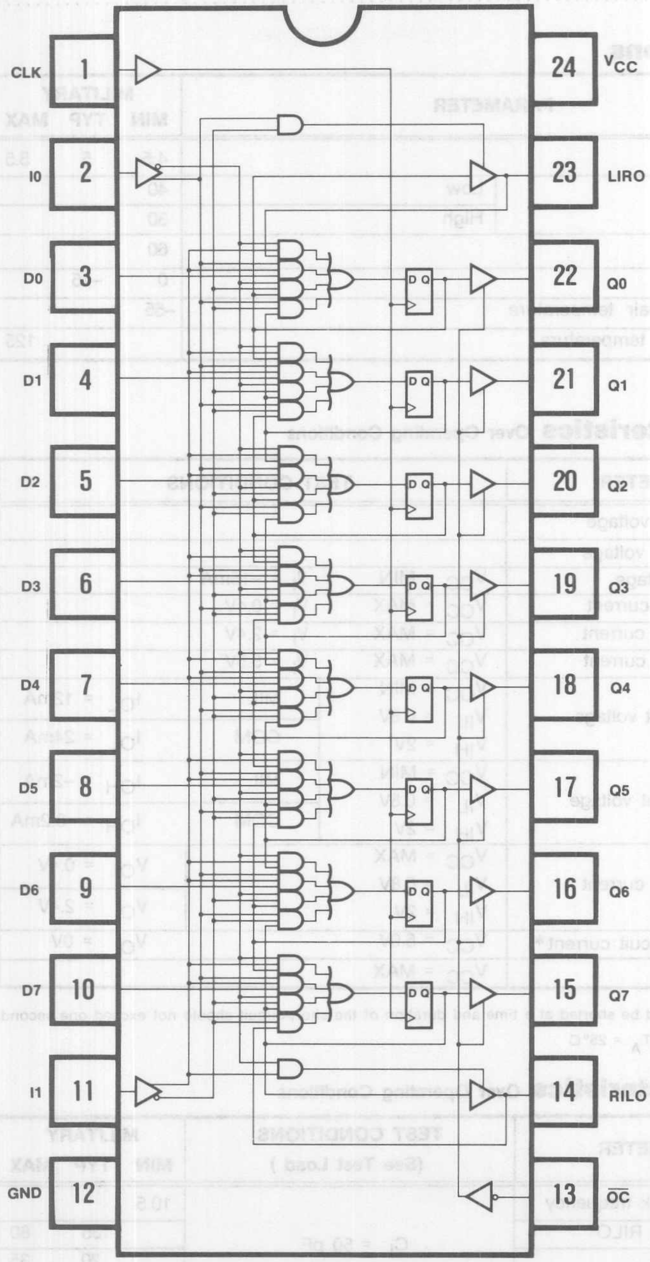
Function Table

$\overline{OC}$	CLK	I_1	I_0	D_7–D_0	Q_7–Q_0	OPERATION
H	X	X	X	X	Z	HI-Z
L	↑	L	L	X	L	HOLD
L	↑	L	H	X	SR(Q)	SHIFT RIGHT
L	↑	H	L	X	SL(Q)	SHIFT LEFT
L	↑	H	H	D	D	LOAD

For supplementary information, see appendix, this section.

Logic Diagram

Octal Shift Register



8

Absolute Maximum Ratings

Supply voltage V_{CC} 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	40			35			ns
		High	30			25			
t_{su}	Set up time		60			50			ns
t_h	Hold time		0	−15		0	−15		
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OL} = 12mA			0.5	V
			COM I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OH} = −2mA	2.4			V
			COM I_{OH} = −3.2mA				
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.4V			−100	μA
I_{OZH}			V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V	V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX			120	180	mA

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

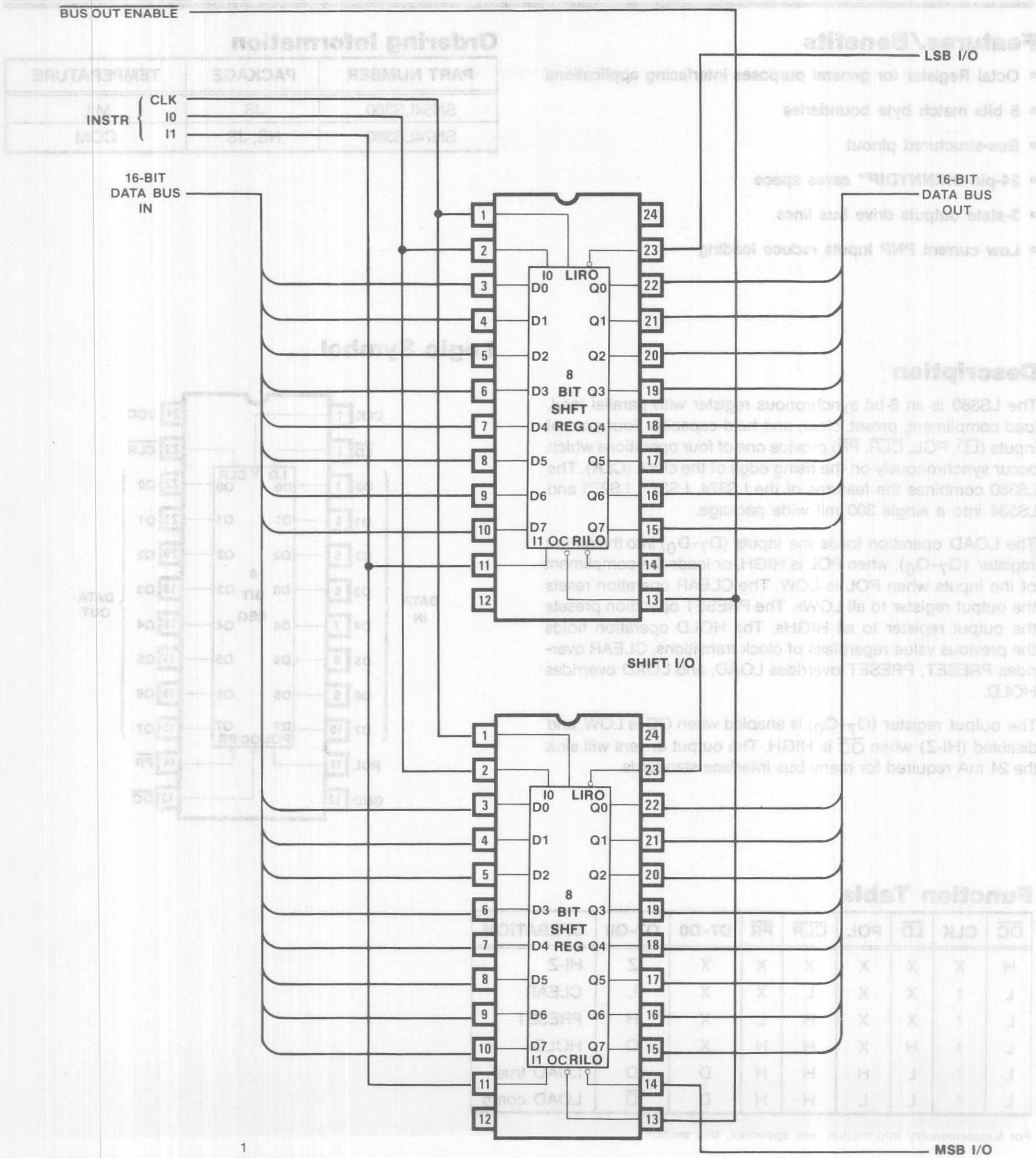
† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 50 pF, R_1 = 200Ω, R_2 = 390Ω	10.5			12.5			MHz
t_{PD}	I0, I1 to LIRO, RILO			35	60		35	50	ns
t_{PD}	Clock to Q			20	35		20	30	ns
t_{PD}	Clock to LIRO, RILO			55	95		55	80	ns
t_{PZX}	Output enable delay			35	55		35	45	ns
t_{PXZ}	Output disable delay			35	55		35	45	ns

Application

16-Bit Shift Register



NOTE: $f_{MAX} = \dfrac{1}{t_{PD\ CLK\ TO\ LIRO} + t_{SU}}$

8

Multifunction Octal Register

SN54/74LS380

Features/Benefits

- Octal Register for general purposes interfacing applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP™ saves space
- 3-state outputs drive bus lines
- Low current PNP inputs reduce loading

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54LS380	JS	MIL
SN74LS380	NS, JS	COM

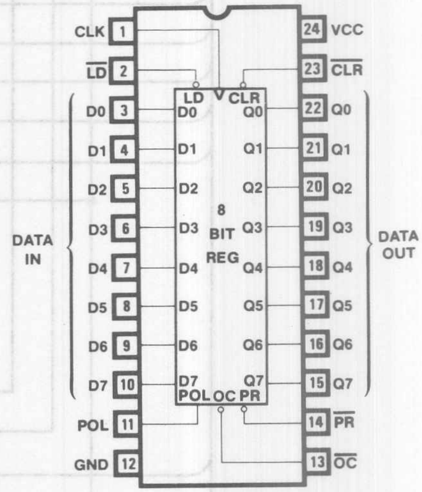
Description

The LS380 is an 8-bit synchronous register with parallel load, load compliment, preset, clear, and hold capacity. Four control inputs ($\overline{LD}$, POL, $\overline{CLR}$, $\overline{PR}$) provide one of four operations which occur synchronously on the rising edge of the clock (CLK). The LS380 combines the features of the LS374, LS377, LS273 and LS534 into a single 300 mil wide package.

The LOAD operation loads the inputs (D_7-D_0) into the output register (Q_7-Q_0), when POL is HIGH, or loads the compliment of the inputs when POL is LOW. The CLEAR operation resets the output register to all LOWs. The PRESET operation presets the output register to all HIGHs. The HOLD operation holds the previous value regardless of clock transitions. CLEAR overrides PRESET, PRESET overrides LOAD, and LOAD overrides HOLD.

The output register (Q_7-Q_0) is enabled when OC is LOW, and disabled (HI-Z) when $\overline{OC}$ is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

Logic Symbol

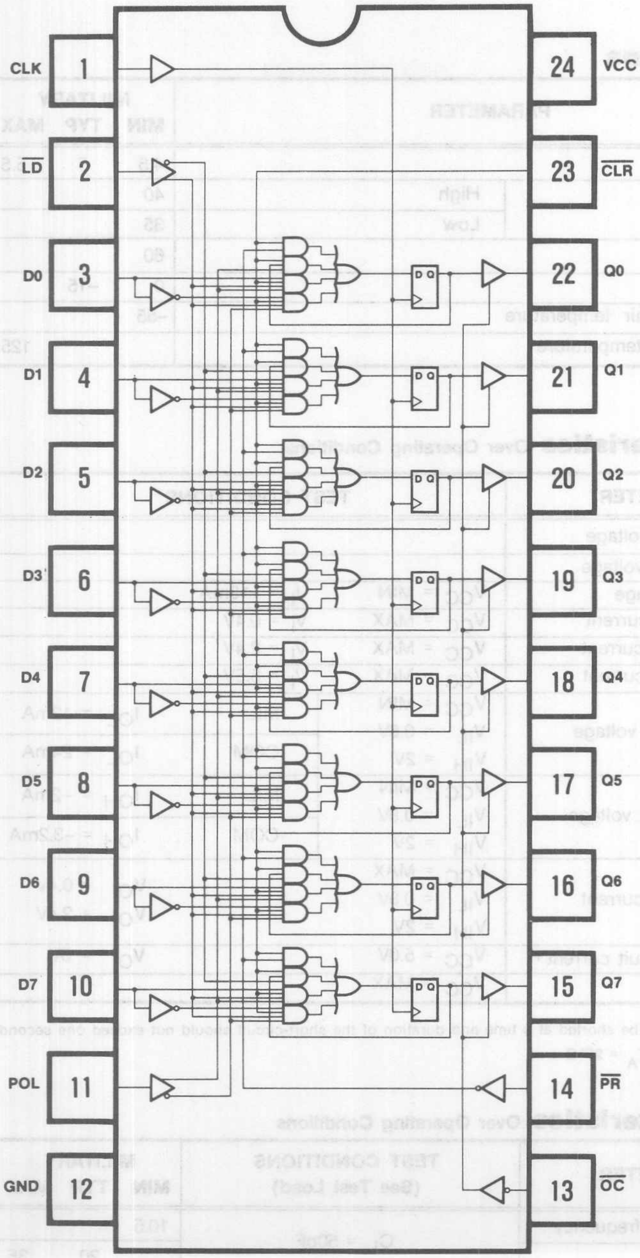


Function Table

$\overline{OC}$	CLK	$\overline{LD}$	POL	$\overline{CLR}$	$\overline{PR}$	D7-D0	Q7-Q0	OPERATION
H	X	X	X	X	X	X	Z	HI-Z
L	↑	X	X	L	X	X	L	CLEAR
L	↑	X	X	H	L	X	H	PRESET
L	↑	H	X	H	H	X	Q	HOLD
L	↑	L	H	H	H	D	D	LOAD true
L	↑	L	L	H	H	D	$\overline{D}$	LOAD comp

For supplementary information, see appendix, this section.

Octal Register



8

Absolute Maximum Ratings

Supply voltage V_{CC} 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	High	40			40			ns
		Low	35			35			
t_{su}	Set up time		60			50			ns
t_h	Hold time		0	−15		0	−15		
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OL} = 12mA			0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OH} = −2mA	2.4			V
			COM	I_{OH} = −3.2mA				
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V		V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V		V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX				120	180	mA

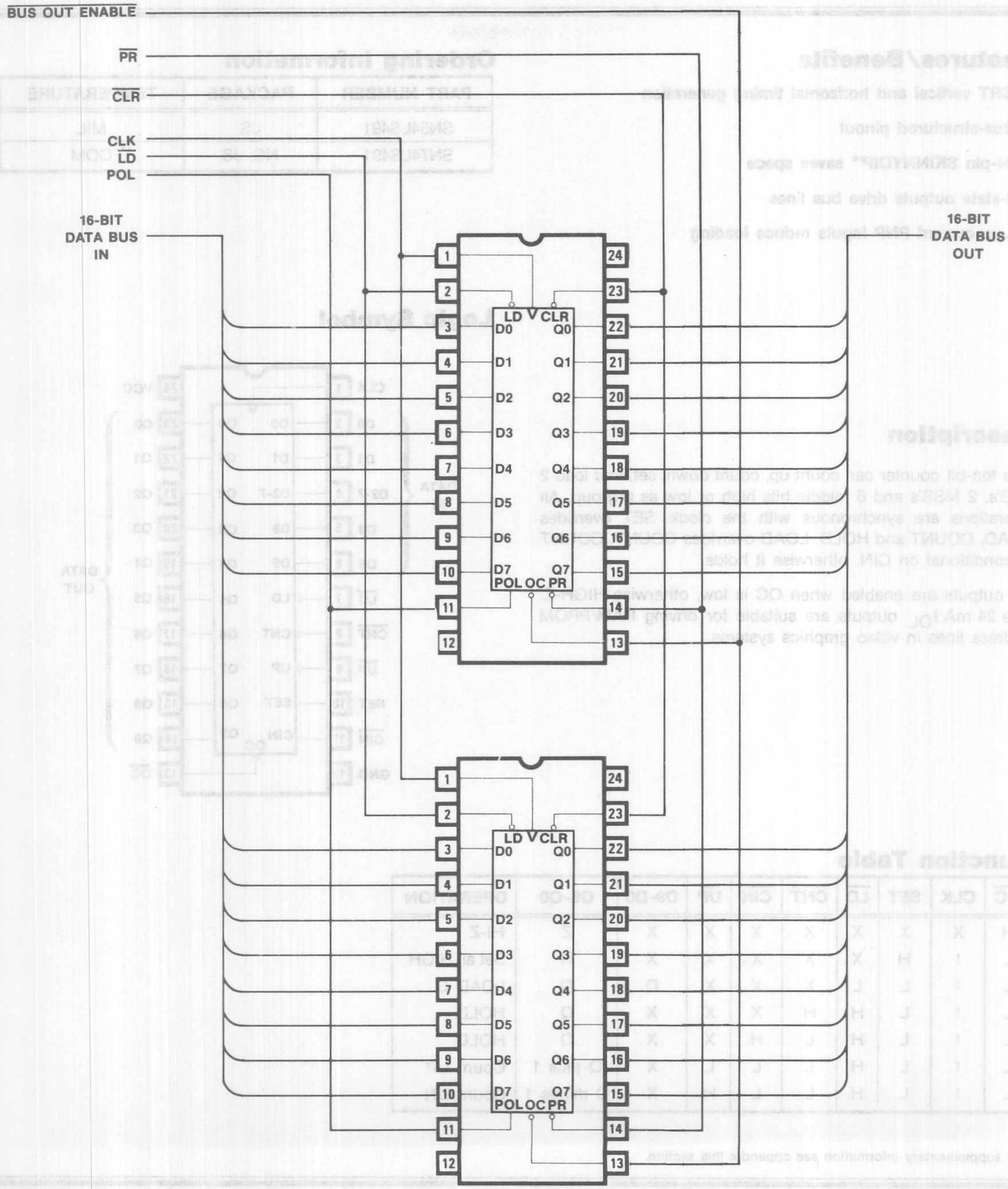
* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 50pF, R_1 = 200Ω, R_2 = 390Ω	10.5			12.5			MHz
t_{PD}	Clock to Q			20	35		20	30	ns
t_{PZX}	Output enable delay			35	55		35	45	ns
t_{PXZ}	Output disable delay			35	55		35	45	ns

Application

16-Bit Register



10-Bit Counter
SN54/74LS491

Features/Benefits

- CRT vertical and horizontal timing generation
- Bus-structured pinout
- 24-pin SKINNYDIP™ saves space
- 3-state outputs drive bus lines
- Low current PNP inputs reduce loading

Ordering Information

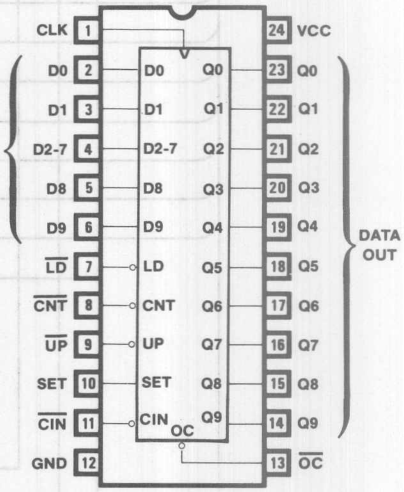
PART NUMBER	PACKAGE	TEMPERATURE
SN54LS491	JS	MIL
SN74LS491	NS, JS	COM

Description

The ten-bit counter can count up, count down, set, and load 2 LSB's, 2 MSB's and 6 middle bits high or low as a group. All operations are synchronous with the clock. SET overrides LOAD, COUNT and HOLD. LOAD overrides COUNT. COUNT is conditional on CIN, otherwise it holds.

All outputs are enabled when OC is low, otherwise HIGH-Z. The 24 mA I_{OL} outputs are suitable for driving RAM/PROM address lines in video graphics systems.

Logic Symbol



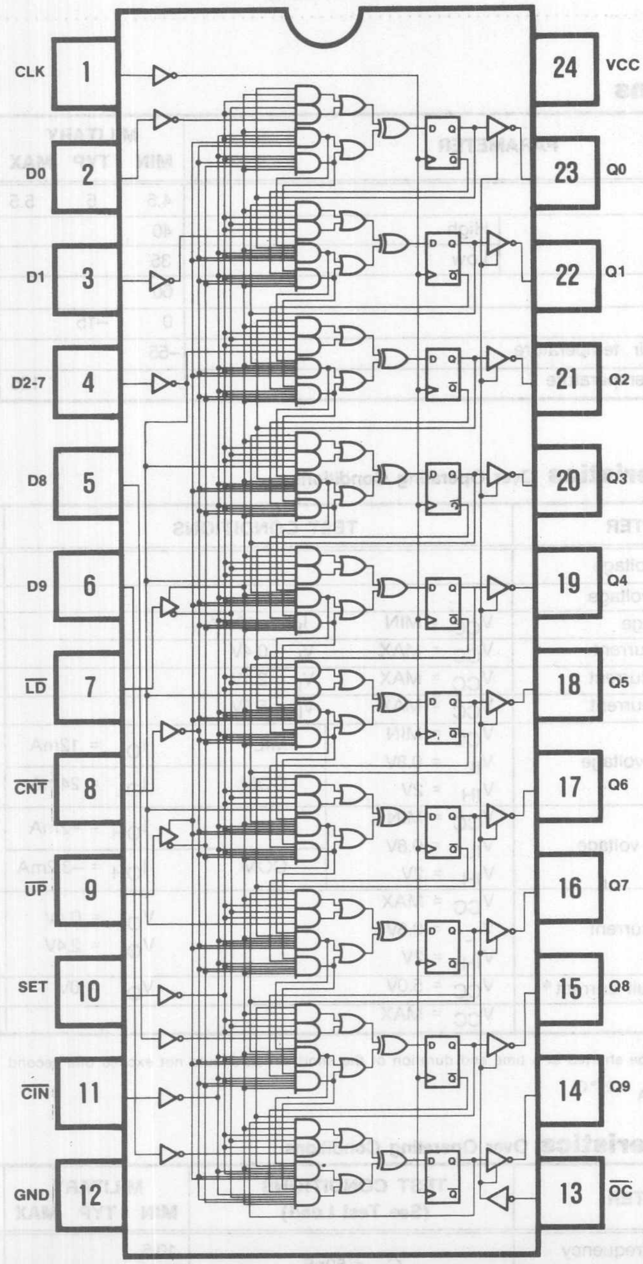
Function Table

$\overline{OC}$	CLK	SET	$\overline{LD}$	$\overline{CNT}$	$\overline{CIN}$	$\overline{UP}$	D9–D0	Q9–Q0	OPERATION
H	X	X	X	X	X	X	X	Z	HI-Z
L	↑	H	X	X	X	X	X	H	Set all HIGH
L	↑	L	L	X	X	X	D	D	LOAD D
L	↑	L	H	H	X	X	X	Q	HOLD
L	↑	L	H	L	H	X	X	Q	HOLD
L	↑	L	H	L	L	L	X	Q plus 1	Count UP
L	↑	L	H	L	L	H	X	Q minus 1	Count DN

For supplementary information see appendix this section.

Logic Diagram

10-Bit Up/Down Counter



Absolute Maximum Ratings

Supply voltage V_{CC} 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	High	40			40			ns
		Low	35			35			
t_{su}	Set up time		60			50			ns
t_h	Hold time		0	−15		0	−15		
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL COM	I_{OL} = 12mA I_{OL} = 24mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL COM	I_{OH} = −2mA I_{OH} = −3.2mA	2.4			V
I_{OZL} I_{OZH}	Off-state output current	V_{CC} = MAX V_{IL} = 0.8V V_{IH} = 2V		V_O = 0.4V V_O = 2.4V			−100 100	μA μA
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V		V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX				120	180	mA

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

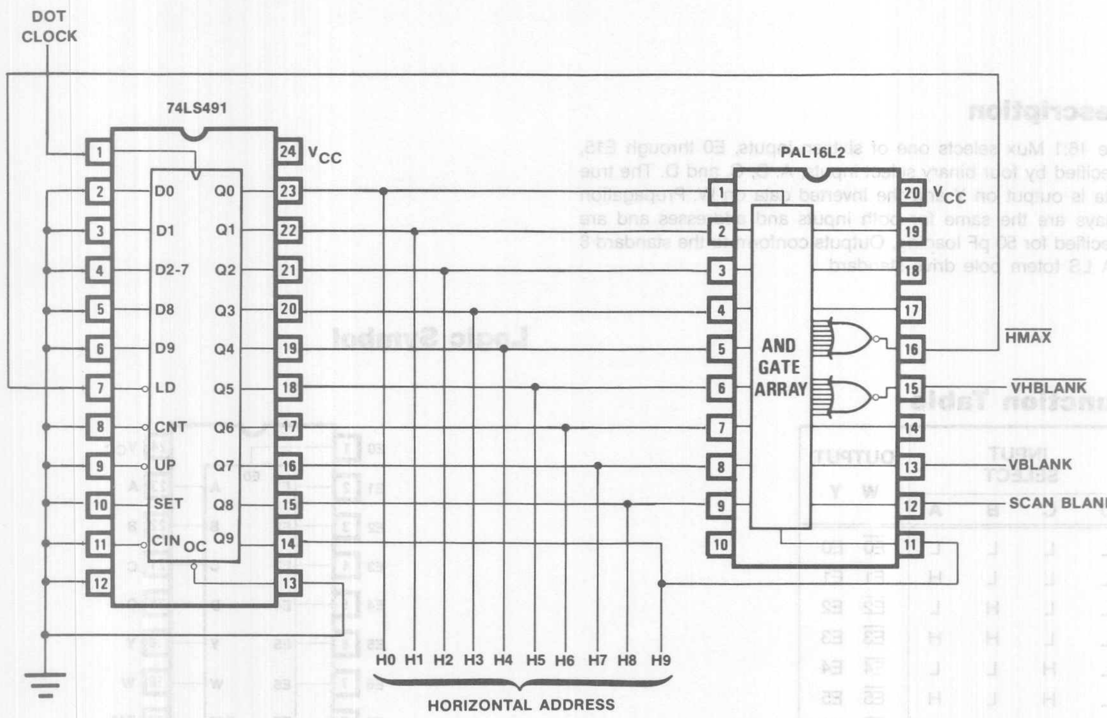
† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 50pF R_1 = 200Ω R_2 = 390Ω	10.5			12.5			MHz
t_{PD}	Clock to Q			20	35		20	30	ns
t_{PZX}	Output enable delay			35	55		35	45	ns
t_{PXZ}	Output disable delay			35	55		35	45	ns

Application

CRT Horizontal Timing and Blanking



16:1 Mux
SN54/74LS450

Features/Benefits

- 24-pin SKINNYDIP™ saves space
- Similar to 74150 (Fat DIP)
- Low current PNP inputs reduce loading

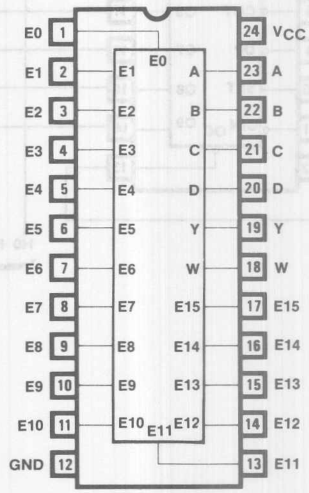
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54LS450	JS	MIL
SN74LS450	NS, JS	COM

Description

The 16:1 Mux selects one of sixteen inputs, E0 through E15, specified by four binary select inputs, A, B, C, and D. The true data is output on Y and the inverted data on W. Propagation delays are the same for both inputs and addresses and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem pole drive standard.

Logic Symbol

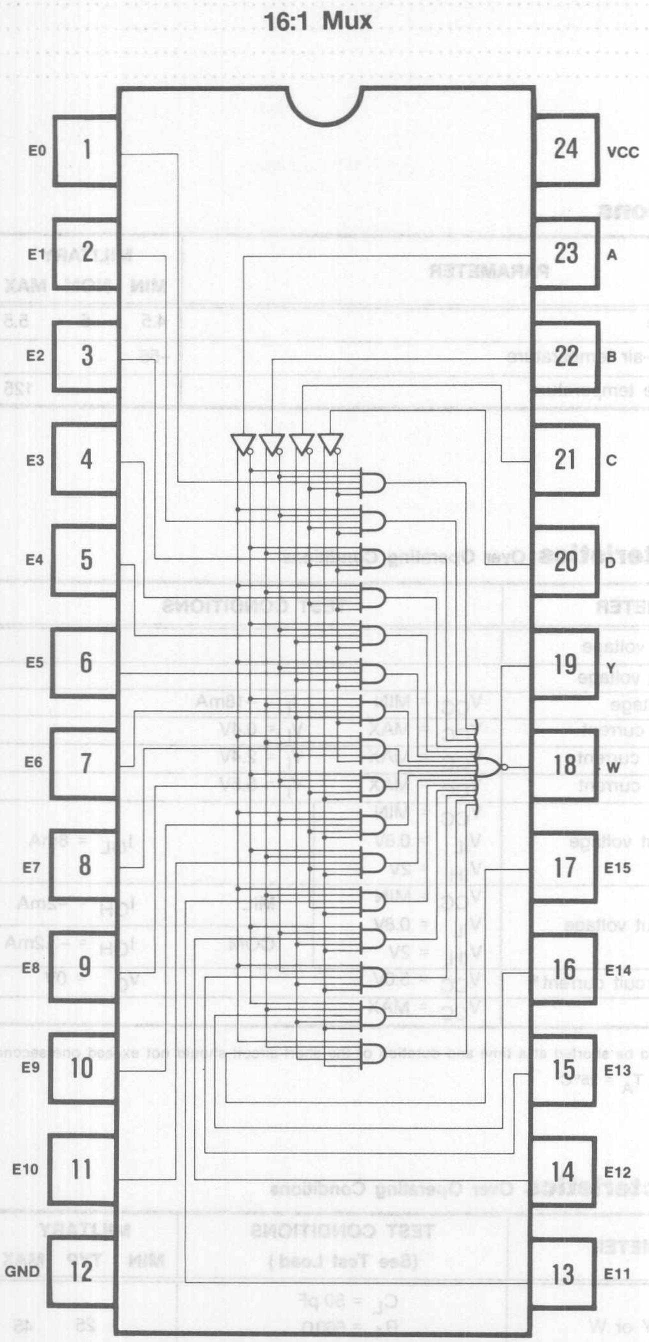


Function Table

INPUT SELECT				OUTPUT	
D	C	B	A	W	Y
L	L	L	L	$\overline{E0}$	E0
L	L	L	H	$\overline{E1}$	E1
L	L	H	L	$\overline{E2}$	E2
L	L	H	H	$\overline{E3}$	E3
L	H	L	L	$\overline{E4}$	E4
L	H	L	H	$\overline{E5}$	E5
L	H	H	L	$\overline{E6}$	E6
L	H	H	H	$\overline{E7}$	E7
H	L	L	L	$\overline{E8}$	E8
H	L	L	H	$\overline{E9}$	E9
H	L	H	L	$\overline{E10}$	E10
H	L	H	H	$\overline{E11}$	E11
H	H	L	L	$\overline{E12}$	E12
H	H	L	H	$\overline{E13}$	E13
H	H	H	L	$\overline{E14}$	E14
H	H	H	H	$\overline{E15}$	E15

For supplementary information, see appendix, this section.

Logic Diagram



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Absolute Maximum Ratings

Supply voltage V_{CC} 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55			0		75	°C
T_C	Operating case temperature			125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX		V_I = 0.4V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V		I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL COM	I_{OH} = −2mA I_{OH} = −3.2mA	2.4			V
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V		V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX				60	100	mA

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

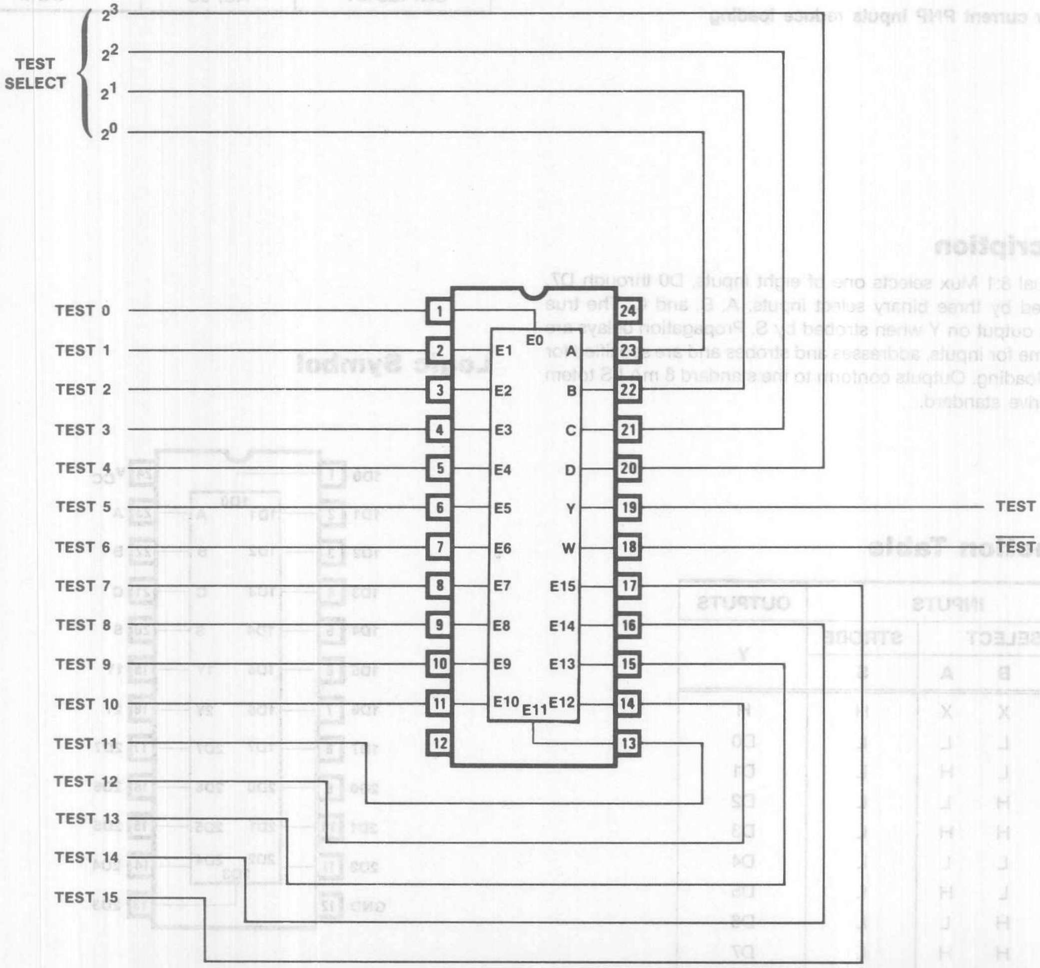
† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Any input to Y or W	C_L = 50 pF R_1 = 560Ω R_2 = 1.1kΩ		25	45		25	40	ns

Application

Test Condition Mux



Dual 8:1 Mux
SN54/74LS451

Features/Benefits

- 24-pin SKINNYDIP™ saves space
- Twice the density of 74LS151
- Low current PNP inputs reduce loading

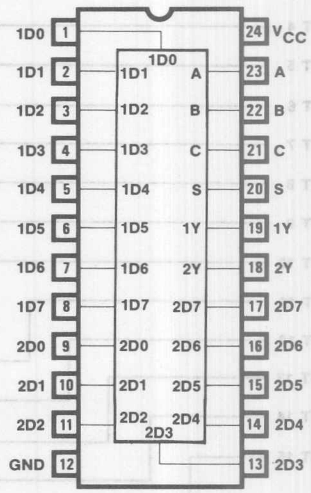
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54LS451	JS	MIL
SN74LS451	NS, JS	COM

Description

The dual 8:1 Mux selects one of eight inputs, D0 through D7, specified by three binary select inputs, A, B, and C. The true data is output on Y when strobed by S. Propagation delays are the same for inputs, addresses and strobes and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem pole drive standard.

Logic Symbol



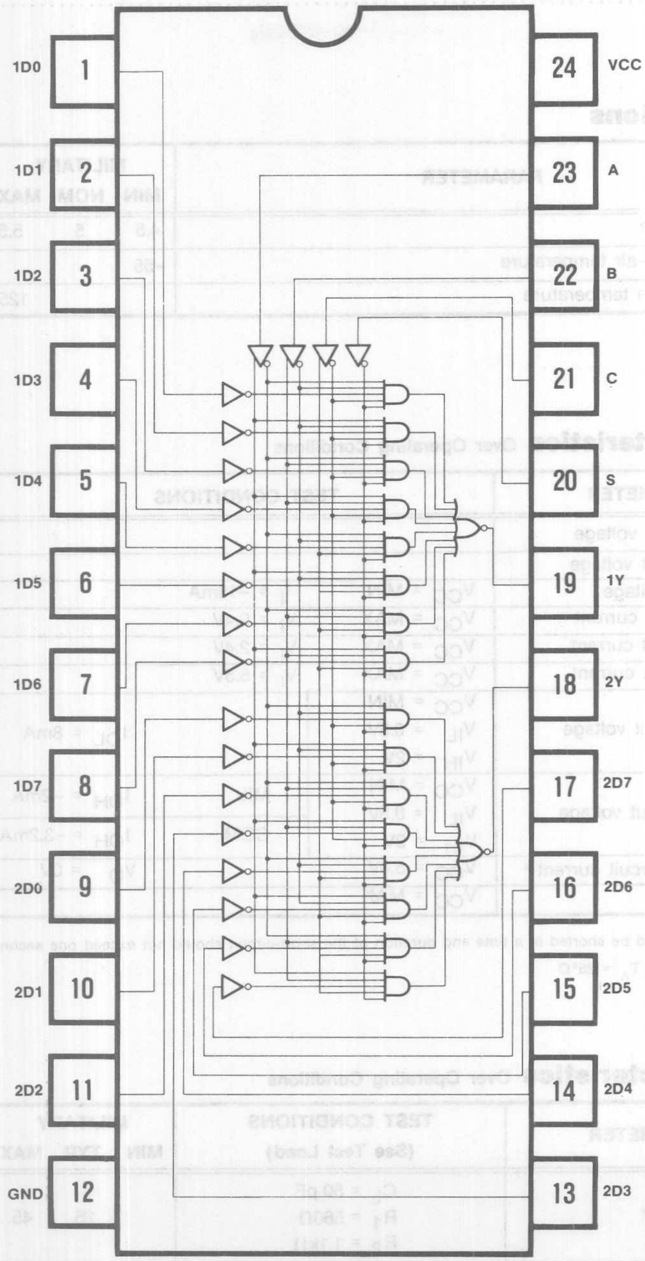
Function Table

INPUTS				OUTPUTS
SELECT			STROBE	Y
C	B	A	S	
X	X	X	H	H
L	L	L	L	D0
L	L	H	L	D1
L	H	L	L	D2
L	H	H	L	D3
H	L	L	L	D4
H	L	H	L	D5
H	H	L	L	D6
H	H	H	L	D7

For supplementary information, see appendix, this section.

Logic Diagram

Dual 8:1 Mux



Absolute Maximum Ratings

Supply voltage V_{CC} 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55			0		75	°C
T_C	Operating case temperature			125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	µA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL: I_{OH} = −2mA; COM: I_{OH} = −3.2mA	2.4			V
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V	V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX			60	100	mA

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

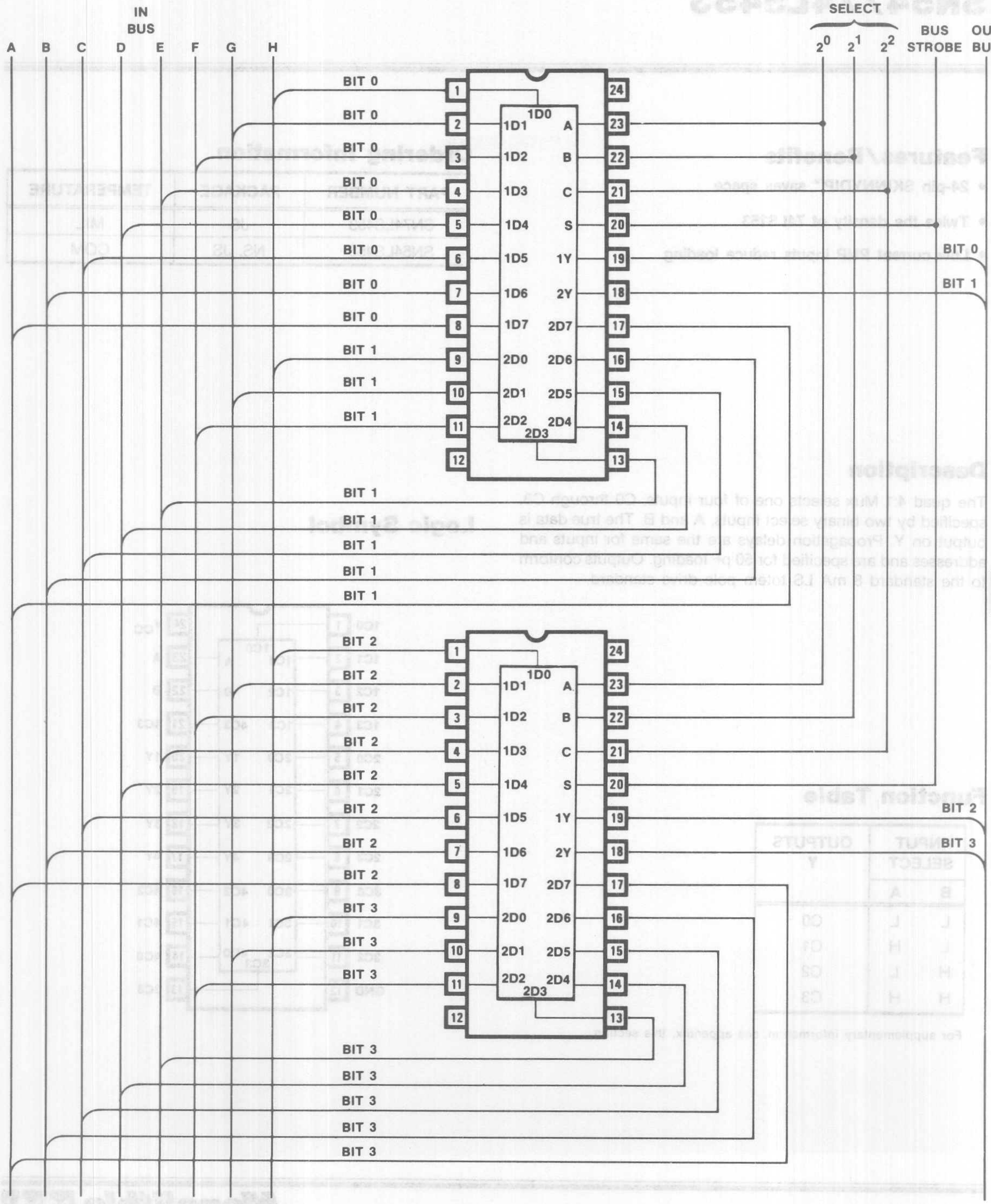
† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Any input to Y	C_L = 50 pF, R_1 = 560Ω, R_2 = 1.1kΩ		25	45		25	40	ns

Application

8:1 Bus Select



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Quad 4:1 Mux
SN54/74LS453

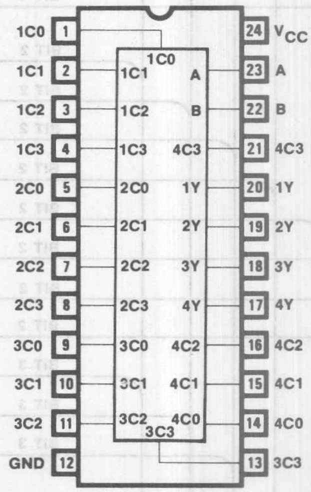
Features/Benefits
- 24-pin SKINNYDIP™ saves space
- Twice the density of 74LS153
- Low current PNP inputs reduce loading

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN74LS453	JS	MIL
SN54LS453	NS, JS	COM

Description
The quad 4:1 Mux selects one of four inputs, C0 through C3, specified by two binary select inputs, A and B. The true data is output on Y. Propagation delays are the same for inputs and addresses and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem pole drive standard.

Logic Symbol



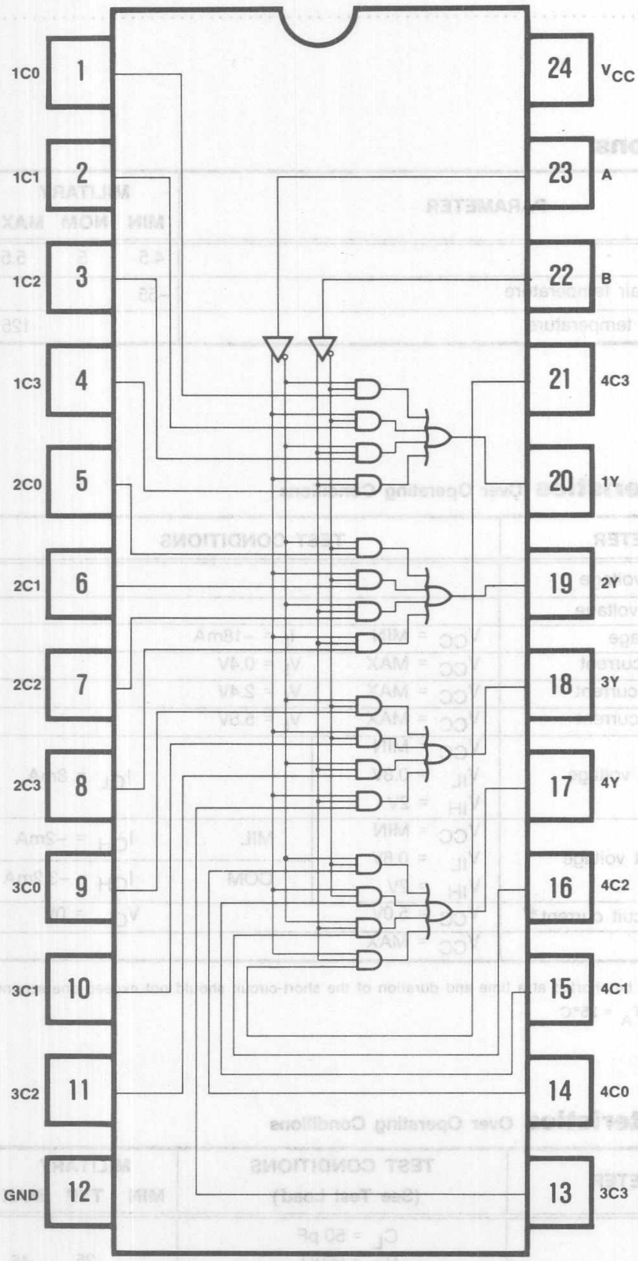
Function Table

INPUT SELECT		OUTPUTS Y
B	A	
L	L	C0
L	H	C1
H	L	C2
H	H	C3

For supplementary information, see appendix, this section.

Logic Diagram

Quad 4:1 Mux



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Absolute Maximum Ratings

Supply voltage V_{CC}	7V
Input voltage	5.5V
Off-state output voltage	5.5V
Storage temperature	−65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55			0		75	°C
T_C	Operating case temperature			125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OH} = −2mA; COM I_{OH} = −3.2mA	2.4			V
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V	V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX			60	100	mA

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

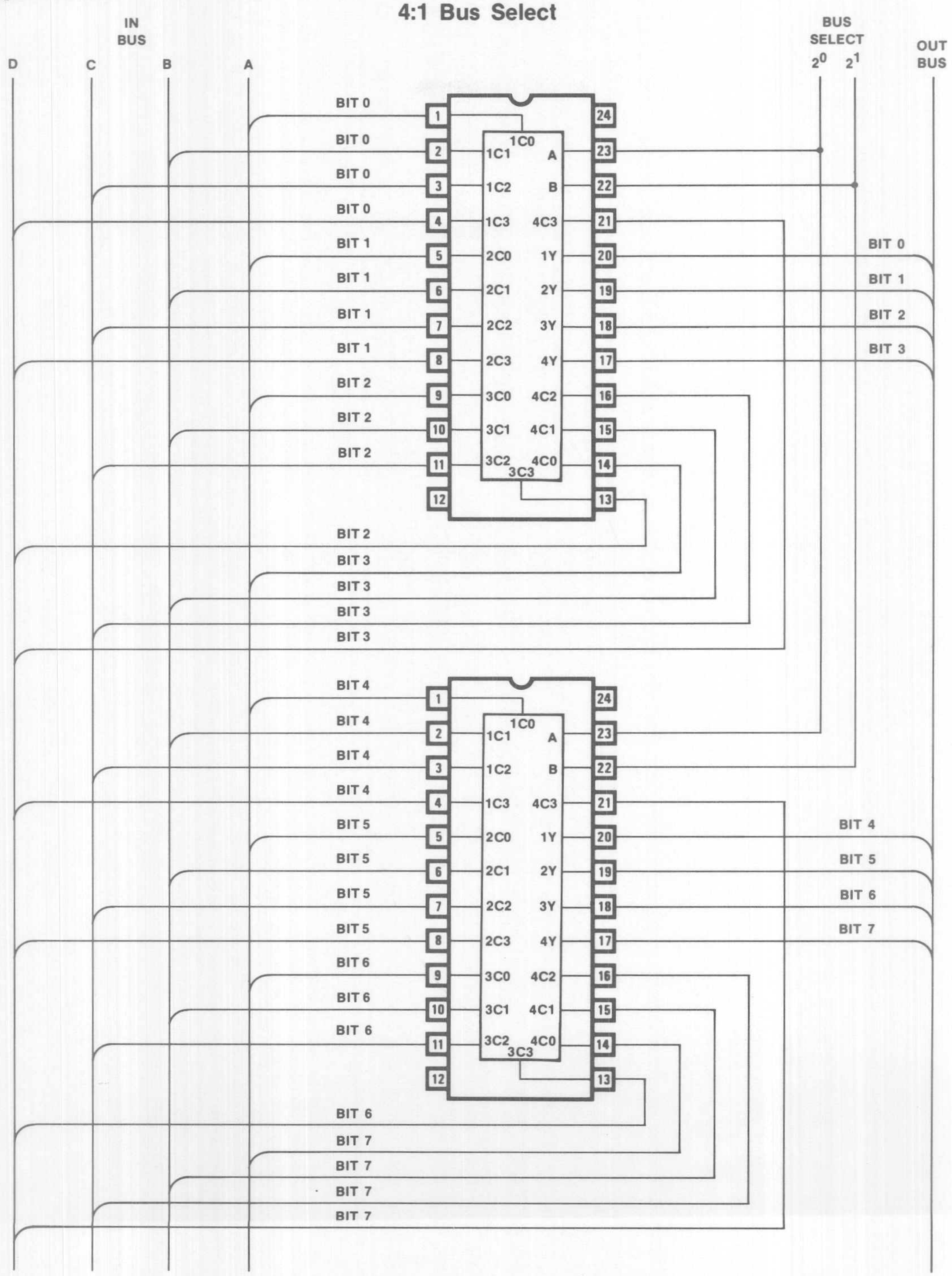
† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Any input to Y	C_L = 50 pF, R_1 = 560Ω, R_2 = 1.1kΩ		25	45		25	40	ns

Application

4:1 Bus Select



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HMSI Appendix

8

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PAL20X8                                          PAL DESIGN SPECIFICATION
P8005 (74LS461)                                  BIRKNER/KAZMI/BLASCO 02/10/81
8-BIT SYNCHRONOUS COUNTER
MMI  SUNNYVALE, CALIFORNIA
CLK I0 D0 D1 D2 D3 D4 D5 D6 D7 I1 GND
/OC /CO Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0 /CI VCC


/Q0 :=  /I1*/I0                                  ;CLEAR LSB
     +        I0 * /Q0                           ;COUNT/HOLD
    :+:  I1*/I0 * /D0                            ;LOAD D0 (LSB)
     +   I1* I0 * CI                             ;COUNT

/Q1 :=  /I1*/I0                                  ;CLEAR
     +        I0 * /Q1                           ;COUNT/HOLD
    :+:  I1*/I0 * /D1                            ;LOAD D1
     +   I1* I0 * CI*Q0                          ;COUNT

/Q2 :=  /I1*/I0                                  ;CLEAR
     +        I0 * /Q2                           ;COUNT/HOLD
    :+:  I1*/I0 * /D2                            ;LOAD D2
     +   I1* I0 * CI*Q0*Q1                       ;COUNT

/Q3 :=  /I1*/I0                                  ;CLEAR
     +        I0 * /Q3                           ;COUNT/HOLD
    :+:  I1*/I0 * /D3                            ;LOAD D3
     +   I1* I0 * CI*Q0*Q1*Q2                    ;COUNT

/Q4 :=  /I1*/I0                                  ;CLEAR
     +        I0 * /Q4                           ;COUNT/HOLD
    :+:  I1*/I0 * /D4                            ;LOAD D4
     +   I1* I0 * CI*Q0*Q1*Q2*Q3                 ;COUNT

/Q5 :=  /I1*/I0                                  ;CLEAR
     +        I0 * /Q5                           ;COUNT/HOLD
    :+:  I1*/I0 * /D5                            ;LOAD D5
     +   I1* I0 * CI*Q0*Q1*Q2*Q3*Q4              ;COUNT

/Q6 :=  /I1*/I0                                  ;CLEAR
     +        I0 * /Q6                           ;COUNT/HOLD
    :+:  I1*/I0 * /D6                            ;LOAD D6
     +   I1* I0 * CI*Q0*Q1*Q2*Q3*Q4*Q5           ;COUNT

/Q7 :=  /I1*/I0                                  ;CLEAR MSB
     +        I0 * /Q7                           ;COUNT/HOLD
    :+:  I1*/I0 * /D7                            ;LOAD D7 (MSB)
     +   I1* I0 * CI*Q0*Q1*Q2*Q3*Q4*Q5*Q6        ;COUNT

IF (VCC)  CO = CI*Q0*Q1*Q2*Q3*Q4*Q5*Q6*Q7        ;CARRY OUT
```

FUNCTION TABLE

```
CLK /OC I1 I0 D7 D6 D5 D4 D3 D2 D1 D0 /CI /CO Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0

;                   -INPUT--           -OUTPUT-
;CONTROL   INSTR   DDDDDDDD   CARRY   QQQQQQQQ   COMMENTS
;CLK /OC   I1 I0   76543210   /CI /CO 76543210   (HEX VALUES)
-----------------------------------------------------------------------------
  C   L     H  L   LLLLLLLH    X   H   LLLLLLLH   LOAD (01)
  C   L     H  H   XXXXXXXX    L   H   LLLLLLHL   INCREMENT
  C   L     H  L   LLLLLLHH    X   H   LLLLLLHH   LOAD (03)
  C   L     H  H   XXXXXXXX    L   H   LLLLLHLL   INCREMENT
  C   L     H  L   LLLLLHHH    X   H   LLLLLHHH   LOAD (07)
  C   L     H  H   XXXXXXXX    L   H   LLLLHLLL   INCREMENT
  C   L     H  L   LLLLHHHH    X   H   LLLLHHHH   LOAD (0F)
  C   L     H  H   XXXXXXXX    L   H   LLLHLLLL   INCREMENT
  C   L     H  L   LLLHHHHH    X   H   LLLHHHHH   LOAD (1F)
  C   L     H  H   XXXXXXXX    L   H   LLHLLLLL   INCREMENT
  C   L     H  L   LLHHHHHH    X   H   LLHHHHHH   LOAD (3F)
  C   L     H  H   XXXXXXXX    L   H   LHLLLLLL   INCREMENT
  C   L     H  L   LHHHHHHH    X   H   LHHHHHHH   LOAD (7F)
  C   L     H  H   XXXXXXXX    L   H   HLLLLLLL   INCREMENT
  C   L     H  L   HHHHHHHH    L   L   HHHHHHHH   LOAD (FF)
  C   L     H  H   XXXXXXXX    L   H   LLLLLLLL   INCREMENT (ROLL OVER)
  C   L     H  L   HHHHHHHH    L   L   HHHHHHHH   LOAD (FF)
  C   L     H  L   HHHHHHHL    X   H   HHHHHHHL   LOAD (FE)
  C   L     H  L   HHHHHHLH    X   H   HHHHHHLH   LOAD (FD)
  C   L     H  L   HHHHHLHH    X   H   HHHHHLHH   LOAD (FB)
  C   L     H  L   HHHHLHHH    X   H   HHHHLHHH   LOAD (F7)
  C   L     H  L   HHHLHHHH    X   H   HHHLHHHH   LOAD (EF)
  C   L     H  L   HHLHHHHH    X   H   HHLHHHHH   LOAD (DF)
  C   L     H  L   HLHHHHHH    X   H   HLHHHHHH   LOAD (BF)
  C   L     H  L   LHHHHHHH    X   H   LHHHHHHH   LOAD (7F)
  C   L     H  L   HHHHHHHH    L   L   HHHHHHHH   LOAD (FF)
  C   L     L  L   XXXXXXXX    X   H   LLLLLLLL   CLEAR
  C   L     H  H   XXXXXXXX    L   H   LLLLLLLH   INCREMENT TO (01)
  C   L     H  H   XXXXXXXX    L   H   LLLLLLHL   INCREMENT TO (02)
  C   L     H  H   XXXXXXXX    L   H   LLLLLLHH   INCREMENT TO (03)
  C   L     H  H   XXXXXXXX    L   H   LLLLLHLL   INCREMENT TO (04)
  C   L     H  H   XXXXXXXX    L   H   LLLLLHLH   INCREMENT TO (05)
  C   L     H  H   XXXXXXXX    L   H   LLLLLHHL   INCREMENT TO (06)
  C   L     H  H   XXXXXXXX    L   H   LLLLLHHH   INCREMENT TO (07)
  C   L     H  H   XXXXXXXX    L   H   LLLLHLLL   INCREMENT TO (08)
  C   L     H  H   XXXXXXXX    L   H   LLLLHLLH   INCREMENT TO (09)
  C   L     H  H   XXXXXXXX    L   H   LLLLHLHL   INCREMENT TO (0A)
  C   L     H  H   XXXXXXXX    L   H   LLLLHLHH   INCREMENT TO (0B)
  C   L     H  H   XXXXXXXX    L   H   LLLLHHLL   INCREMENT TO (0C)
  C   L     H  L   HHHHHHHL    X   H   HHHHHHHL   LOAD (FE)
  C   L     H  H   XXXXXXXX    L   L   HHHHHHHH   INCREMENT TO (FF) /CO=L
  C   L     H  H   XXXXXXXX    H   H   HHHHHHHH   CI INHIBITS COUNT AND CO
  C   L     L  H   LLLLLLLL    L   L   HHHHHHHH   HOLD SEL INHIBITS COUNT ONLY
  C   L     H  H   HHHHHHHH    L   H   LLLLLLLL   INCREMENT TO (00)
  X   H     X  X   XXXXXXXX    X   X   ZZZZZZZZ   TEST HI-Z
-----------------------------------------------------------------------------
```

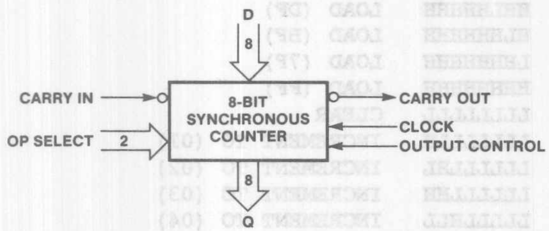
DESCRIPTION

THIS IS AN 8-BIT SYNCHRONOUS COUNTER WITH PARALLEL LOAD, CLEAR, AND HOLD CAPABILITY. THE LOAD OPERATION LOADS THE INPUTS (D7-D0) INTO THE OUTPUT REGISTER (Q7-Q0). THE CLEAR OPERATION RESETS THE OUTPUT REGISTER TO ALL LOWS. THE HOLD OPERATION HOLDS THE PREVIOUS VALUE REGARDLESS OF CLOCK TRANSITIONS. THE INCREMENT OPERATION ADDS ONE TO THE OUTPUT REGISTER WHEN THE CARRY-IN IS TRUE (/CI=L), OTHERWISE THE OPERATION IS A HOLD. THE CARRY-OUT (/CO) IS TRUE (/CO=L) WHEN THE OUTPUT REGISTER (Q7-Q0) IS ALL HIGHS, OTHERWISE FALSE (/CO=H).

THESE OPERATIONS ARE EXERCISED IN THE FUNCTION TABLE AND SUMMARIZED IN THE OPERATIONS TABLE:

/OC	CLK	I1	I0	/CI	D7-D0	Q7-Q0	OPERATION
H	X	X	X	X	X	Z	HI-Z
L	C	L	L	X	X	L	CLEAR
L	C	L	H	X	X	Q	HOLD
L	C	H	L	X	D	D	LOAD
L	C	H	H	H	X	Q	HOLD
L	C	H	H	L	X	Q PLUS 1	INCREMENT

TWO OR MORE 8-BIT COUNTERS MAY BE CASCADED TO PROVIDE LARGER COUNTERS. THE OPERATION CODES WERE CHOSEN SUCH THAT WHEN I1 IS HIGH, I0 MAY BE USED TO SELECT BETWEEN LOAD AND INCREMENT AS IN A PROGRAM COUNTER (JUMP/INCREMENT). ALSO, CARRY-OUT (/CO) AND CARRY-IN (/CI) ARE LOCATED ON PINS 14 AND 23 RESPECTIVELY, WHICH PROVIDES FOR CONVENIENT INTERCONNECTIONS WHEN TWO OR MORE 8-BIT COUNTERS ARE CASCADED TO IMPLEMENT LARGER COUNTERS.



```
8-BIT SYNCHRONOUS COUNTER

 1 C010000001X0HLLLLLLLHX1
 2 C1XXXXXXXX1X0HLLLLLLHL01
 3 C0110000001X0HLLLLLLHHX1
 4 C1XXXXXXXX1X0HLLLLLHLL01
 5 C0111000001X0HLLLLLHHHX1
 6 C1XXXXXXXX1X0HLLLLHLLL01
 7 C0111100001X0HLLLLHHHHX1
 8 C1XXXXXXXX1X0HLLLHLLLL01
 9 C0111110001X0HLLLHHHHHX1
10 C1XXXXXXXX1X0HLLHLLLLL01
11 C0111111001X0HLLHHHHHHX1
12 C1XXXXXXXX1X0HLHLLLLLL01
13 C0111111101X0HLHHHHHHHX1
14 C1XXXXXXXX1X0HHLLLLLLL01
15 C0111111111X0LHHHHHHHH01
16 C1XXXXXXXX1X0HLLLLLLLL01
17 C0111111111X0LHHHHHHHH01
18 C0011111111X0HHHHHHHHLX1
19 C0101111111X0HHHHHHHLHX1
20 C0110111111X0HHHHHHLHHX1
21 C0111011111X0HHHHHLHHHX1
22 C0111101111X0HHHHLHHHHX1
23 C0111110111X0HHHLHHHHHX1
24 C0111111011X0HHLHHHHHHX1
25 C0111111101X0HLHHHHHHHX1
26 C0111111111X0LHHHHHHHH01
27 C0XXXXXXXX0X0HLLLLLLLLX1
28 C1XXXXXXXX1X0HLLLLLLLH01
29 C1XXXXXXXX1X0HLLLLLLHL01
30 C1XXXXXXXX1X0HLLLLLLHH01
31 C1XXXXXXXX1X0HLLLLLHLL01
32 C1XXXXXXXX1X0HLLLLLHLH01
33 C1XXXXXXXX1X0HLLLLLHHL01
34 C1XXXXXXXX1X0HLLLLLHHH01
35 C1XXXXXXXX1X0HLLLLHLLL01
36 C1XXXXXXXX1X0HLLLLHLHH01
37 C1XXXXXXXX1X0HLLLLHHLL01
38 C1XXXXXXXX1X0HLLLLHHLH01
39 C1XXXXXXXX1X0HLLLLHHHL01
40 C0011111111X0HHHHHHHHLX1
41 C1XXXXXXXX1X0LHHHHHHHH01
42 C1XXXXXXXX1X0HHHHHHHHH11
43 C1000000000X0LHHHHHHHH01
44 C1111111111X0HLLLLLLLL01
45 XXXXXXXXXXXX1XZZZZZZZZX1

PASS SIMULATION
```

8-BIT SYNCHRONOUS COUNTER

```
                11 1111 1111 2222 2222 2233 3333 3333
   0123 4567 8901 2345 6789 0123 4567 8901 2345 6789

 8 -X-- ---- ---- ---- ---- ---- ---- ---- ---- -X-- /I1*/I0
 9 X--- ---X ---- ---- ---- ---- ---- ---- ---- ---- I0*/Q0
10 -X-- -X-- ---- ---- ---- ---- ---- ---- ---- X--- I1*/I0*/D0
11 X--X ---- ---- ---- ---- ---- ---- ---- ---- X--- I1*I0*CI

16 -X-- ---- ---- ---- ---- ---- ---- ---- ---- -X-- /I1*/I0
17 X--- ---- ---X ---- ---- ---- ---- ---- ---- ---- I0*/Q1
18 -X-- ---- -X-- ---- ---- ---- ---- ---- ---- X--- I1*/I0*/D1
19 X--X --X- ---- ---- ---- ---- ---- ---- ---- X--- I1*I0*CI*Q0

24 -X-- ---- ---- ---- ---- ---- ---- ---- ---- -X-- /I1*/I0
25 X--- ---- ---- ---X ---- ---- ---- ---- ---- ---- I0*/Q2
26 -X-- ---- ---- -X-- ---- ---- ---- ---- ---- X--- I1*/I0*/D2
27 X--X --X- --X- ---- ---- ---- ---- ---- ---- X--- I1*I0*CI*Q0*Q1

32 -X-- ---- ---- ---- ---- ---- ---- ---- ---- -X-- /I1*/I0
33 X--- ---- ---- ---- ---X ---- ---- ---- ---- ---- I0*/Q3
34 -X-- ---- ---- ---- -X-- ---- ---- ---- ---- X--- I1*/I0*/D3
35 X--X --X- --X- --X- ---- ---- ---- ---- ---- X--- I1*I0*CI*Q0*Q1*Q2

40 -X-- ---- ---- ---- ---- ---- ---- ---- ---- -X-- /I1*/I0
41 X--- ---- ---- ---- ---- ---X ---- ---- ---- ---- I0*/Q4
42 -X-- ---- ---- ---- ---- -X-- ---- ---- ---- X--- I1*/I0*/D4
43 X--X --X- --X- --X- --X- ---- ---- ---- ---- X--- I1*I0*CI*Q0*Q1*Q2*Q3

48 -X-- ---- ---- ---- ---- ---- ---- ---- ---- -X-- /I1*/I0
49 X--- ---- ---- ---- ---- ---- ---X ---- ---- ---- I0*/Q5
50 -X-- ---- ---- ---- ---- ---- -X-- ---- ---- X--- I1*/I0*/D5
51 X--X --X- --X- --X- --X- --X- ---- ---- ---- X--- I1*I0*CI*Q0*Q1*Q2*Q3*Q4

56 -X-- ---- ---- ---- ---- ---- ---- ---- ---- -X-- /I1*/I0
57 X--- ---- ---- ---- ---- ---- ---- ---X ---- ---- I0*/Q6
58 -X-- ---- ---- ---- ---- ---- ---- -X-- ---- X--- I1*/I0*/D6
59 X--X --X- --X- --X- --X- --X- --X- ---- ---- X--- I1*I0*CI*Q0*Q1*Q2*Q3*Q4-

64 -X-- ---- ---- ---- ---- ---- ---- ---- ---- -X-- /I1*/I0
65 X--- ---- ---- ---- ---- ---- ---- ---- ---X ---- I0*/Q7
66 -X-- ---- ---- ---- ---- ---- ---- ---- -X-- X--- I1*/I0*/D7
67 X--X --X- --X- --X- --X- --X- --X- --X- ---- X--- I1*I0*CI*Q0*Q1*Q2*Q3*Q4-

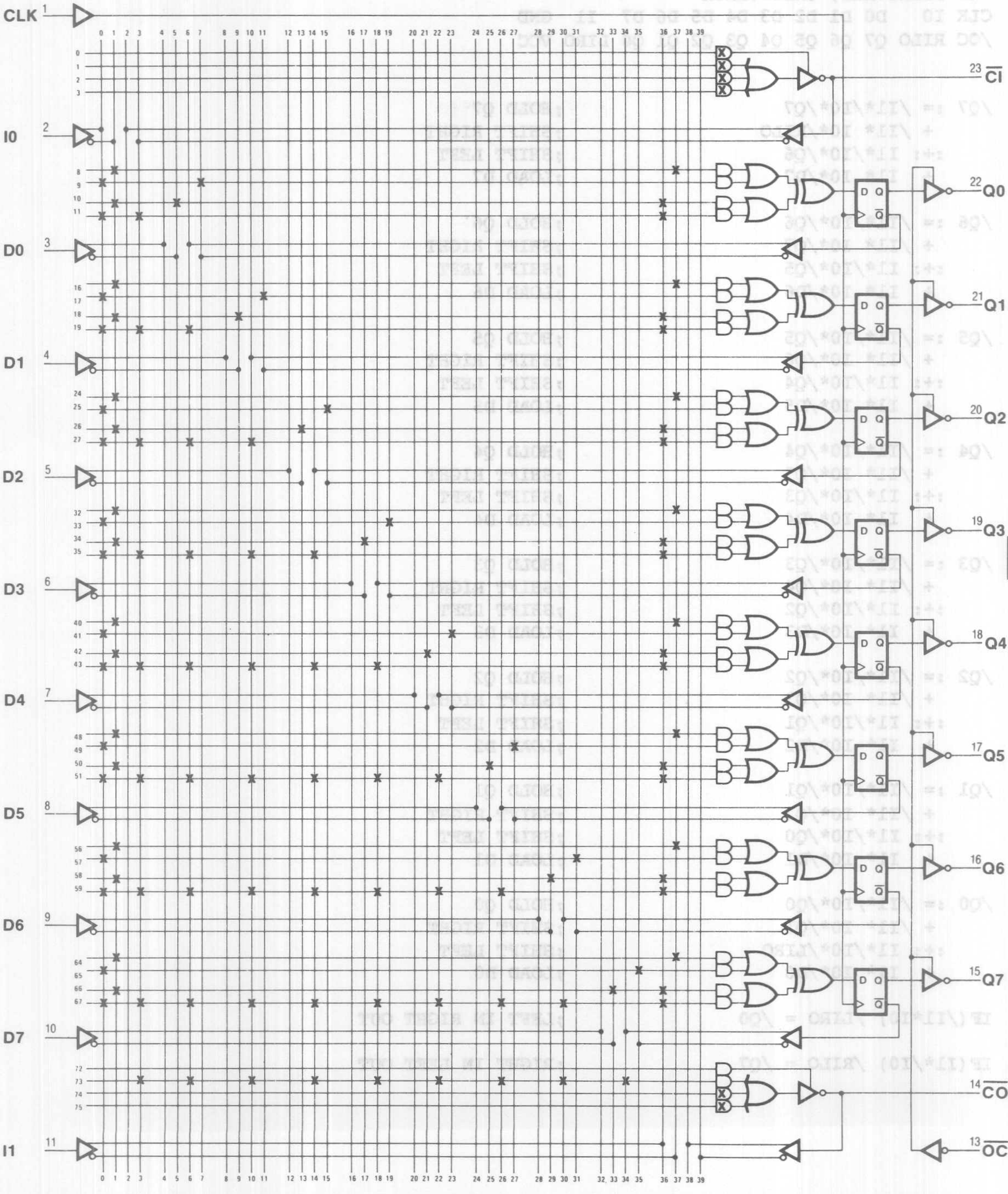
72 ---- ---- ---- ---- ---- ---- ---- ---- ---- ----
73 ---X --X- --X- --X- --X- --X- --X- --X- --X- ---- CI*Q0*Q1*Q2*Q3*Q4*Q5*Q6-

LEGEND:  X : FUSE NOT BLOWN (L,N,0)   - : FUSE BLOWN   (H,P,1)

NUMBER OF FUSES BLOW = 1243
```

8-Bit Synchronous Counter

Logic Diagram PAL20X8



```
PAL20X8                                       PAL DESIGN SPECIFICATION
P8003 (74LS498)                                    UDI GORDON 02/20/81
8-BIT SHIFT REGISTER, PARALLEL IN/OUT
MMI SUNNYVALE, CALIFORNIA
CLK I0   D0 D1 D2 D3 D4 D5 D6 D7  I1  GND
/OC RILO Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0 LIRO VCC

/Q7 := /I1*/I0*/Q7                     ;HOLD Q7
     + /I1* I0*/RILO                   ;SHIFT RIGHT
    :+: I1*/I0*/Q6                     ;SHIFT LEFT
     +  I1* I0*/D7                     ;LOAD D7

/Q6 := /I1*/I0*/Q6                     ;HOLD Q6
     + /I1* I0*/Q7                     ;SHIFT RIGHT
    :+: I1*/I0*/Q5                     ;SHIFT LEFT
     +  I1* I0*/D6                     ;LOAD D6

/Q5 := /I1*/I0*/Q5                     ;HOLD Q5
     + /I1* I0*/Q6                     ;SHIFT RIGHT
    :+: I1*/I0*/Q4                     ;SHIFT LEFT
     +  I1* I0*/D5                     ;LOAD D5

/Q4 := /I1*/I0*/Q4                     ;HOLD Q4
     + /I1* I0*/Q5                     ;SHIFT RIGHT
    :+: I1*/I0*/Q3                     ;SHIFT LEFT
     +  I1* I0*/D4                     ;LOAD D4

/Q3 := /I1*/I0*/Q3                     ;HOLD Q3
     + /I1* I0*/Q4                     ;SHIFT RIGHT
    :+: I1*/I0*/Q2                     ;SHIFT LEFT
     +  I1* I0*/D3                     ;LOAD D3

/Q2 := /I1*/I0*/Q2                     ;HOLD Q2
     + /I1* I0*/Q3                     ;SHIFT RIGHT
    :+: I1*/I0*/Q1                     ;SHIFT LEFT
     +  I1* I0*/D2                     ;LOAD D2

/Q1 := /I1*/I0*/Q1                     ;HOLD Q1
     + /I1* I0*/Q2                     ;SHIFT RIGHT
    :+: I1*/I0*/Q0                     ;SHIFT LEFT
     +  I1* I0*/D1                     ;LOAD D1

/Q0 := /I1*/I0*/Q0                     ;HOLD Q0
     + /I1* I0*/Q1                     ;SHIFT RIGHT
    :+: I1*/I0*/LIRO                   ;SHIFT LEFT
     +  I1* I0*/D0                     ;LOAD D0

IF(/I1*I0) /LIRO = /Q0                 ;LEFT IN RIGHT OUT

IF(I1*/I0) /RILO = /Q7                 ;RIGHT IN LEFT OUT
```

```
FUNCTION TABLE

I1 I0 D7 D6 D5 D4 D3 D2 D1 D0 CLK /OC RILO LIRO Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0

;       DATA  IN                           Q  OUT
;INST  D7----D0  CLK /OC RILO LIRO  Q7----Q0     COMMENTS
-----------------------------------------------------------------------
  HH   LLLLLLLL   C   L    Z    Z   LLLLLLLL     LOAD ZEROS
  LL   XXXXXXXX   C   L    Z    Z   LLLLLLLL     HOLD
  HL   XXXXXXXX   C   L    L    H   LLLLLLLH     SHIFT LEFT IN A H
  HL   XXXXXXXX   C   L    L    L   LLLLLLHL     SHIFT LEFT IN A L
  HL   XXXXXXXX   C   L    L    L   LLLLLHLL     SHIFT LEFT IN A L
  HL   XXXXXXXX   C   L    L    L   LLLLHLLL     SHIFT LEFT IN A L
  HL   XXXXXXXX   C   L    L    L   LLLHLLLL     SHIFT LEFT IN A L
  HL   XXXXXXXX   C   L    L    L   LLHLLLLL     SHIFT LEFT IN A L
  HL   XXXXXXXX   C   L    L    L   LHLLLLLL     SHIFT LEFT IN A L
  HL   XXXXXXXX   C   L    H    L   HLLLLLLL     SHIFT LEFT IN A L
  HL   XXXXXXXX   C   L    L    L   LLLLLLLL     SHIFT LEFT IN A L
  LL   XXXXXXXX   X   H    Z    Z   ZZZZZZZZ     TEST HI-Z
  HH   HHHHHHHH   C   L    Z    Z   HHHHHHHH     LOAD ONES
  LL   XXXXXXXX   C   L    Z    Z   HHHHHHHH     HOLD
  LH   XXXXXXXX   C   L    L    H   LHHHHHHH     SHIFT RIGHT IN A L
  LH   XXXXXXXX   C   L    H    H   HLHHHHHH     SHIFT RIGHT IN A H
  LH   XXXXXXXX   C   L    H    H   HHLHHHHH     SHIFT RIGHT IN A H
  LH   XXXXXXXX   C   L    H    H   HHHLHHHH     SHIFT RIGHT IN A H
  LH   XXXXXXXX   C   L    H    H   HHHHLHHH     SHIFT RIGHT IN A H
  LH   XXXXXXXX   C   L    H    H   HHHHHLHH     SHIFT RIGHT IN A H
  LH   XXXXXXXX   C   L    H    H   HHHHHHLH     SHIFT RIGHT IN A H
  LH   XXXXXXXX   C   L    H    L   HHHHHHHL     SHIFT RIGHT IN A H
  LH   XXXXXXXX   C   L    H    H   HHHHHHHH     SHIFT RIGHT IN A H
  LL   XXXXXXXX   X   H    Z    Z   ZZZZZZZZ     TEST HI-Z
-----------------------------------------------------------------------
```

DESCRIPTION

THIS PAL IS AN 8-BIT SHIFT REGISTER WITH PARALLEL LOAD AND HOLD CAPABILITY. TWO FUNCTION SELECT INPUTS (I0,I1) PROVIDE ONE OF FOUR OPERATIONS WHICH OCCUR SYNCHRONOUSLY ON THE RISING EDGE OF THE CLOCK (CLK). THESE OPERATIONS ARE:

```
/OC  CLK  I1  I0  D7-D0  Q7-Q0    OPERATION
----------------------------------------------
 H    X    X   X    X      Z      HI-Z
 L    C    L   L    X      L      HOLD
 L    C    L   H    X    SR(Q)    SHIFT RIGHT
 L    C    H   L    X    SL(Q)    SHIFT LEFT
 L    C    H   H    D      D      LOAD
----------------------------------------------
```

TWO OR MORE 8-BIT SHIFT REGISTERS MAY BE CASCADED TO PROVIDE LARGER SHIFT REGISTERS. RILO AND LIRO ARE LOCATED ON PINS 14 AND 23 RESPECTIVELY, WHICH PROVIDES FOR CONVENIENT INTERCONNECTIONS WHEN TWO OR MORE 8-BIT SHIFT REGISTERS ARE CASCADED TO IMPLEMENT LARGER SHIFT REGISTERS.

```
8-BIT SHIFT REGISTER, PARALLEL IN/OUT

               11 1111 1111 2222 2222 2233 3333 3333
 0123 4567 8901 2345 6789 0123 4567 8901 2345 6789

 0 X--- ---- ---- ---- ---- ---- ---- ---- ---- -X-- /I1*I0
 1 ---- ---X ---- ---- ---- ---- ---- ---- ---- ---- /Q0

 8 -X-- ---X ---- ---- ---- ---- ---- ---- ---- -X-- /I1*/I0*/Q0
 9 X--- ---- ---X ---- ---- ---- ---- ---- ---- -X-- /I1*I0*/Q1
10 -X-X ---- ---- ---- ---- ---- ---- ---- ---- X--- I1*/I0*/LIRO
11 X--- -X-- ---- ---- ---- ---- ---- ---- ---- X--- I1*I0*/D0

16 -X-- ---- ---X ---- ---- ---- ---- ---- ---- -X-- /I1*/I0*/Q1
17 X--- ---- ---- ---X ---- ---- ---- ---- ---- -X-- /I1*I0*/Q2
18 -X-- ---X ---- ---- ---- ---- ---- ---- ---- X--- I1*/I0*/Q0
19 X--- ---- -X-- ---- ---- ---- ---- ---- ---- X--- I1*I0*/D1

24 -X-- ---- ---- ---X ---- ---- ---- ---- ---- -X-- /I1*/I0*/Q2
25 X--- ---- ---- ---- ---X ---- ---- ---- ---- -X-- /I1*I0*/Q3
26 -X-- ---- ---X ---- ---- ---- ---- ---- ---- X--- I1*/I0*/Q1
27 X--- ---- ---- -X-- ---- ---- ---- ---- ---- X--- I1*I0*/D2

32 -X-- ---- ---- ---- ---X ---- ---- ---- ---- -X-- /I1*/I0*/Q3
33 X--- ---- ---- ---- ---- ---X ---- ---- ---- -X-- /I1*I0*/Q4
34 -X-- ---- ---- ---X ---- ---- ---- ---- ---- X--- I1*/I0*/Q2
35 X--- ---- ---- ---- -X-- ---- ---- ---- ---- X--- I1*I0*/D3

40 -X-- ---- ---- ---- ---- ---X ---- ---- ---- -X-- /I1*/I0*/Q4
41 X--- ---- ---- ---- ---- ---- ---X ---- ---- -X-- /I1*I0*/Q5
42 -X-- ---- ---- ---- ---X ---- ---- ---- ---- X--- I1*/I0*/Q3
43 X--- ---- ---- ---- ---- -X-- ---- ---- ---- X--- I1*I0*/D4

48 -X-- ---- ---- ---- ---- ---- ---X ---- ---- -X-- /I1*/I0*/Q5
49 X--- ---- ---- ---- ---- ---- ---- ---X ---- -X-- /I1*I0*/Q6
50 -X-- ---- ---- ---- ---- ---X ---- ---- ---- X--- I1*/I0*/Q4
51 X--- ---- ---- ---- ---- ---- -X-- ---- ---- X--- I1*I0*/D5

56 -X-- ---- ---- ---- ---- ---- ---- ---X ---- -X-- /I1*/I0*/Q6
57 X--- ---- ---- ---- ---- ---- ---- ---- ---X -X-- /I1*I0*/Q7
58 -X-- ---- ---- ---- ---- ---- ---X ---- ---- X--- I1*/I0*/Q5
59 X--- ---- ---- ---- ---- ---- ---- -X-- ---- X--- I1*I0*/D6

64 -X-- ---- ---- ---- ---- ---- ---- ---- ---X -X-- /I1*/I0*/Q7
65 X--- ---- ---- ---- ---- ---- ---- ---- ---- -X-X /I1*I0*/RILO
66 -X-- ---- ---- ---- ---- ---- ---- ---X ---- X--- I1*/I0*/Q6
67 X--- ---- ---- ---- ---- ---- ---- ---- -X-- X--- I1*I0*/D7

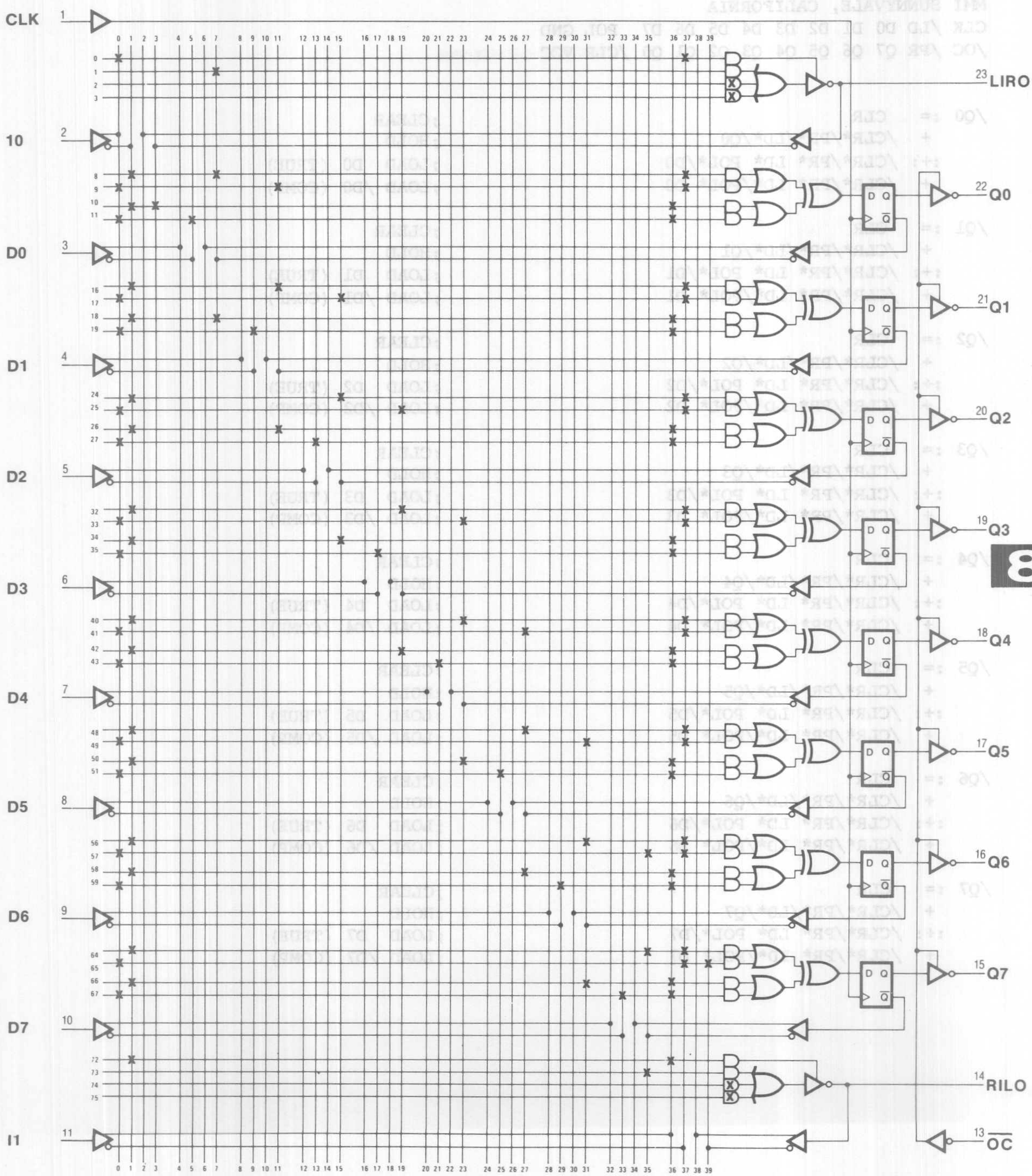
72 -X-- ---- ---- ---- ---- ---- ---- ---- ---- X--- I1*/I0
73 ---- ---- ---- ---- ---- ---- ---- ---- ---X ---- /Q7

LEGEND:  X : FUSE NOT BLOWN (L,N,0)   - : FUSE BLOWN   (H,P,1)

NUMBER OF FUSES BLOW = 1338
```

8-bit Shift Register, Parallel In/Out

Logic Diagram PAL20X8



8

```
PAL20X8                                          PAL DESIGN SPECIFICATION
74LS380                                      BIRKNER/KAZMI/BLASCO 02/16/81
MULTIFUNCTION OCTAL REGISTER
MMI SUNNYVALE, CALIFORNIA
CLK /LD D0 D1 D2 D3 D4 D5 D6 D7  POL GND
/OC /PR Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0 /CLR VCC

/Q0 :=   CLR                                    ;CLEAR
     +  /CLR*/PR*/LD*/Q0                        ;HOLD
   :+:  /CLR*/PR* LD* POL*/D0                   ;LOAD  D0 (TRUE)
     +  /CLR*/PR* LD*/POL* D0                   ;LOAD /D0 (COMP)

/Q1 :=   CLR                                    ;CLEAR
     +  /CLR*/PR*/LD*/Q1                        ;HOLD
   :+:  /CLR*/PR* LD* POL*/D1                   ;LOAD  D1 (TRUE)
     +  /CLR*/PR* LD*/POL* D1                   ;LOAD /D1 (COMP)

/Q2 :=   CLR                                    ;CLEAR
     +  /CLR*/PR*/LD*/Q2                        ;HOLD
   :+:  /CLR*/PR* LD* POL*/D2                   ;LOAD  D2 (TRUE)
     +  /CLR*/PR* LD*/POL* D2                   ;LOAD /D2 (COMP)

/Q3 :=   CLR                                    ;CLEAR
     +  /CLR*/PR*/LD*/Q3                        ;HOLD
   :+:  /CLR*/PR* LD* POL*/D3                   ;LOAD  D3 (TRUE)
     +  /CLR*/PR* LD*/POL* D3                   ;LOAD /D3 (COMP)

/Q4 :=   CLR                                    ;CLEAR
     +  /CLR*/PR*/LD*/Q4                        ;HOLD
   :+:  /CLR*/PR* LD* POL*/D4                   ;LOAD  D4 (TRUE)
     +  /CLR*/PR* LD*/POL* D4                   ;LOAD /D4 (COMP)

/Q5 :=   CLR                                    ;CLEAR
     +  /CLR*/PR*/LD*/Q5                        ;HOLD
   :+:  /CLR*/PR* LD* POL*/D5                   ;LOAD  D5 (TRUE)
     +  /CLR*/PR* LD*/POL* D5                   ;LOAD /D5 (COMP)

/Q6 :=   CLR                                    ;CLEAR
     +  /CLR*/PR*/LD*/Q6                        ;HOLD
   :+:  /CLR*/PR* LD* POL*/D6                   ;LOAD  D6 (TRUE)
     +  /CLR*/PR* LD*/POL* D6                   ;LOAD /D6 (COMP)

/Q7 :=   CLR                                    ;CLEAR
     +  /CLR*/PR*/LD*/Q7                        ;HOLD
   :+:  /CLR*/PR* LD* POL*/D7                   ;LOAD  D7 (TRUE)
     +  /CLR*/PR* LD*/POL* D7                   ;LOAD /D7 (COMP)
```

```
FUNCTION TABLE

D7 D6 D5 D4 D3 D2 D1 D0 /CLR /PR /LD POL CLK /OC Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0

;  INPUTS          CONTROL            OUTPUTS    COMMENTS
; D7----D0   /CLR /PR /LD POL CLK /OC   Q7----Q0
-----------------------------------------------------------------------------
;CLEAR AND PRESET TESTS
  HHHHHHHH    L   L   L   H   C   L   LLLLLLLL   CLEAR (OVERRIDES PRESET/LOAD)
  LLLLLLLL    H   L   L   H   C   L   HHHHHHHH   PRESET (OVERRIDES LOAD)
  LLLLLLLL    L   L   L   L   C   L   LLLLLLLL   CLEAR (POL=L)
  HHHHHHHH    H   L   L   L   C   L   HHHHHHHH   PRESET (POL=L)
;LOAD DATA - WALKING ZEROES (TRUE DATA)
  HHHHHHHL    H   H   L   H   C   L   HHHHHHHL   LOAD HEX(FE)
  HHHHHHLH    H   H   L   H   C   L   HHHHHHLH   LOAD HEX(FD)
  HHHHHLHH    H   H   L   H   C   L   HHHHHLHH   LOAD HEX(FB)
  HHHHLHHH    H   H   L   H   C   L   HHHHLHHH   LOAD HEX(F7)
  HHHLHHHH    H   H   L   H   C   L   HHHLHHHH   LOAD HEX(EF)
  HHLHHHHH    H   H   L   H   C   L   HHLHHHHH   LOAD HEX(DF)
  HLHHHHHH    H   H   L   H   C   L   HLHHHHHH   LOAD HEX(BF)
  LHHHHHHH    H   H   L   H   C   L   LHHHHHHH   LOAD HEX(7F)
  HHHHHHHH    H   H   L   H   C   L   HHHHHHHH   LOAD HEX(FF)
;LOAD DATA - WALKING ONES (TRUE DATA)
  LLLLLLLH    H   H   L   H   C   L   LLLLLLLH   LOAD HEX(01)
  LLLLLLHL    H   H   L   H   C   L   LLLLLLHL   LOAD HEX(02)
  LLLLLHLL    H   H   L   H   C   L   LLLLLHLL   LOAD HEX(04)
  LLLLHLLL    H   H   L   H   C   L   LLLLHLLL   LOAD HEX(08)
  LLLHLLLL    H   H   L   H   C   L   LLLHLLLL   LOAD HEX(10)
  LLHLLLLL    H   H   L   H   C   L   LLHLLLLL   LOAD HEX(20)
  LHLLLLLL    H   H   L   H   C   L   LHLLLLLL   LOAD HEX(40)
  HLLLLLLL    H   H   L   H   C   L   HLLLLLLL   LOAD HEX(80)
  LLLLLLLL    H   H   L   H   C   L   LLLLLLLL   LOAD HEX(00)
;LOAD DATA - WALKING ONES (COMP DATA) WITH HOLD TESTS
  LLLLLLLL    H   H   H   L   C   L   LLLLLLLL   HOLD
  LLLLLLLL    H   H   L   L   C   L   HHHHHHHH   LOAD HEX(00) (COMP)
  LLLLLLLL    H   H   H   H   C   L   HHHHHHHH   HOLD
  LLLLLLLH    H   H   L   L   C   L   HHHHHHHL   LOAD HEX(01) (COMP)
  LLLLLLLL    H   H   H   L   C   L   HHHHHHHL   HOLD
  LLLLLLHL    H   H   L   L   C   L   HHHHHHLH   LOAD HEX(02) (COMP)
  HHHHHHHH    H   H   H   H   C   L   HHHHHHLH   HOLD
  LLLLLHLL    H   H   L   L   C   L   HHHHHLHH   LOAD HEX(04) (COMP)
  LLLLLLLL    H   H   H   L   C   L   HHHHHLHH   HOLD
  LLLLHLLL    H   H   L   L   C   L   HHHHLHHH   LOAD HEX(80) (COMP)
  HHHHHHHH    H   H   H   H   C   L   HHHHLHHH   HOLD
  LLLHLLLL    H   H   L   L   C   L   HHHLHHHH   LOAD HEX(10) (COMP)
  LLLLLLLL    H   H   H   L   C   L   HHHLHHHH   HOLD
  LLHLLLLL    H   H   L   L   C   L   HHLHHHHH   LOAD HEX(20) (COMP)
  HHHHHHHH    H   H   H   H   C   L   HHLHHHHH   HOLD
  LHLLLLLL    H   H   L   L   C   L   HLHHHHHH   LOAD HEX(40) (COMP)
  LLLLLLLL    H   H   H   L   C   L   HLHHHHHH   HOLD
  HLLLLLLL    H   H   L   L   C   L   LHHHHHHH   LOAD HEX(80) (COMP)
  HHHHHHHH    H   H   H   H   C   L   LHHHHHHH   HOLD
  LLLLLLLL    H   H   L   L   C   L   HHHHHHHH   LOAD HEX(00) (COMP)
  XXXXXXXX    X   X   X   X   X   H   ZZZZZZZZ   TEST HI-Z
-----------------------------------------------------------------------------
```

DESCRIPTION

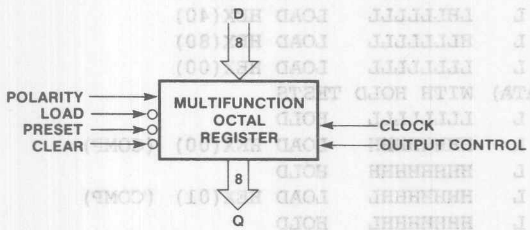
THIS IS AN 8-BIT SYNCHRONOUS REGISTER WITH PARALLEL LOAD, LOAD COMPLIMENT, PRESET, CLEAR, AND HOLD CAPABILITIES. FOUR CONTROL INPUTS (/LD,POL,/CLR,/PR) PROVIDE ONE OF FOUR OPERATIONS WHICH OCCUR SYNCHRONOUSLY WITH THE CLOCK (CLK).

THE LOAD OPERATION LOADS THE INPUTS (D7-D0) INTO THE OUTPUT REGISTER (Q7-Q0), WHEN POL=H OR LOADS THE COMPLIMENT OF THE INPUTS WHEN POL=L. THE CLEAR (/CLR) OPERATION RESETS THE OUTPUT REGISTERS TO ALL LOWS. THE PRESET (/PR) OPERATION PRESETS THE OUTPUT REGISTERS TO ALL HIGHS. THE HOLD OPERATION HOLDS THE PREVIOUS VALUE REGARDLESS OF CLOCK TRANSITIONS.

CLEAR OVERRIDES PRESET, PRESET OVERRIDES LOAD, AND LOAD OVERRIDES HOLD.

THESE OPERATIONS ARE EXERCISED IN THE FUNCTION TABLE AND SUMMARIZED IN THE OPERATIONS TABLE:

/OC	CLK	/CLR	/PR	/LD	POL	D7-D0	Q7-Q0	OPERATION
H	X	X	X	X	X	X	Z	HI-Z
L	C	L	X	X	X	X	L	CLEAR
L	C	H	L	L	X	X	H	PRESET
L	C	H	H	H	X	X	Q	HOLD
L	C	H	H	L	H	D	D	LOAD TRUE
L	C	H	H	L	L	D	/D	LOAD COMP



MULTIFUNCTION OCTAL REGISTER

```
 1 C0111111111X00LLLLLLLL01
 2 C0000000001X00HHHHHHHH11
 3 C0000000000X00LLLLLLLL01
 4 C0111111110X00HHHHHHHH11
 5 C0011111111X01HHHHHHHL11
 6 C0101111111X01HHHHHHLH11
 7 C0110111111X01HHHHHLHH11
 8 C0111011111X01HHHHLHHH11
 9 C0111101111X01HHHLHHHH11
10 C0111110111X01HHLHHHHH11
11 C0111111011X01HLHHHHHH11
12 C0111111101X01LHHHHHHH11
13 C0111111111X01HHHHHHHH11
14 C0100000001X01LLLLLLLH11
15 C0010000001X01LLLLLLHL11
16 C0001000001X01LLLLLHLL11
17 C0000100001X01LLLLHLLL11
18 C0000010001X01LLLHLLLL11
19 C0000001001X01LLHLLLLL11
20 C0000000101X01LHLLLLLL11
21 C0000000011X01HLLLLLLL11
22 C0000000001X01LLLLLLLL11
23 C1000000000X01LLLLLLLL11
24 C0000000000X01HHHHHHHH11
25 C1000000001X01HHHHHHHH11
26 C0100000000X01HHHHHHHL11
27 C1000000000X01HHHHHHHL11
28 C0010000000X01HHHHHHLH11
29 C1111111111X01HHHHHHLH11
30 C0001000000X01HHHHHLHH11
31 C1000000000X01HHHHHLHH11
32 C0000100000X01HHHHLHHH11
33 C1111111111X01HHHHLHHH11
34 C0000010000X01HHHLHHHH11
35 C1000000000X01HHHLHHHH11
36 C0000001000X01HHLHHHHH11
37 C1111111111X01HHLHHHHH11
38 C0000000100X01HLHHHHHH11
39 C1000000000X01HLHHHHHH11
40 C0000000010X01LHHHHHHH11
41 C1111111111X01LHHHHHHH11
42 C0000000000X01HHHHHHHH11
43 XXXXXXXXXXXX1XZZZZZZZZX1
```

PASS SIMULATION

8

```
     0123 4567 8901 2345 6789 0123 4567 8901 2345 6789

  8  ---X ---- ---- ---- ---- ---- ---- ---- ---- ---- CLR
  9  X-X- ---X ---- ---- ---- ---- ---- ---- ---- --X- /CLR*/PR*/LD*/Q0
 10  -XX- -X-- ---- ---- ---- ---- ---- ---- ---- X-X- /CLR*/PR*LD*POL*/D0
 11  -XX- X--- ---- ---- ---- ---- ---- ---- ---- -XX- /CLR*/PR*LD*/POL*D0

 16  ---X ---- ---- ---- ---- ---- ---- ---- ---- ---- CLR
 17  X-X- ---- ---X ---- ---- ---- ---- ---- ---- --X- /CLR*/PR*/LD*/Q1
 18  -XX- ---- -X-- ---- ---- ---- ---- ---- ---- X-X- /CLR*/PR*LD*POL*/D1
 19  -XX- ---- X--- ---- ---- ---- ---- ---- ---- -XX- /CLR*/PR*LD*/POL*D1

 24  ---X ---- ---- ---- ---- ---- ---- ---- ---- ---- CLR
 25  X-X- ---- ---- ---X ---- ---- ---- ---- ---- --X- /CLR*/PR*/LD*/Q2
 26  -XX- ---- ---- -X-- ---- ---- ---- ---- ---- X-X- /CLR*/PR*LD*POL*/D2
 27  -XX- ---- ---- X--- ---- ---- ---- ---- ---- -XX- /CLR*/PR*LD*/POL*D2

 32  ---X ---- ---- ---- ---- ---- ---- ---- ---- ---- CLR
 33  X-X- ---- ---- ---- ---X ---- ---- ---- ---- --X- /CLR*/PR*/LD*/Q3
 34  -XX- ---- ---- ---- -X-- ---- ---- ---- ---- X-X- /CLR*/PR*LD*POL*/D3
 35  -XX- ---- ---- ---- X--- ---- ---- ---- ---- -XX- /CLR*/PR*LD*/POL*D3

 40  ---X ---- ---- ---- ---- ---- ---- ---- ---- ---- CLR
 41  X-X- ---- ---- ---- ---- ---X ---- ---- ---- --X- /CLR*/PR*/LD*/Q4
 42  -XX- ---- ---- ---- ---- -X-- ---- ---- ---- X-X- /CLR*/PR*LD*POL*/D4
 43  -XX- ---- ---- ---- ---- X--- ---- ---- ---- -XX- /CLR*/PR*LD*/POL*D4

 48  ---X ---- ---- ---- ---- ---- ---- ---- ---- ---- CLR
 49  X-X- ---- ---- ---- ---- ---- ---X ---- ---- --X- /CLR*/PR*/LD*/Q5
 50  -XX- ---- ---- ---- ---- ---- -X-- ---- ---- X-X- /CLR*/PR*LD*POL*/D5
 51  -XX- ---- ---- ---- ---- ---- X--- ---- ---- -XX- /CLR*/PR*LD*/POL*D5

 56  ---X ---- ---- ---- ---- ---- ---- ---- ---- ---- CLR
 57  X-X- ---- ---- ---- ---- ---- ---- ---X ---- --X- /CLR*/PR*/LD*/Q6
 58  -XX- ---- ---- ---- ---- ---- ---- -X-- ---- X-X- /CLR*/PR*LD*POL*/D6
 59  -XX- ---- ---- ---- ---- ---- ---- X--- ---- -XX- /CLR*/PR*LD*/POL*D6

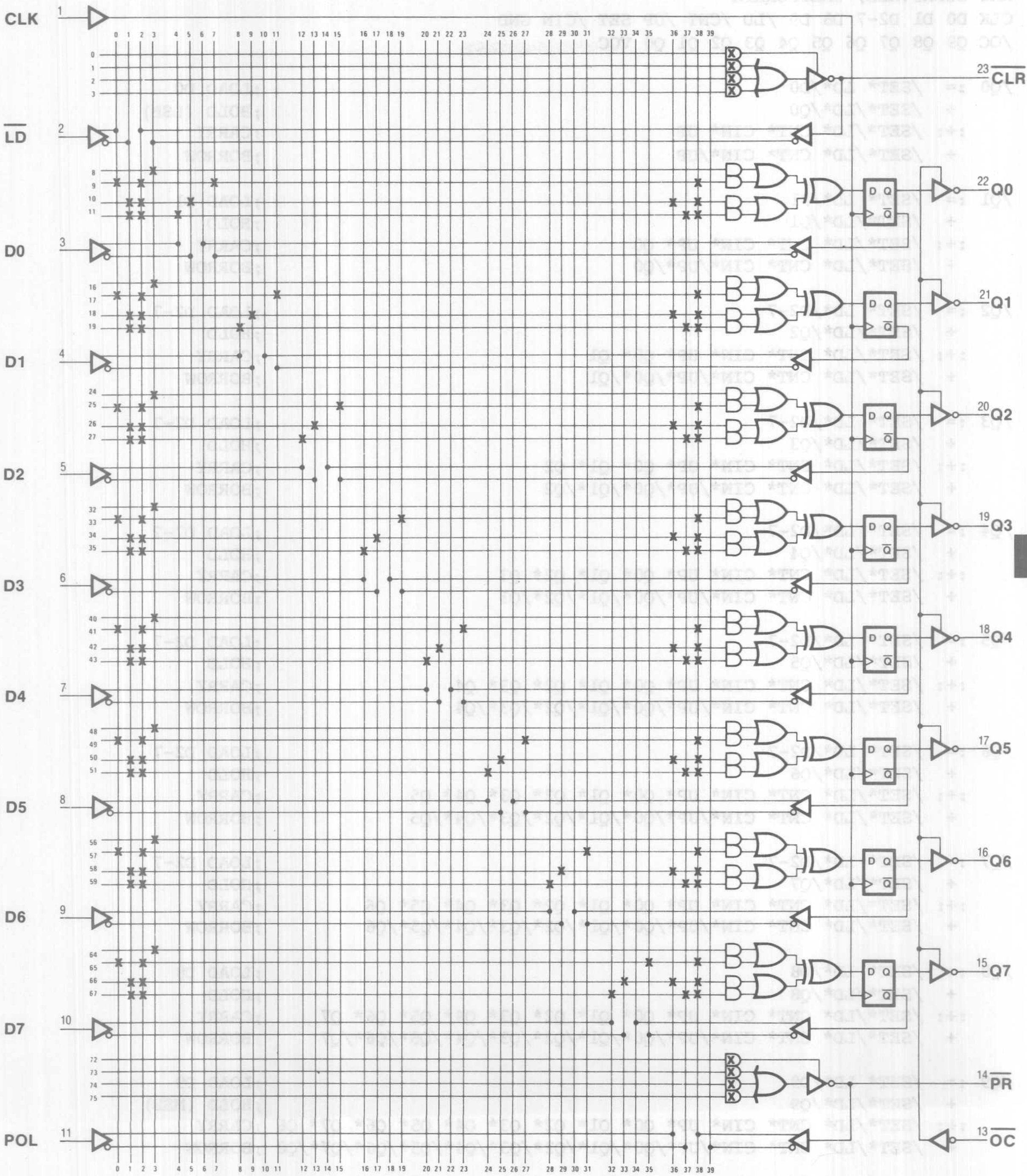
 64  ---X ---- ---- ---- ---- ---- ---- ---- ---- ---- CLR
 65  X-X- ---- ---- ---- ---- ---- ---- ---- ---X --X- /CLR*/PR*/LD*/Q7
 66  -XX- ---- ---- ---- ---- ---- ---- ---- -X-- X-X- /CLR*/PR*LD*POL*/D7
 67  -XX- ---- ---- ---- ---- ---- ---- ---- X--- -XX- /CLR*/PR*LD*/POL*D7


LEGEND:   X : FUSE NOT BLOWN (L,N,0)   - : FUSE BLOWN   (H,P,1)

NUMBER OF FUSES BLOW = 1160
```

Multifunction Octal Register

Logic Diagram PAL20X8



8

```
PAL20X10                                                  PAL DESIGN SPECIFICATION
74LS491                                                     JOHN BIRKNER 04/01/81
10-BIT COUNTER
MMI SUNNYVALE, CALIFORNIA
CLK D0 D1 D2-7 D8 D9 /LD /CNT /UP SET /CIN GND
/OC Q9 Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0 VCC

/Q0 :=  /SET* LD*/D0                                              ;LOAD D0
     +  /SET*/LD*/Q0                                              ;HOLD (LSB)
   :+:  /SET*/LD* CNT* CIN* UP                                    ;CARRY
     +  /SET*/LD* CNT* CIN*/UP                                    ;BORROW

/Q1 :=  /SET* LD*/D1                                              ;LOAD D1
     +  /SET*/LD*/Q1                                              ;HOLD
   :+:  /SET*/LD* CNT* CIN* UP* Q0                                ;CARRY
     +  /SET*/LD* CNT* CIN*/UP*/Q0                                ;BORROW

/Q2 :=  /SET* LD*/D2-7                                            ;LOAD D2-7
     +  /SET*/LD*/Q2                                              ;HOLD
   :+:  /SET*/LD* CNT* CIN* UP* Q0* Q1                            ;CARRY
     +  /SET*/LD* CNT* CIN*/UP*/Q0*/Q1                            ;BORROW

/Q3 :=  /SET* LD*/D2-7                                            ;LOAD D2-7
     +  /SET*/LD*/Q3                                              ;HOLD
   :+:  /SET*/LD* CNT* CIN* UP* Q0* Q1* Q2                        ;CARRY
     +  /SET*/LD* CNT* CIN*/UP*/Q0*/Q1*/Q2                        ;BORROW

/Q4 :=  /SET* LD*/D2-7                                            ;LOAD D2-7
     +  /SET*/LD*/Q4                                              ;HOLD
   :+:  /SET*/LD* CNT* CIN* UP* Q0* Q1* Q2* Q3                    ;CARRY
     +  /SET*/LD* CNT* CIN*/UP*/Q0*/Q1*/Q2*/Q3                    ;BORROW

/Q5 :=  /SET* LD*/D2-7                                            ;LOAD D2-7
     +  /SET*/LD*/Q5                                              ;HOLD
   :+:  /SET*/LD* CNT* CIN* UP* Q0* Q1* Q2* Q3* Q4                ;CARRY
     +  /SET*/LD* CNT* CIN*/UP*/Q0*/Q1*/Q2*/Q3*/Q4                ;BORROW

/Q6 :=  /SET* LD*/D2-7                                            ;LOAD D2-7
     +  /SET*/LD*/Q6                                              ;HOLD
   :+:  /SET*/LD* CNT* CIN* UP* Q0* Q1* Q2* Q3* Q4* Q5            ;CARRY
     +  /SET*/LD* CNT* CIN*/UP*/Q0*/Q1*/Q2*/Q3*/Q4*/Q5            ;BORROW

/Q7 :=  /SET* LD*/D2-7                                            ;LOAD D2-7
     +  /SET*/LD*/Q7                                              ;HOLD
   :+:  /SET*/LD* CNT* CIN* UP* Q0* Q1* Q2* Q3* Q4* Q5* Q6        ;CARRY
     +  /SET*/LD* CNT* CIN*/UP*/Q0*/Q1*/Q2*/Q3*/Q4*/Q5*/Q6        ;BORROW

/Q8 :=  /SET* LD*/D8                                              ;LOAD D8
     +  /SET*/LD*/Q8                                              ;HOLD
   :+:  /SET*/LD* CNT* CIN* UP* Q0* Q1* Q2* Q3* Q4* Q5* Q6* Q7    ;CARRY
     +  /SET*/LD* CNT* CIN*/UP*/Q0*/Q1*/Q2*/Q3*/Q4*/Q5*/Q6*/Q7    ;BORROW

/Q9 :=  /SET* LD*/D9                                              ;LOAD D9
     +  /SET*/LD*/Q9                                              ;HOLD (MSB)
   :+:  /SET*/LD* CNT* CIN* UP* Q0* Q1* Q2* Q3* Q4* Q5* Q6* Q7* Q8 ;CARRY
     +  /SET*/LD* CNT* CIN*/UP*/Q0*/Q1*/Q2*/Q3*/Q4*/Q5*/Q6*/Q7*/Q8 ;BORROW
```

FUNCTION TABLE

```
CLK /OC SET /LD /CNT /CIN /UP D9 D8 D2-7 D1 D0 Q9 Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0

;          / /
;C / S / C C /  -DATA IN-  -DATA OUT-
;L O E L N I U  DD  D  DD  QQQQQQQQQQ
;K C T D T N P  98 2-7 10  9876543210    COMMENT
-------------------------------------------------------------------------------
 C L H X X X X  XX  X  XX  HHHHHHHHHH    SET
 C L L L X X X  LL  L  LL  LLLLLLLLLL    CLEAR
 C L L L X X X  HH  H  HH  HHHHHHHHHH    SET
 C L L H H X X  XX  X  XX  HHHHHHHHHH    HOLD
 C L L L X X X  LL  L  LL  LLLLLLLLLL    CLEAR
 C L L H H X X  XX  X  XX  LLLLLLLLLL    HOLD
 C L L H L H X  XX  X  XX  LLLLLLLLLL    HOLD
 C L L H L L L  XX  X  XX  LLLLLLLLLH    COUNT UP (NOTE 5 CNTRLS LOW NEAR GND)
 C L L H L L L  XX  X  XX  LLLLLLLLHL    COUNT UP
 C L L H L L L  XX  X  XX  LLLLLLLLHH    COUNT UP
 C L L H L L H  XX  X  XX  LLLLLLLLHL    COUNT DOWN
 C L L H L L H  XX  X  XX  LLLLLLLLLH    COUNT DOWN
 C L L H L L H  XX  X  XX  LLLLLLLLLL    COUNT DOWN
 C L L H L L H  XX  X  XX  HHHHHHHHHH    COUNT DOWN (ROLL OVER)
 C L L H L L H  XX  X  XX  HHHHHHHHHL    COUNT DOWN
 X H X X X X X  XX  X  XX  ZZZZZZZZZZ    TEST HI-Z
-------------------------------------------------------------------------------
```

DESCRIPTION

THE 10-BIT COUNTER CAN COUNT UP, COUNT DOWN, SET, AND LOAD 2 LSB'S (D0,D1), 2 MSB'S (D8,D9) AND 6 MIDDLE BITS (D2-7) HIGH OR LOW AS A GROUP.

SET OVERRIDES LOAD (/LD), COUNT (/CNT), AND HOLD. LOAD OVERRIDES COUNT. COUNT IS CONDITIONAL ON CARRY IN (/CIN), OTHERWISE IT HOLDS.

THESE OPERATIONS ARE EXERCISED IN THE FUNCTION TABLE AND SUMMARIZED IN THE OPERATIONS TABLE:

```
/OC  CLK   SET   /LD    /CNT   /CIN  /UP  D9-D0   Q9-Q0      OPERATION
---------------------------------------------------------------------------
 H    X     X     X       X      X     X     X       Z        HI-Z
 L    C     H     X       X      X     X     X       H        SET ALL HIGH
 L    C     L     L       X      X     X     D       D        LOAD D
 L    C     L     H       H      X     X     X       Q        HOLD (/CNT=H)
 L    C     L     H       L      H     X     X       Q        HOLD (/CIN=H)
 L    C     L     H       L      H     L     X     Q PLUS  1  COUNT UP
 L    C     L     H       L      H     H     X     Q MINUS 1  COUNT DOWN
---------------------------------------------------------------------------
```

10-BIT COUNTER

```
              11 1111 1111 2222 2222 2233 3333 3333
   0123 4567 8901 2345 6789 0123 4567 8901 2345 6789

 0 -X-- ---- ---- ---- ---- -X-- ---- ---- -X-- ---- /SET*LD*/D0
 1 ---X ---- ---- ---- ---- X--- ---- ---- -X-- ---- /SET*/LD*/Q0
 2 ---- ---- ---- ---- ---- X--- -X-- -X-- -X-- -X-- /SET*/LD*CNT*CIN*UP
 3 ---- ---- ---- ---- ---- X--- -X-- X--- -X-- -X-- /SET*/LD*CNT*CIN*/UP

 8 ---- -X-- ---- ---- ---- -X-- ---- ---- -X-- ---- /SET*LD*/D1
 9 ---- ---X ---- ---- ---- X--- ---- ---- -X-- ---- /SET*/LD*/Q1
10 --X- ---- ---- ---- ---- X--- -X-- -X-- -X-- -X-- /SET*/LD*CNT*CIN*UP*Q0
11 ---X ---- ---- ---- ---- X--- -X-- X--- -X-- -X-- /SET*/LD*CNT*CIN*/UP*/Q0

16 ---- ---- -X-- ---- ---- -X-- ---- ---- -X-- ---- /SET*LD*/D2-7
17 ---- ---- ---X ---- ---- X--- ---- ---- -X-- ---- /SET*/LD*/Q2
18 --X- --X- ---- ---- ---- X--- -X-- -X-- -X-- -X-- /SET*/LD*CNT*CIN*UP*Q0*-
19 ---X ---X ---- ---- ---- X--- -X-- X--- -X-- -X-- /SET*/LD*CNT*CIN*/UP*/Q-

24 ---- ---- -X-- ---- ---- -X-- ---- ---- -X-- ---- /SET*LD*/D2-7
25 ---- ---- ---- ---X ---- X--- ---- ---- -X-- ---- /SET*/LD*/Q3
26 --X- --X- --X- ---- ---- X--- -X-- -X-- -X-- -X-- /SET*/LD*CNT*CIN*UP*Q0*-
27 ---X ---X ---X ---- ---- X--- -X-- X--- -X-- -X-- /SET*/LD*CNT*CIN*/UP*/Q-

32 ---- ---- -X-- ---- ---- -X-- ---- ---- -X-- ---- /SET*LD*/D2-7
33 ---- ---- ---- ---- ---X X--- ---- ---- -X-- ---- /SET*/LD*/Q4
34 --X- --X- --X- --X- ---- X--- -X-- -X-- -X-- -X-- /SET*/LD*CNT*CIN*UP*Q0*-
35 ---X ---X ---X ---X ---- X--- -X-- X--- -X-- -X-- /SET*/LD*CNT*CIN*/UP*/Q-

40 ---- ---- -X-- ---- ---- -X-- ---- ---- -X-- ---- /SET*LD*/D2-7
41 ---- ---- ---- ---- ---- X--X ---- ---- -X-- ---- /SET*/LD*/Q5
42 --X- --X- --X- --X- --X- X--- -X-- -X-- -X-- -X-- /SET*/LD*CNT*CIN*UP*Q0*-
43 ---X ---X ---X ---X ---X X--- -X-- X--- -X-- -X-- /SET*/LD*CNT*CIN*/UP*/Q-

48 ---- ---- -X-- ---- ---- -X-- ---- ---- -X-- ---- /SET*LD*/D2-7
49 ---- ---- ---- ---- ---- X--- ---X ---- -X-- ---- /SET*/LD*/Q6
50 --X- --X- --X- --X- --X- X-X- -X-- -X-- -X-- -X-- /SET*/LD*CNT*CIN*UP*Q0*-
51 ---X ---X ---X ---X ---X X--X -X-- X--- -X-- -X-- /SET*/LD*CNT*CIN*/UP*/Q-

56 ---- ---- -X-- ---- ---- -X-- ---- ---- -X-- ---- /SET*LD*/D2-7
57 ---- ---- ---- ---- ---- X--- ---- ---X -X-- ---- /SET*/LD*/Q7
58 --X- --X- --X- --X- --X- X-X- -XX- -X-- -X-- -X-- /SET*/LD*CNT*CIN*UP*Q0*-
59 ---X ---X ---X ---X ---X X--X -X-X X--- -X-- -X-- /SET*/LD*CNT*CIN*/UP*/Q-

64 ---- ---- ---- -X-- ---- -X-- ---- ---- -X-- ---- /SET*LD*/D8
65 ---- ---- ---- ---- ---- X--- ---- ---- -X-X ---- /SET*/LD*/Q8
66 --X- --X- --X- --X- --X- X-X- -XX- -XX- -X-- -X-- /SET*/LD*CNT*CIN*UP*Q0*-
67 ---X ---X ---X ---X ---X X--X -X-X X--X -X-- -X-- /SET*/LD*CNT*CIN*/UP*/Q-

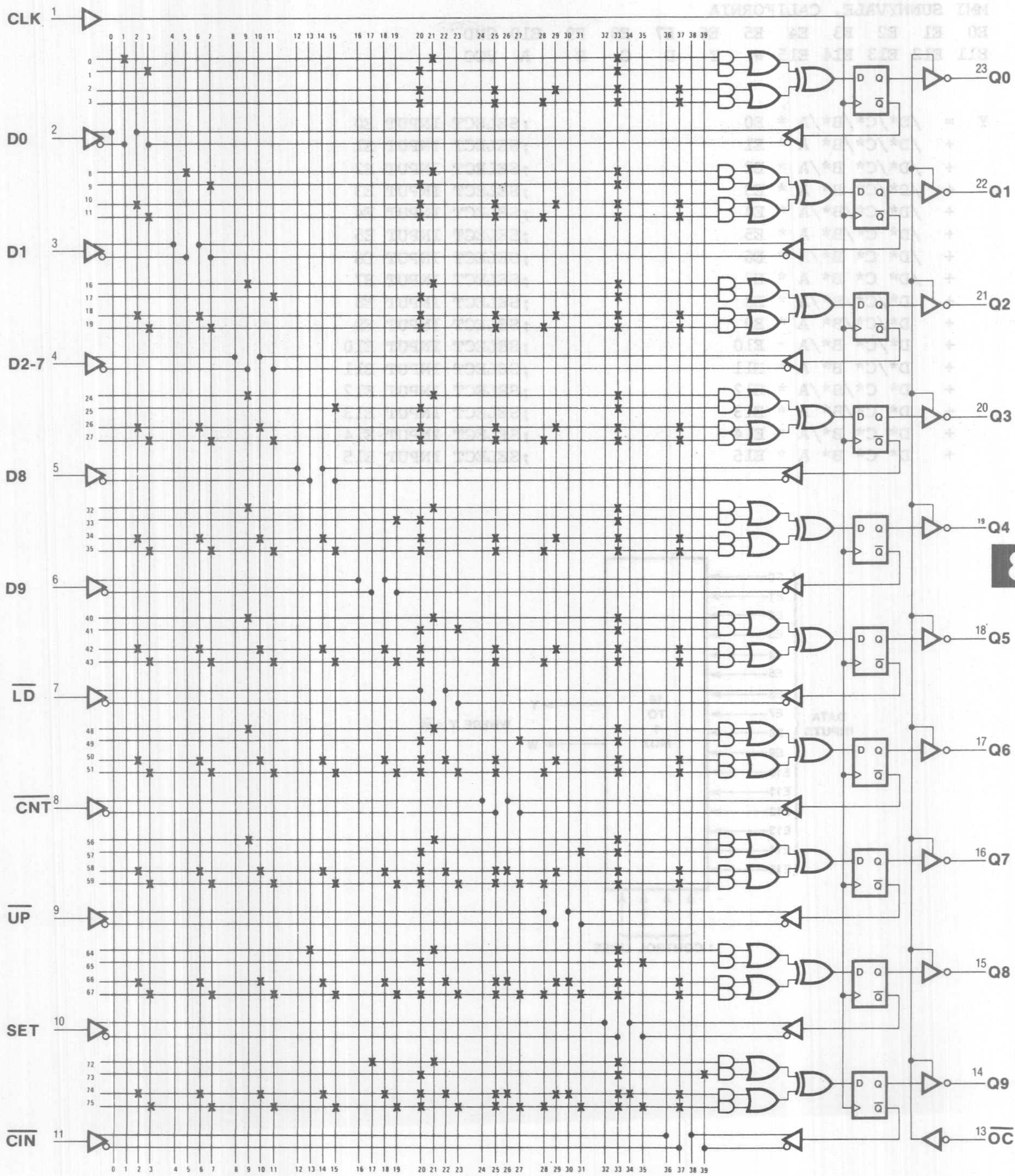
72 ---- ---- ---- ---- -X-- -X-- ---- ---- -X-- ---- /SET*LD*/D9
73 ---- ---- ---- ---- ---- X--- ---- ---- -X-- ---X /SET*/LD*/Q9
74 --X- --X- --X- --X- --X- X-X- -XX- -XX- -XX- -X-- /SET*/LD*CNT*CIN*UP*Q0*-
75 ---X ---X ---X ---X ---X X--X -X-X X--X -X-X -X-- /SET*/LD*CNT*CIN*/UP*/Q-
```

LEGEND: X : FUSE NOT BLOWN (L,N,0)   - : FUSE BLOWN   (H,P,1)

NUMBER OF FUSES BLOW = 1350

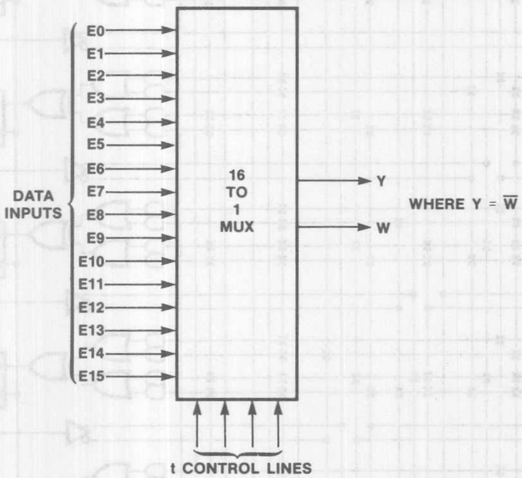
10-Bit Counter

Logic Diagram PAL20X10



```
PAL20C1                                          PAL DESIGN SPECIFICATION
74LS450                                      BIRKNER/KAZMI/BLASCO 02/19/81
16:1 MULTIPLEXER
MMI SUNNYVALE, CALIFORNIA
E0  E1  E2  E3  E4  E5  E6  E7  E8  E9  E10 GND
E11 E12 E13 E14 E15 W   Y   D   C   B    A  VCC

Y  =  /D*/C*/B*/A * E0                        ;SELECT INPUT E0
   +  /D*/C*/B* A * E1                        ;SELECT INPUT E1
   +  /D*/C* B*/A * E2                        ;SELECT INPUT E2
   +  /D*/C* B* A * E3                        ;SELECT INPUT E3
   +  /D* C*/B*/A * E4                        ;SELECT INPUT E4
   +  /D* C*/B* A * E5                        ;SELECT INPUT E5
   +  /D* C* B*/A * E6                        ;SELECT INPUT E6
   +  /D* C* B* A * E7                        ;SELECT INPUT E7
   +   D*/C*/B*/A * E8                        ;SELECT INPUT E8
   +   D*/C*/B* A * E9                        ;SELECT INPUT E9
   +   D*/C* B*/A * E10                       ;SELECT INPUT E10
   +   D*/C* B* A * E11                       ;SELECT INPUT E11
   +   D* C*/B*/A * E12                       ;SELECT INPUT E12
   +   D* C*/B* A * E13                       ;SELECT INPUT E13
   +   D* C* B*/A * E14                       ;SELECT INPUT E14
   +   D* C* B* A * E15                       ;SELECT INPUT E15
```



FUNCTION TABLE

```
D C B A E0 E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 Y W

;  SELECT   -----INPUTS----- OUTPUTS  COMMENTS
;                     111111
; D C B A   0123456789012345   Y  W
--------------------------------------------------------------
  L L L L   LHHHHHHHHHHHHHHH   L  H      INPUT E0 = 0
  L L L L   HLLLLLLLLLLLLLLL   H  L      INPUT E0 = 1
  L L L L   HHHHHHHHHHHHHHHH   H  L      TOGGLE OTHER LINES
  L L L H   HLHHHHHHHHHHHHHH   L  H      INPUT E1 = 0
  L L L H   LHLLLLLLLLLLLLLL   H  L      INPUT E1 = 1
  L L L H   HHHHHHHHHHHHHHHH   H  L      TOGGLE OTHER LINES
  L L H L   HHLHHHHHHHHHHHHH   L  H      INPUT E2 = 0
  L L H L   LLHLLLLLLLLLLLLL   H  L      INPUT E2 = 1
  L L H L   HHHHHHHHHHHHHHHH   H  L      TOGGLE OTHER LINES
  L L H H   HHHLHHHHHHHHHHHH   L  H      INPUT E3 = 0
  L L H H   LLLHLLLLLLLLLLLL   H  L      INPUT E3 = 1
  L L H H   HHHHHHHHHHHHHHHH   H  L      TOGGLE OTHER LINES
  L H L L   HHHHLHHHHHHHHHHH   L  H      INPUT E4 = 0
  L H L L   LLLLHLLLLLLLLLLL   H  L      INPUT E4 = 1
  L H L L   HHHHHHHHHHHHHHHH   H  L      TOGGLE OTHER LINES
  L H L H   HHHHHLHHHHHHHHHH   L  H      INPUT E5 = 0
  L H L H   LLLLLHLLLLLLLLLL   H  L      INPUT E5 = 1
  L H L H   HHHHHHHHHHHHHHHH   H  L      TOGGLE OTHER LINES
  L H H L   HHHHHHLHHHHHHHHH   L  H      INPUT E6 = 0
  L H H L   LLLLLLHLLLLLLLLL   H  L      INPUT E6 = 1
  L H H L   HHHHHHHHHHHHHHHH   H  L      TOGGLE OTHER LINES
  L H H H   HHHHHHHLHHHHHHHH   L  H      INPUT E7 = 0
  L H H H   LLLLLLLHLLLLLLLL   H  L      INPUT E7 = 1
  L H H H   HHHHHHHHHHHHHHHH   H  L      TOGGLE OTHER LINES
  H L L L   HHHHHHHHLHHHHHHH   L  H      INPUT E8 = 0
  H L L L   LLLLLLLLHLLLLLLL   H  L      INPUT E8 = 1
  H L L L   HHHHHHHHHHHHHHHH   H  L      TOGGLE OTHER LINES
  H L L H   HHHHHHHHHLHHHHHH   L  H      INPUT E9 = 0
  H L L H   LLLLLLLLLHLLLLLL   H  L      INPUT E9 = 1
  H L L H   HHHHHHHHHHHHHHHH   H  L      TOGGLE OTHER LINES
  H L H L   HHHHHHHHHHLHHHHH   L  H      INPUT E10 = 0
  H L H L   LLLLLLLLLLHLLLLL   H  L      INPUT E10 = 1
  H L H L   HHHHHHHHHHHHHHHH   H  L      TOGGLE OTHER LINES
  H L H H   HHHHHHHHHHHLHHHH   L  H      INPUT E11 = 0
  H L H H   LLLLLLLLLLLHLLLL   H  L      INPUT E11 = 1
  H L H H   HHHHHHHHHHHHHHHH   H  L      TOGGLE OTHER LINES
  H H L L   HHHHHHHHHHHHLHHH   L  H      INPUT E12 = 0
  H H L L   LLLLLLLLLLLLHLLL   H  L      INPUT E12 = 1
  H H L L   HHHHHHHHHHHHHHHH   H  L      TOGGLE OTHER LINES
  H H L H   HHHHHHHHHHHHHLHH   L  H      INPUT E13 = 0
  H H L H   LLLLLLLLLLLLLHLL   H  L      INPUT E13 = 1
  H H L H   HHHHHHHHHHHHHHHH   H  L      TOGGLE OTHER LINES
  H H H L   HHHHHHHHHHHHHHLH   L  H      INPUT E14 = 0
  H H H L   LLLLLLLLLLLLLLHL   H  L      INPUT E14 = 1
  H H H L   HHHHHHHHHHHHHHHH   H  L      TOGGLE OTHER LINES
  H H H H   HHHHHHHHHHHHHHHL   L  H      INPUT E15 = 0
  H H H H   LLLLLLLLLLLLLLLH   H  L      INPUT E15 = 1
  H H H H   HHHHHHHHHHHHHHHH   H  L      TOGGLE OTHER LINES
--------------------------------------------------------------
```

(Y) AND COMPLIMENT (W) OUTPUTS ARE PROVIDED. THE SELECT LINES A,B,C,D ARE ENCODED IN BINARY, WITH A REPRESENTING THE LSB AND D REPRESENTING THE MSB.

OPERATIONS TABLE:

INPUTS SELECT LINES				OUTPUTS	
D	C	B	A	W	Y
L	L	L	L	/E0	E0
L	L	L	H	/E1	E1
L	L	H	L	/E2	E2
L	L	H	H	/E3	E3
L	H	L	L	/E4	E4
L	H	L	H	/E5	E5
L	H	H	L	/E6	E6
L	H	H	H	/E7	E7
H	L	L	L	/E8	E8
H	L	L	H	/E9	E9
H	L	H	L	/E10	E10
H	L	H	H	/E11	E11
H	H	L	L	/E12	E12
H	H	L	H	/E13	E13
H	H	H	L	/E14	E14
H	H	H	H	/E15	E15

```
16:1 MULTIPLEXER

 1 01111111111X11111HL00001
 2 10000000000X00000LH00001
 3 11111111111X11111LH00001
 4 10111111111X11111HL00011
 5 01000000000X00000LH00011
 6 11111111111X11111LH00011
 7 11011111111X11111HL00101
 8 00100000000X00000LH00101
 9 11111111111X11111LH00101
10 11101111111X11111HL00111
11 00010000000X00000LH00111
12 11111111111X11111LH00111
13 11110111111X11111HL01001
14 00001000000X00000LH01001
15 11111111111X11111LH01001
16 11111011111X11111HL01011
17 00000100000X00000LH01011
18 11111111111X11111LH01011
19 11111101111X11111HL01101
20 00000010000X00000LH01101
21 11111111111X11111LH01101
22 11111110111X11111HL01111
23 00000001000X00000LH01111
24 11111111111X11111LH01111
25 11111111011X11111HL10001
26 00000000100X00000LH10001
27 11111111111X11111LH10001
28 11111111101X11111HL10011
29 00000000010X00000LH10011
30 11111111111X11111LH10011
31 11111111110X11111HL10101
32 00000000001X00000LH10101
33 11111111111X11111LH10101
34 11111111111X01111HL10111
35 00000000000X10000LH10111
36 11111111111X11111LH10111
37 11111111111X10111HL11001
38 00000000000X01000LH11001
39 11111111111X11111LH11001
40 11111111111X11011HL11011
41 00000000000X00100LH11011
42 11111111111X11111LH11011
43 11111111111X11101HL11101
44 00000000000X00010LH11101
45 11111111111X11111LH11101
46 11111111111X11110HL11111
47 00000000000X00001LH11111
48 11111111111X11111LH11111

PASS SIMULATION
```

```
16:1 MULTIPLEXER

                 11 1111 1111 2222 2222 2233 3333 3333
   0123 4567 8901 2345 6789 0123 4567 8901 2345 6789





32 --X- ---X ---X ---X ---X ---- ---- ---- ---- ---- /D*/C*/B*/A*E0
33 X--- --X- ---X ---X ---X ---- ---- ---- ---- ---- /D*/C*/B*A*E1
34 ---- X--X --X- ---X ---X ---- ---- ---- ---- ---- /D*/C*B*/A*E2
35 ---- --X- X-X- ---X ---X ---- ---- ---- ---- ---- /D*/C*B*A*E3
36 ---- ---X ---X X-X- ---X ---- ---- ---- ---- ---- /D*C*/B*/A*E4
37 ---- --X- ---X --X- X--X ---- ---- ---- ---- ---- /D*C*/B*A*E5
38 ---- ---X --X- --X- ---X X--- ---- ---- ---- ---- /D*C*B*/A*E6
39 ---- --X- --X- --X- ---X ---- X--- ---- ---- ---- /D*C*B*A*E7

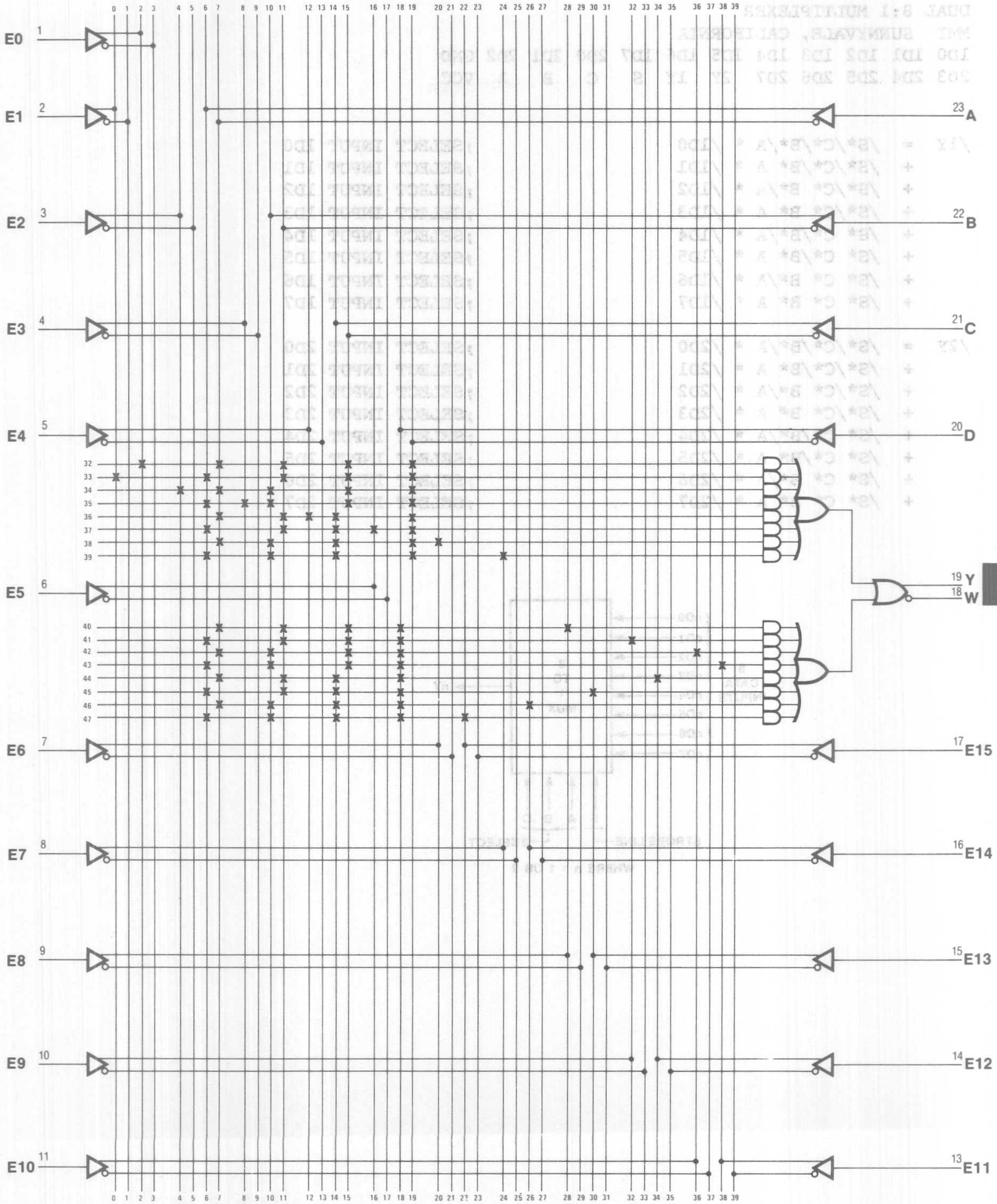
40 ---- ---X ---X ---X --X- ---- ---- X--- ---- ---- D*/C*/B*/A*E8
41 ---- --X- ---X ---X --X- ---- ---- ---- X--- ---- D*/C*/B*A*E9
42 ---- ---X --X- ---X --X- ---- ---- ---- ---- X--- D*/C*B*/A*E10
43 ---- --X- --X- ---X --X- ---- ---- ---- ---- --X- D*/C*B*A*E11
44 ---- ---X ---X --X- --X- ---- ---- ---- --X- ---- D*C*/B*/A*E12
45 ---- --X- ---X --X- --X- ---- ---- --X- ---- ---- D*C*/B*A*E13
46 ---- ---X --X- --X- --X- ---- --X- ---- ---- ---- D*C*B*/A*E14
47 ---- --X- --X- --X- --X- --X- ---- ---- ---- ---- D*C*B*A*E15




LEGEND:  X : FUSE NOT BLOWN (L,N,0)   - : FUSE BLOWN   (H,P,1)

NUMBER OF FUSES BLOW =  560
```

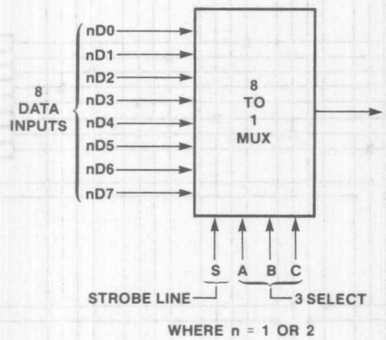
16:1 Multiplexer **Logic Diagram PAL20C1**



```
MMI  SUNNYVALE, CALIFORNIA
1D0 1D1 1D2 1D3 1D4 1D5 1D6 1D7 2D0 2D1 2D2 GND
2D3 2D4 2D5 2D6 2D7  2Y  1Y  S   C   B   A  VCC

/1Y  =  /S*/C*/B*/A * /1D0               ;SELECT INPUT 1D0
     +  /S*/C*/B* A * /1D1               ;SELECT INPUT 1D1
     +  /S*/C* B*/A * /1D2               ;SELECT INPUT 1D2
     +  /S*/C* B* A * /1D3               ;SELECT INPUT 1D3
     +  /S* C*/B*/A * /1D4               ;SELECT INPUT 1D4
     +  /S* C*/B* A * /1D5               ;SELECT INPUT 1D5
     +  /S* C* B*/A * /1D6               ;SELECT INPUT 1D6
     +  /S* C* B* A * /1D7               ;SELECT INPUT 1D7

/2Y  =  /S*/C*/B*/A * /2D0               ;SELECT INPUT 2D0
     +  /S*/C*/B* A * /2D1               ;SELECT INPUT 2D1
     +  /S*/C* B*/A * /2D2               ;SELECT INPUT 2D2
     +  /S*/C* B* A * /2D3               ;SELECT INPUT 2D3
     +  /S* C*/B*/A * /2D4               ;SELECT INPUT 2D4
     +  /S* C*/B* A * /2D5               ;SELECT INPUT 2D5
     +  /S* C* B*/A * /2D6               ;SELECT INPUT 2D6
     +  /S* C* B* A * /2D7               ;SELECT INPUT 2D7
```



FUNCTION TABLE

```
C B A 1D0 1D1 1D2 1D3 1D4 1D5 1D6 1D7 2D0 2D1 2D2 2D3 2D4 2D5 2D6 2D7 S 1Y 2Y

;  SEL   INPUTS    INPUTS    OUTPUTS      COMMENTS
;         1D-       2D-
; C B A 01234567  01234567   S  1Y  2Y
---------------------------------------------------------------
  L L L LHHHHHHH  LHHHHHHH   L   L   L     1D0=0 2D0=0
  L L L HLLLLLLL  LHHHHHHH   L   H   L     1D0=1 2D0=0
  L L L LHHHHHHH  HLLLLLLL   L   L   H     1D0=0 2D0=1
  L L L HLLLLLLL  HLLLLLLL   L   H   H     1D0=1 2D0=1
  L L L HHHHHHHH  HHHHHHHH   L   H   H     TOGGLE OTHER LINES
  L L H HLHHHHHH  HLHHHHHH   L   L   L     1D1=0 2D1=0
  L L H LHLLLLLL  HLHHHHHH   L   H   L     1D1=1 2D1=0
  L L H HLHHHHHH  LHLLLLLL   L   L   H     1D1=0 2D1=1
  L L H LHLLLLLL  LHLLLLLL   L   H   H     1D1=1 2D1=1
  L L H HHHHHHHH  HHHHHHHH   L   H   H     TOGGLE OTHER LINES
  L H L HHLHHHHH  HHLHHHHH   L   L   L     1D2=0 2D2=0
  L H L LLHLLLLL  HHLHHHHH   L   H   L     1D2=1 2D2=0
  L H L HHLHHHHH  LLHLLLLL   L   L   H     1D2=0 2D2=1
  L H L LLHLLLLL  LLHLLLLL   L   H   H     1D2=1 2D2=1
  L H L HHHHHHHH  HHHHHHHH   L   H   H     TOGGLE OTHER LINES
  L H H HHHLHHHH  HHHLHHHH   L   L   L     1D3=0 2D3=0
  L H H LLLHLLLL  HHHLHHHH   L   H   L     1D3=1 2D3=0
  L H H HHHLHHHH  LLLHLLLL   L   L   H     1D3=0 2D3=1
  L H H LLLHLLLL  LLLHLLLL   L   H   H     1D3=1 2D3=1
  L H H HHHHHHHH  HHHHHHHH   L   H   H     TOGGLE OTHER LINES
  H L L HHHHLHHH  HHHHLHHH   L   L   L     1D4=0 2D4=0
  H L L LLLLHLLL  HHHHLHHH   L   H   L     1D4=1 2D4=0
  H L L HHHHLHHH  LLLLHLLL   L   L   H     1D4=0 2D4=1
  H L L LLLLHLLL  LLLLHLLL   L   H   H     1D4=1 2D4=1
  H L L HHHHHHHH  HHHHHHHH   L   H   H     TOGGLE OTHER LINES
  H L H HHHHHLHH  HHHHHLHH   L   L   L     1D5=0 2D5=0
  H L H LLLLLHLL  HHHHHLHH   L   H   L     1D5=1 2D5=0
  H L H HHHHHLHH  LLLLLHLL   L   L   H     1D5=0 2D5=1
  H L H LLLLLHLL  LLLLLHLL   L   H   H     1D5=1 2D5=1
  H L H HHHHHHHH  HHHHHHHH   L   H   H     TOGGLE OTHER LINES
  H H L HHHHHHLH  HHHHHHLH   L   L   L     1D6=0 2D6=0
  H H L LLLLLLHL  HHHHHHLH   L   H   L     1D6=1 2D6=0
  H H L HHHHHHLH  LLLLLLHL   L   L   H     1D6=0 2D6=1
  H H L LLLLLLHL  LLLLLLHL   L   H   H     1D6=1 2D6=1
  H H L HHHHHHHH  HHHHHHHH   L   H   H     TOGGLE OTHER LINES
  H H H HHHHHHHL  HHHHHHHL   L   L   L     1D7=0 2D7=0
  H H H LLLLLLLH  HHHHHHHL   L   H   L     1D7=1 2D7=0
  H H H HHHHHHHL  LLLLLLLH   L   L   H     1D7=0 2D7=1
  H H H LLLLLLLH  LLLLLLLH   L   H   H     1D7=1 2D7=1
  H H H HHHHHHHH  HHHHHHHH   L   H   H     TOGGLE OTHER LINES
  X X X LLLLLLLL  LLLLLLLL   H   H   H     STROBE TEST 0
  X X X HHHHHHHH  HHHHHHHH   H   H   H     STROBE TEST 1
---------------------------------------------------------------
```

8

DESCRIPTION

THIS IS AN EXAMPLE OF A DUAL 8-TO-1 MULTIPLEXER USING A PAL20L2. A STROBE LINE (S) IS PROVIDED TO GATE THE OUTPUTS OFF (HIGH) WHEN THE STROBE INPUT IS HIGH THE SELECT LINES A,B,C ARE ENCODED IN BINARY, WITH A REPRESENTING THE LSB.

OPERATIONS TABLE:

-----INPUTS-----				OUTPUTS
SELECT			STROBE	
C	B	A	S	Y
X	X	X	H	L
L	L	L	L	D0
L	L	H	L	D1
L	H	L	L	D2
L	H	H	L	D3
H	L	L	L	D4
H	L	H	L	D5
H	H	L	L	D6
H	H	H	L	D7

8

DUAL 8:1 MULTIPLEXER

```
 1 01111111011X11111LL00001
 2 10000000011X11111LH00001
 3 01111111100X00000HL00001
 4 10000000100X00000HH00001
 5 11111111111X11111HH00001
 6 10111111101X11111LL00011
 7 01000000101X11111LH00011
 8 10111111010X00000HL00011
 9 01000000010X00000HH00011
10 11111111111X11111HH00011
11 11011111110X11111LL00101
12 00100000110X11111LH00101
13 11011111001X00000HL00101
14 00100000001X00000HH00101
15 11111111111X11111HH00101
16 11101111111X01111LL00111
17 00010000111X01111LH00111
18 11101111000X10000HL00111
19 00010000000X10000HH00111
20 11111111111X11111HH00111
21 11110111111X10111LL01001
22 00001000111X10111LH01001
23 11110111000X01000HL01001
24 00001000000X01000HH01001
25 11111111111X11111HH01001
26 11111011111X11011LL01011
27 00000100111X11011LH01011
28 11111011000X00100HL01011
29 00000100000X00100HH01011
30 11111111111X11111HH01011
31 11111101111X11101LL01101
32 00000010111X11101LH01101
33 11111101000X00010HL01101
34 00000010000X00010HH01101
35 11111111111X11111HH01101
36 11111110111X11110LL01111
37 00000001111X11110LH01111
38 11111110000X00001HL01111
39 00000001000X00001HH01111
40 11111111111X11111HH01111
41 00000000000X00000HH1XXX1
42 11111111111X11111HH1XXX1
```

PASS SIMULATION

```
     0123 4567 8901 2345 6789 0123 4567 8901 2345 6789


32 ---X ---X ---X ---X ---X ---- ---- ---- ---- ---- /S*/C*/B*/A*/1D0
33 -X-- --X- ---X ---X ---X ---- ---- ---- ---- ---- /S*/C*/B*A*/1D1
34 ---- -X-X --X- ---X ---X ---- ---- ---- ---- ---- /S*/C*B*/A*/1D2
35 ---- --X- -XX- ---X ---X ---- ---- ---- ---- ---- /S*/C*B*A*/1D3
36 ---- ---X ---X -XX- ---X ---- ---- ---- ---- ---- /S*C*/B*/A*/1D4
37 ---- --X- ---X --X- -X-X ---- ---- ---- ---- ---- /S*C*/B*A*/1D5
38 ---- ---X --X- --X- ---X -X-- ---- ---- ---- ---- /S*C*B*/A*/1D6
39 ---- --X- --X- --X- ---X ---- -X-- ---- ---- ---- /S*C*B*A*/1D7

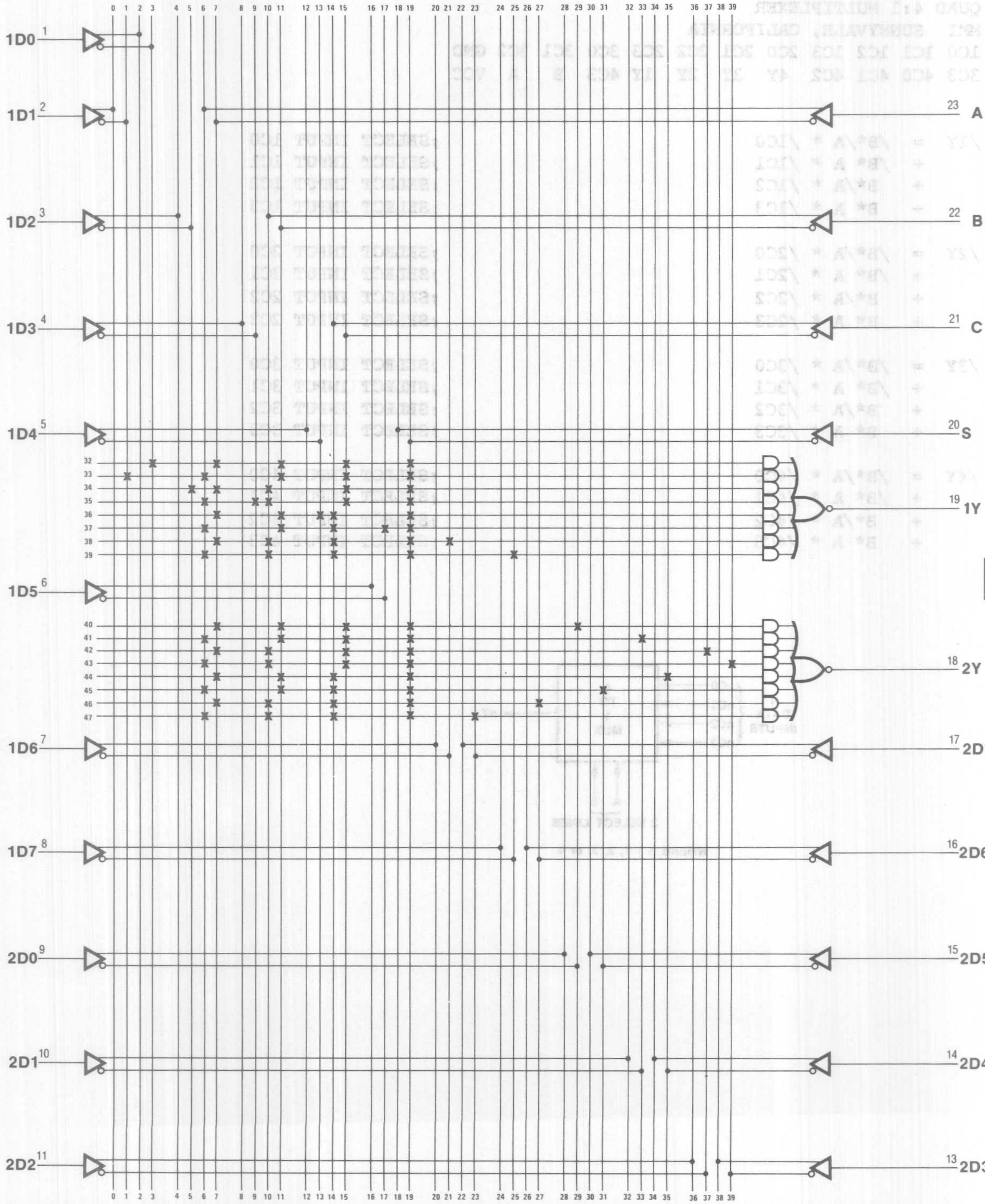
40 ---- ---X ---X ---X ---X ---- ---- -X-- ---- ---- /S*/C*/B*/A*/2D0
41 ---- --X- ---X ---X ---X ---- ---- ---- -X-- ---- /S*/C*/B*A*/2D1
42 ---- ---X --X- ---X ---X ---- ---- ---- ---- -X-- /S*/C*B*/A*/2D2
43 ---- --X- --X- ---X ---X ---- ---- ---- ---- ---X /S*/C*B*A*/2D3
44 ---- ---X ---X --X- ---X ---- ---- ---- ---X ---- /S*C*/B*/A*/2D4
45 ---- --X- ---X --X- ---X ---- ---- ---X ---- ---- /S*C*/B*A*/2D5
46 ---- ---X --X- --X- ---X ---- ---X ---- ---- ---- /S*C*B*/A*/2D6
47 ---- --X- --X- --X- ---X ---X ---- ---- ---- ---- /S*C*B*A*/2D7




LEGEND:  X : FUSE NOT BLOWN (L,N,0)   - : FUSE BLOWN   (H,P,1)

NUMBER OF FUSES BLOW =  560
```

Dual 8:1 Multiplexer **Logic Diagram PAL20L2**



8

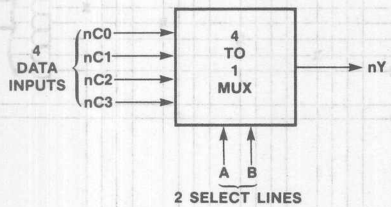
```
PAL18L4                                          PAL DESIGN SPECIFICATION
P80    (74LS453)                          BIRKNER/KAZMI/BLASCO 03/10/81
QUAD 4:1 MULTIPLEXER
MMI   SUNNYVALE, CALIFORNIA
1C0 1C1 1C2 1C3 2C0 2C1 2C2 2C3 3C0 3C1 3C2 GND
3C3 4C0 4C1 4C2  4Y  3Y  2Y  1Y 4C3  B   A  VCC

/1Y  =  /B*/A * /1C0                            ;SELECT INPUT 1C0
     +  /B* A * /1C1                            ;SELECT INPUT 1C1
     +   B*/A * /1C2                            ;SELECT INPUT 1C2
     +   B* A * /1C3                            ;SELECT INPUT 1C3

/2Y  =  /B*/A * /2C0                            ;SELECT INPUT 2C0
     +  /B* A * /2C1                            ;SELECT INPUT 2C1
     +   B*/A * /2C2                            ;SELECT INPUT 2C2
     +   B* A * /2C3                            ;SELECT INPUT 2C3

/3Y  =  /B*/A * /3C0                            ;SELECT INPUT 3C0
     +  /B* A * /3C1                            ;SELECT INPUT 3C1
     +   B*/A * /3C2                            ;SELECT INPUT 3C2
     +   B* A * /3C3                            ;SELECT INPUT 3C3

/4Y  =  /B*/A * /4C0                            ;SELECT INPUT 4C0
     +  /B* A * /4C1                            ;SELECT INPUT 4C1
     +   B*/A * /4C2                            ;SELECT INPUT 4C2
     +   B* A * /4C3                            ;SELECT INPUT 4C3
```



WHERE n = 1, 2, 3, or 4

FUNCTION TABLE

```
B A 1C0 1C1 1C2 1C3 2C0 2C1 2C2 2C3 3C0 3C1 3C2 3C3 4C0 4C1 4C2 4C3 1Y 2Y 3Y 4Y

; SEL   --------INPUTS--------   --OUTPUTS--      COMMENTS
;        1C    2C    3C    4C
; B A   0123  0123  0123  0123  1Y 2Y 3Y 4Y
------------------------------------------------------------
  L L   LHHH  HHHH  HHHH  HHHH  L  H  H  H       1C0=0
  L L   HHHH  LHHH  HHHH  HHHH  H  L  H  H       2C0=0
  L L   HHHH  HHHH  LHHH  HHHH  H  H  L  H       3C0=0
  L L   HHHH  HHHH  HHHH  LHHH  H  H  H  L       4C0=0
  L L   HLLL  LLLL  LLLL  LLLL  H  L  L  L       1C0=1
  L L   LLLL  HLLL  LLLL  LLLL  L  H  L  L       2C0=1
  L L   LLLL  LLLL  HLLL  LLLL  L  L  H  L       3C0=1
  L L   LLLL  LLLL  LLLL  HLLL  L  L  L  H       4C0=1
  L L   HHHH  HHHH  HHHH  HHHH  H  H  H  H       TOGGLE LINES
  L H   HLHH  HHHH  HHHH  HHHH  L  H  H  H       1C1=0
  L H   HHHH  HLHH  HHHH  HHHH  H  L  H  H       2C1=0
  L H   HHHH  HHHH  HLHH  HHHH  H  H  L  H       3C1=0
  L H   HHHH  HHHH  HHHH  HLHH  H  H  H  L       4C1=0
  L H   LHLL  LLLL  LLLL  LLLL  H  L  L  L       1C1=1
  L H   LLLL  LHLL  LLLL  LLLL  L  H  L  L       2C1=1
  L H   LLLL  LLLL  LHLL  LLLL  L  L  H  L       3C1=1
  L H   LLLL  LLLL  LLLL  LHLL  L  L  L  H       4C1=1
  L H   HHHH  HHHH  HHHH  HHHH  H  H  H  H       TOGGLE LINES
  H L   HHLH  HHHH  HHHH  HHHH  L  H  H  H       1C2=0
  H L   HHHH  HHLH  HHHH  HHHH  H  L  H  H       2C2=0
  H L   HHHH  HHHH  HHLH  HHHH  H  H  L  H       3C2=0
  H L   HHHH  HHHH  HHHH  HHLH  H  H  H  L       4C2=0
  H L   LLHL  LLLL  LLLL  LLLL  H  L  L  L       1C2=1
  H L   LLLL  LLHL  LLLL  LLLL  L  H  L  L       2C2=1
  H L   LLLL  LLLL  LLHL  LLLL  L  L  H  L       3C2=1
  H L   LLLL  LLLL  LLLL  LLHL  L  L  L  H       4C2=1
  H L   HHHH  HHHH  HHHH  HHHH  H  H  H  H       TOGGLE LINES
  H H   HHHL  HHHH  HHHH  HHHH  L  H  H  H       1C3=0
  H H   HHHH  HHHL  HHHH  HHHH  H  L  H  H       2C3=0
  H H   HHHH  HHHH  HHHL  HHHH  H  H  L  H       3C3=0
  H H   HHHH  HHHH  HHHH  HHHL  H  H  H  L       4C3=0
  H H   LLLH  LLLL  LLLL  LLLL  H  L  L  L       1C3=1
  H H   LLLL  LLLH  LLLL  LLLL  L  H  L  L       2C3=1
  H H   LLLL  LLLL  LLLH  LLLL  L  L  H  L       3C3=1
  H H   LLLL  LLLL  LLLL  LLLH  L  L  L  H       4C3=1
  H H   HHHH  HHHH  HHHH  HHHH  H  H  H  H       TOGGLE LINES
  ----------------------------------------------------------
```

8

LINES A,B ARE ENCODED IN BINARY, WITH A REPRESENTING THE LSB.

OPERATIONS TABLE:

INPUT SELECT B	A	OUTPUTS Y
L	L	C0
L	H	C1
H	L	C2
H	H	C3

```
QUAD 4:1 MULTIPLEXER

 1 01111111111X1111HHHL1001
 2 11110111111X1111HHLH1001
 3 11111111011X1111HLHH1001
 4 11111111111X1011LHHH1001
 5 10000000000X0000LLLH0001
 6 00001000000X0000LLHL0001
 7 00000000100X0000LHLL0001
 8 00000000000X0100HLLL0001
 9 11111111111X1111HHHH1001
10 10111111111X1111HHHL1011
11 11111011111X1111HHLH1011
12 11111111101X1111HLHH1011
13 11111111111X1101LHHH1011
14 01000000000X0000LLLH0011
15 00000100000X0000LLHL0011
16 00000000010X0000LHLL0011
17 00000000000X0010HLLL0011
18 11111111111X1111HHHH1011
19 11011111111X1111HHHL1101
20 11111101111X1111HHLH1101
21 11111111110X1111HLHH1101
22 11111111111X1110LHHH1101
23 00100000000X0000LLLH0101
24 00000010000X0000LLHL0101
25 00000000001X0000LHLL0101
26 00000000000X0001HLLL0101
27 11111111111X1111HHHH1101
28 11101111111X1111HHHL1111
29 11111110111X1111HHLH1111
30 11111111111X0111HLHH1111
31 11111111111X1111LHHH0111
32 00010000000X0000LLLH0111
33 00000001000X0000LLHL0111
34 00000000000X1000LHLL0111
35 00000000000X0000HLLL1111
36 11111111111X1111HHHH1111

PASS SIMULATION
```

8

QUAD 4:1 MULTIPLEXER

```
               11 1111 1111 2222 2222 2233 3333 3333
   0123 4567 8901 2345 6789 0123 4567 8901 2345 6789




24 ---X ---X ---X ---- --   --   ---- ---- ---- ---- /B*/A*/1C0
25 -X-- --X- ---X ---- --   --   ---- ---- ---- ---- /B*A*/1C1
26 ---- -X-X --X- ---- --   --   ---- ---- ---- ---- B*/A*/1C2
27 ---- --X- -XX- ---- --   --   ---- ---- ---- ---- B*A*/1C3

32 ---- ---X ---X -X-- --   --   ---- ---- ---- ---- /B*/A*/2C0
33 ---- --X- ---X ---- -X   --   ---- ---- ---- ---- /B*A*/2C1
34 ---- ---X --X- ---- --   -X   ---- ---- ---- ---- B*/A*/2C2
35 ---- --X- --X- ---- --   --   -X-- ---- ---- ---- B*A*/2C3

40 ---- ---X ---X ---- --   --   ---- -X-- ---- ---- /B*/A*/3C0
41 ---- --X- ---X ---- --   --   ---- ---- -X-- ---- /B*A*/3C1
42 ---- ---X --X- ---- --   --   ---- ---- ---- -X-- B*/A*/3C2
43 ---- --X- --X- ---- --   --   ---- ---- ---- ---X B*A*/3C3

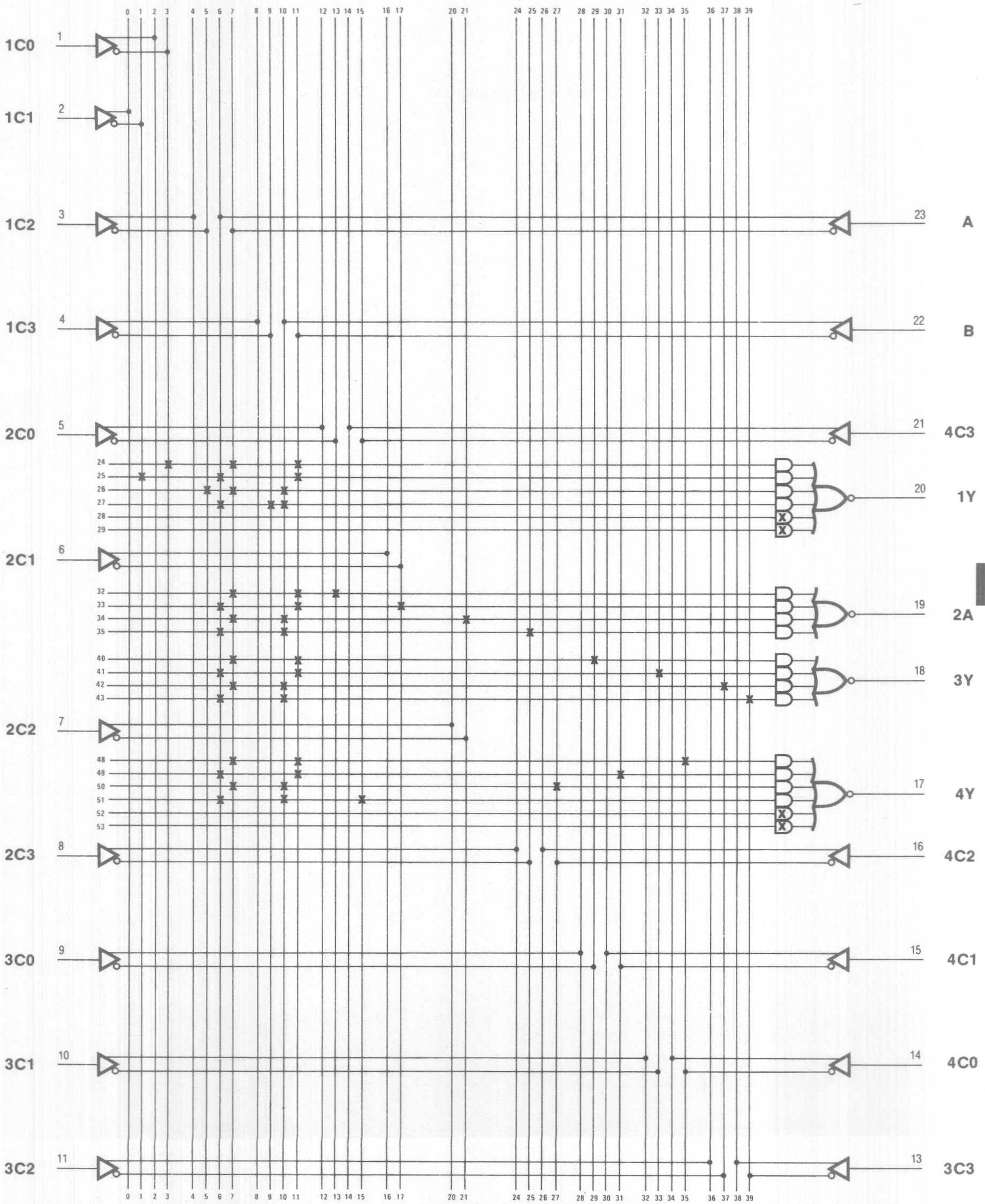
48 ---- ---X ---X ---- --   --   ---- ---- ---X ---- /B*/A*/4C0
49 ---- --X- ---X ---- --   --   ---- ---X ---- ---- /B*A*/4C1
50 ---- ---X --X- ---- --   --   ---X ---- ---- ---- B*/A*/4C2
51 ---- --X- --X- ---X --   --   ---- ---- ---- ---- B*A*/4C3
```

LEGEND: X : FUSE NOT BLOWN (L,N,0)   - : FUSE BLOWN   (H,P,1)

NUMBER OF FUSES BLOW = 592

Quad 4:1 Multiplexer

Logic Diagram PAL18L4



The following selection guides are designed to simplify the choice of the particular function to fit the specific application.

First-In First-Out (FIFO)

ORGANIZATION	FREQUENCY	CASCASDABLE	STAND ALONE
COM 64x4	15 MHz	C67401A	67401A
COM 64x5	15 MHz	C67402A	67402A
COM 64x4	10 MHz	C67401	67401
COM 64x5	10 MHz	C67402	67402
MIL 64x4	10 MHz	C57401A	57401A
MIL 64x5	10 MHz	C57402A	57402A
MIL 64x4	7 MHz	C57401	57401
MIL 64x5	7 MHz	C57402	57402

First-In First-Out (FIFO) 64x4 64x5 Serial Cascadable Memory C5/C67401A C5/C67402A C5/C67401 C5/C67402

Features/Benefits

- Choice of 15 and 10 MHz shift out guaranteed rates
- Choice of 4 bit or 5 bit data width
- TTL inputs and outputs
- Readily expandable in the word and bit dimensions
- Output pins directly opposite corresponding input pins
- Asynchronous or synchronous operation
- Pin compatible with Fairchild's F3341 MOS FIFO and many times as fast

Description

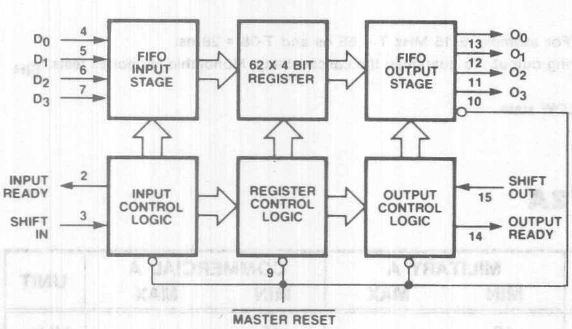
The C5/C67401A/2A/1/2 are expandable "fall-through" high speed First-In First-Out (FIFO) memory organized 64 words by 4-bits and 64 words by 5-bits respectively. A 15 MHz data rate allows usage in high speed tape or disc controllers and communication buffer applications.

Ordering Information

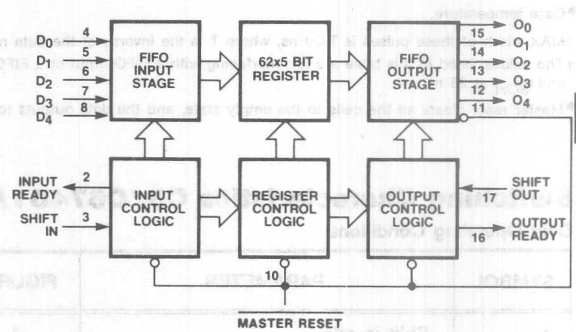
PART NUMBER	PKG	TEMP	DESCRIPTION
C57401	J,F	MIL	7 MHz 64x4 FIFO
C67401	J	COM	10 MHz 64x4 FIFO
C57402	J,F	MIL	7 MHz 64x5 FIFO
C67402	J	COM	10 MHz 64x5 FIFO
C57401A	J,F	MIL	10 MHz 64x4 FIFO
C67401A	J	COM	15 MHz 64x4 FIFO
C57402A	J,F	MIL	10 MHz 64x5 FIFO
C67402A	J	COM	15 MHz 64x5 FIFO

Block Diagrams

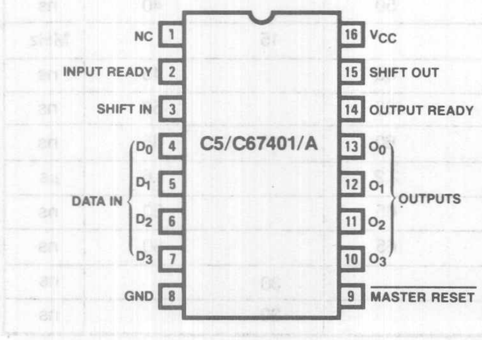
C5/C67401/A 64x4

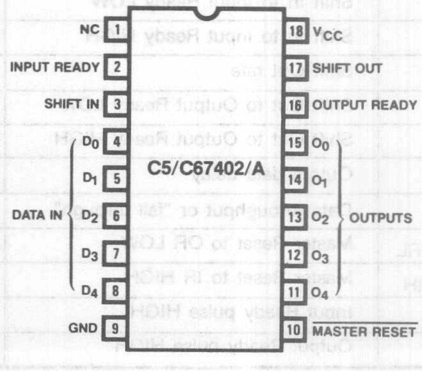


C5/C67402/A 64x5



Pin Configurations





9

Off-state output voltage 5.5V
Storage temperature .... –65° to +150°C

Operating Conditions C5/C67401A/2A

SYMBOL	PARAMETER	FIGURE	MILITARY A MIN	MILITARY A NOM	MILITARY A MAX	COMMERCIAL A MIN	COMMERCIAL A NOM	COMMERCIAL A MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		–55		*125	0		75	°C
t_{SIH}††	Shift in HIGH time	1	35			23		28†	ns
t_{SIL}	Shift in LOW time	1	35			25			ns
t_{IDS}	Input data set up	1	0			0			ns
t_{IDH}	Input data hold time	1	45			40			ns
t_{SOH}††	Shift Out HIGH time	6	35			23		28	ns
t_{SOL}	Shift Out LOW time	6	35			25			ns
t_{MRW}	Master Reset pulse**	11	40			35			ns
t_{MRS}	Master Reset to SI	11	45			35			ns

*Case temperature.

†MAX width of these pulses is T-38 ns, where T is the inverse of the data rate. For example at 15 MHz T = 66 ns and T-38 = 28 ns.

††The values listed in this table are for interfacing with a FIFO input or a FIFO/string output. To guarantee the cascadability, Monolithic Memories tests t_{SIH} and t_{SOH} at 23 ns.

**Master reset clears all the cells to the empty state, and the data outputs to a LOW state.

Switching Characteristics C5/C67401A/2A

Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY A MIN	MILITARY A MAX	COMMERCIAL A MIN	COMMERCIAL A MAX	UNIT
f_{IN}	Shift in rate	1	10		15		MHz
t_{IRL}	Shift In to Input Ready LOW	1		50		40	ns
t_{IRH}	Shift In to Input Ready HIGH	1		50		40	ns
f_{OUT}	Shift Out rate	6	10		15		MHz
t_{ORL}	Shift Out to Output Ready LOW	6		65		45	ns
t_{ORH}	Shift Out to Output Ready HIGH	6		65		50	ns
t_{OD}	Output data delay	6	10	60	10	45	ns
t_{PT}	Data throughput or "fall through"	4, 9		2.2		1.6	μs
t_{MRORL}	Master Reset to OR LOW	11		65		60	ns
t_{MRIRH}	Master Reset to IR HIGH	11		65		60	ns
t_{IPH}	Input Ready pulse HIGH	4	30		30		ns
t_{OPH}	Output Ready pulse HIGH	9	30		30		ns

Absolute Maximum Ratings

Supply voltage V_{CC}	7V
Input voltage	7V
Off-state output voltage	5.5V
Storage temperature	−65° to +150°C

Operating Conditions C5/C67401/2

SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		*125	0		75	°C
t_{SIH}†	Shift in HIGH time	1	45			35			ns
t_{SIL}	Shift in LOW time	1	45			35			ns
t_{IDS}	Input data set up	1	0			0			ns
t_{IDH}	Input data hold time	1	55			45			ns
t_{SOH}†	Shift Out HIGH time	6	45			35			ns
t_{SOL}	Shift Out LOW time	6	45			35			ns
t_{MRW}	Master Reset pulse††	11	30			35			ns
t_{MRS}	Master Reset to SI	11	45			35			ns

* Case temperature.

†The values listed in this table are for interfacing to a FIFO input or a FIFO/string output. To guarantee the cascadability, Monolithic Memories tests t_{SIH} and t_{SOH} at 25 ns.

††Master reset clears all the cells to the empty state, and the data outputs to a LOW state.

9

Switching Characteristics C5/C67401/2

Over Operating Conditions

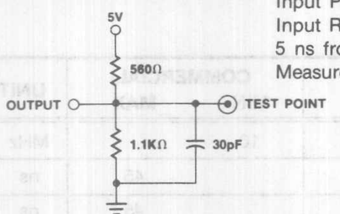
SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	7		10		MHz
t_{IRL}	Shift In to Input Ready LOW	1		60		45	ns
t_{IRH}	Shift In to Input Ready HIGH	1		60		45	ns
f_{OUT}	Shift Out rate	6	7		10		MHz
t_{ORL}	Shift Out to Output Ready LOW	6		65		55	ns
t_{ORH}	Shift Out to Output Ready HIGH	6		70		60	ns
t_{OD}	Output data delay	6	10	65	10	55	ns
t_{PT}	Data throughput or "fall through"	4, 9		4		3	μs
t_{MRORL}	Master Reset to OR LOW	11		65		60	ns
t_{MRIRH}	Master Reset to IR HIGH	11		65		60	ns
t_{IPH}	Input Ready pulse HIGH	4	30		30		ns
t_{OPH}	Output Ready pulse HIGH	9	30		30		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL1}	Low-level input current: D_0–D_4, $\overline{MR}$	V_{CC} = MAX	V_I = 0.45V			−0.8	mA
I_{IL2}	Low-level input current: SI, SO	V_{CC} = MAX	V_I = 0.45V			−1.6	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V			50	μA
I_I	Maximum input current	VCC = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −0.9mA	2.4			V
I_{OS}	Output short-circuit current *	V_{CC} = MAX	V_0 = 0V	−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX, Inputs low, outputs open	C5/67401			160	mA
			C5/67402			180	mA
			C5/67401A			170	mA
			C5/67402A			190	mA

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Standard Test Load



Input Pulse Amplitude = 3V
Input Rise and Fall Time
5 ns from 1 V to 2 V
Measurements made at 1.5 V

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 11) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

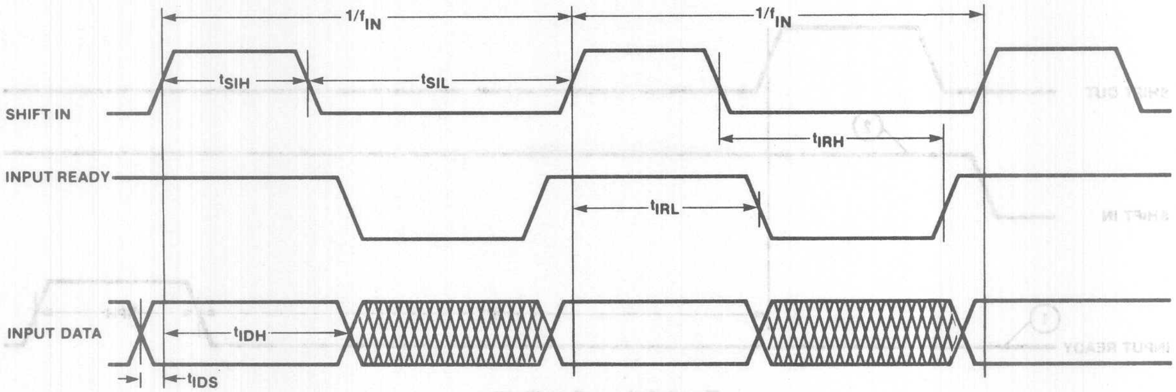


Figure 1. Input Timing

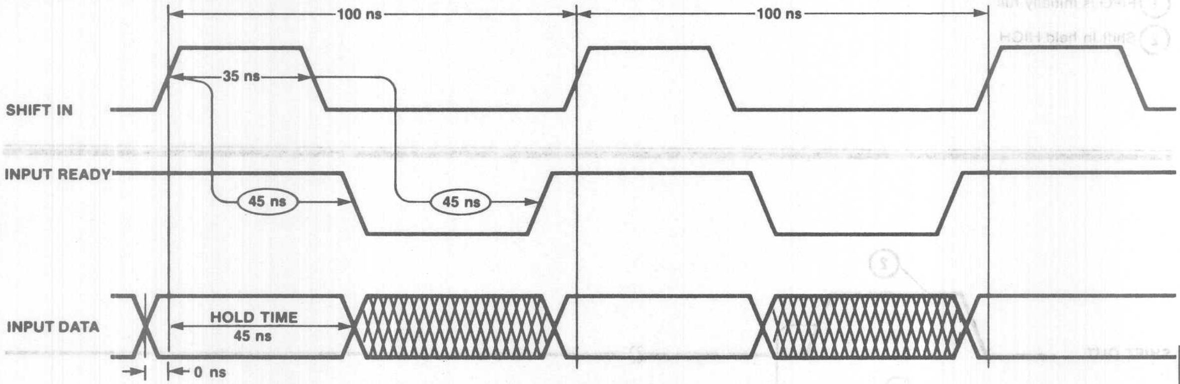


Figure 2. Typical Waveforms for 10 MHz Shift In Data Rate (C67401)

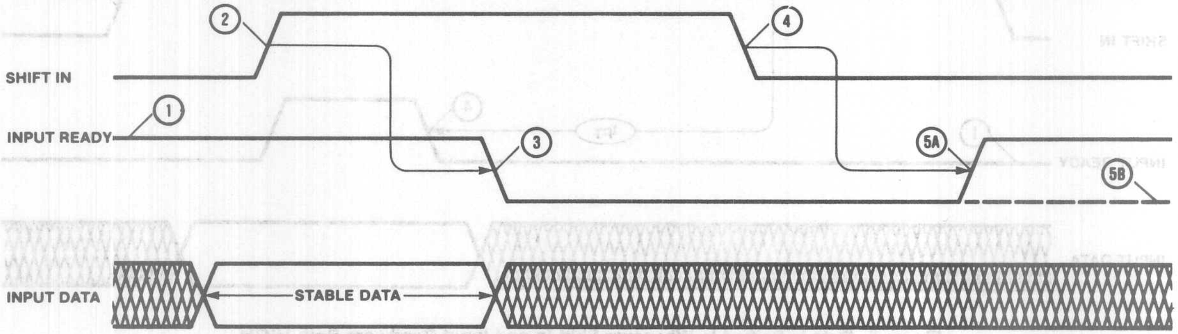


Figure 3. The Mechanism of Shifting Data into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied.

(2) Input Data is loaded into the first word.

(3) Input Ready goes LOW indicating the first word is full.

(4) The Data from the first word is released for "fall-through" to second word.

(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

(5B) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

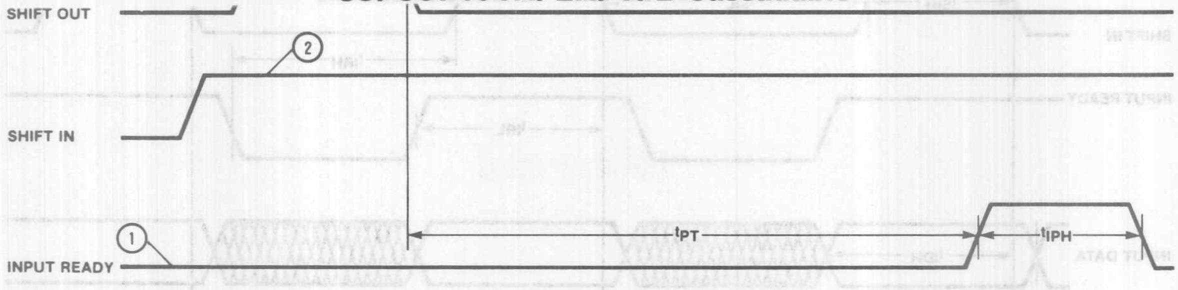


Figure 4. t_{IPH} Specification

(1) FIFO is initially full.

(2) Shift In held HIGH.

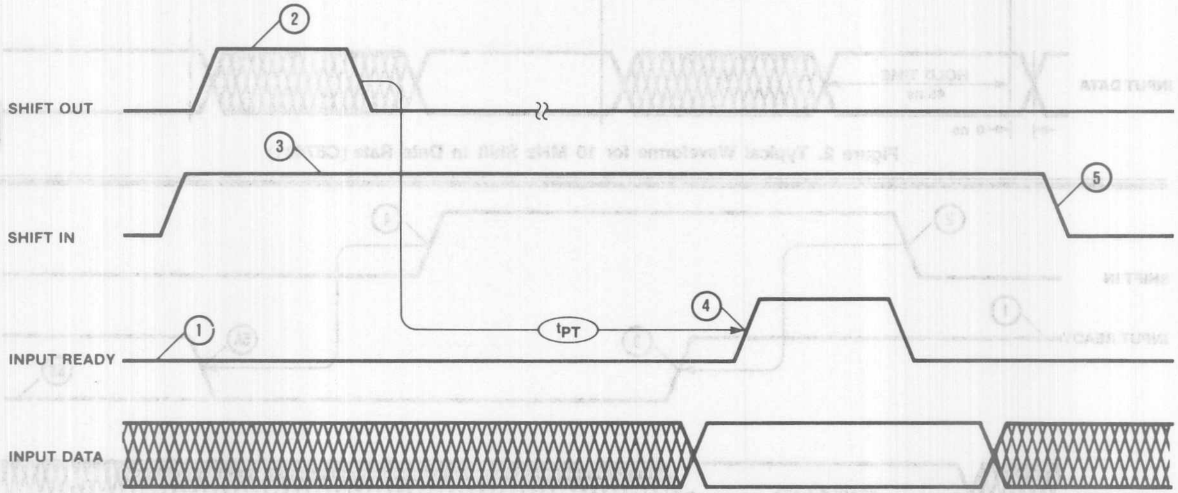


Figure 5. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

(1) FIFO is initially full.

(2) Shift Out pulse is applied. An empty location start "bubbling" to the front.

(3) Shift In is held HIGH.

(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

(5) The Data from the first word is released for "fall through" to second word.

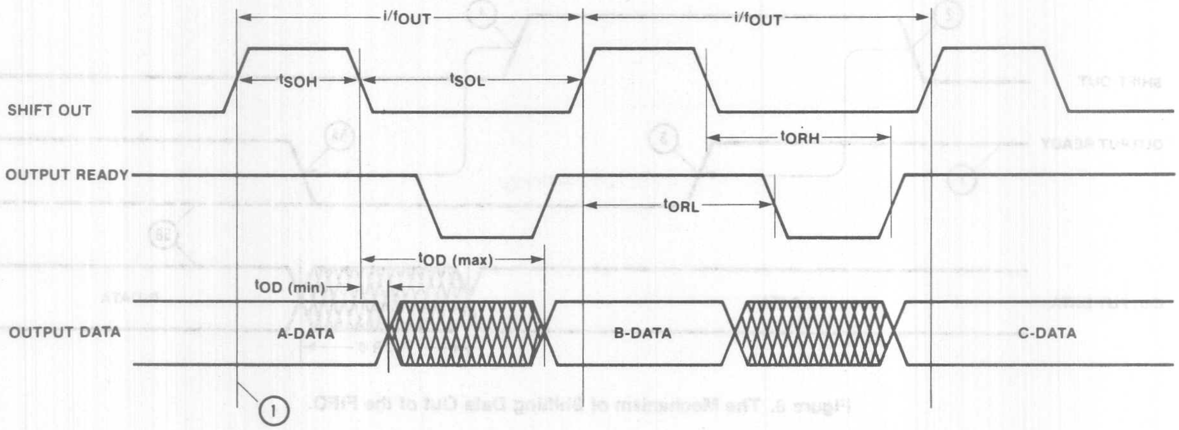


Figure 6. Output Timing

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

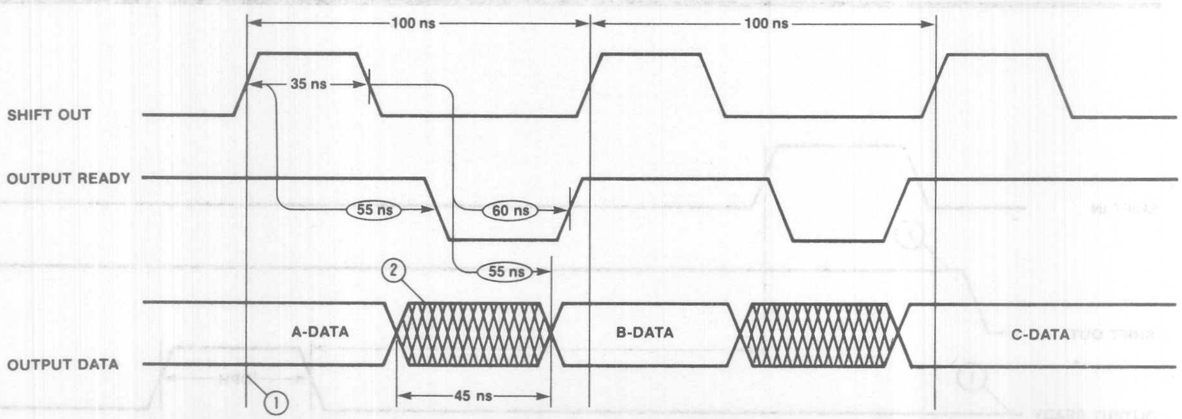


Figure 7. Typical Waveforms for 10 MHz Shift Out Data Rate (C67401)

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

(2) Data in the crosshatched region may be A or B Data.

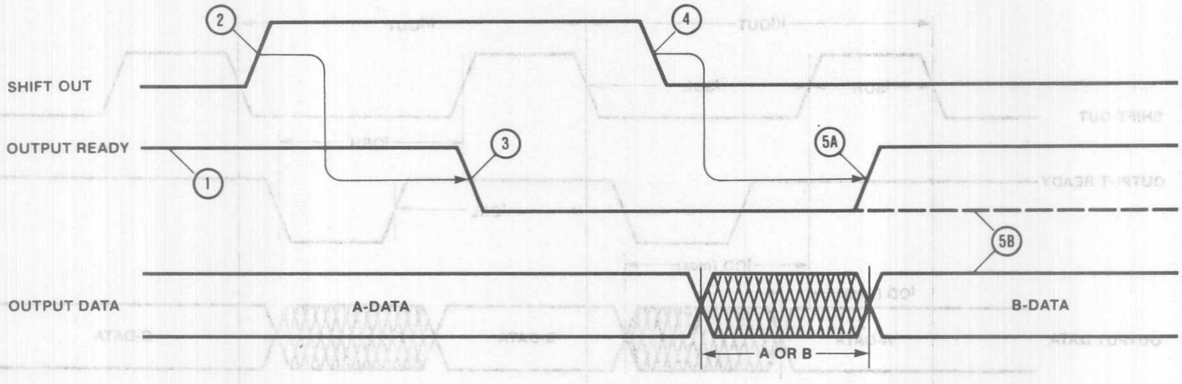


Figure 8. The Mechanism of Shifting Data Out of the FIFO.

1 Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.

2 Shift Out goes HIGH causing the next step.

3 Output Ready goes LOW.

4 Contents of word 62 (B-DATA) is released for "fall through" to word 63.

5A Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.

5B If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.

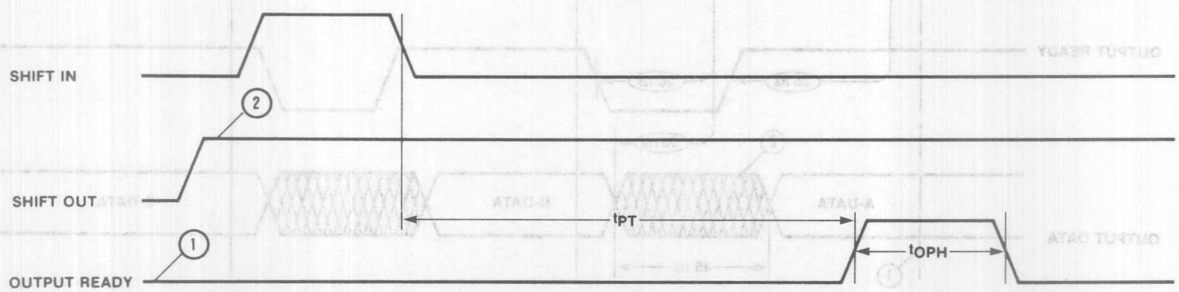


Figure 9. t_{PT} and t_{OPH} Specification

1 FIFO initially empty.

2 Shift Out held HIGH.

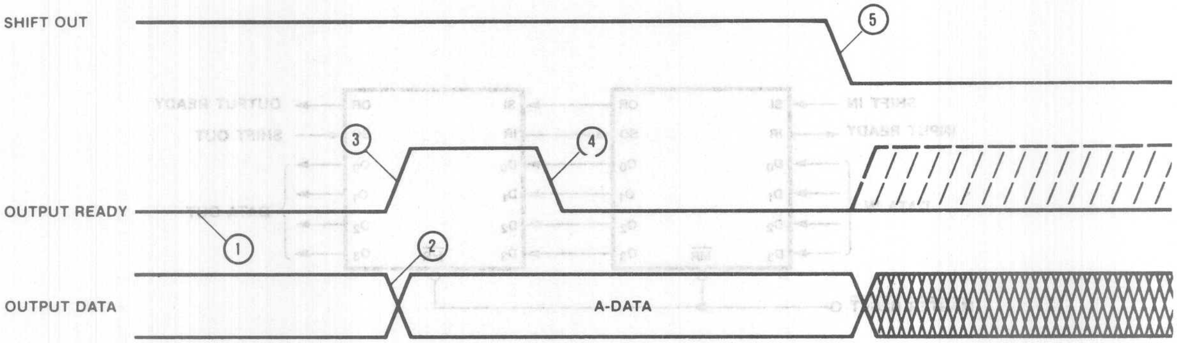


Figure 10. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

1. Word 63 is empty.
2. New data (A) arrives at the outputs (word 63).
3. Output Ready goes HIGH indicating the arrival of the new data.
4. Since Shift Out is held HIGH, Output Ready goes immediately LOW.
5. As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.

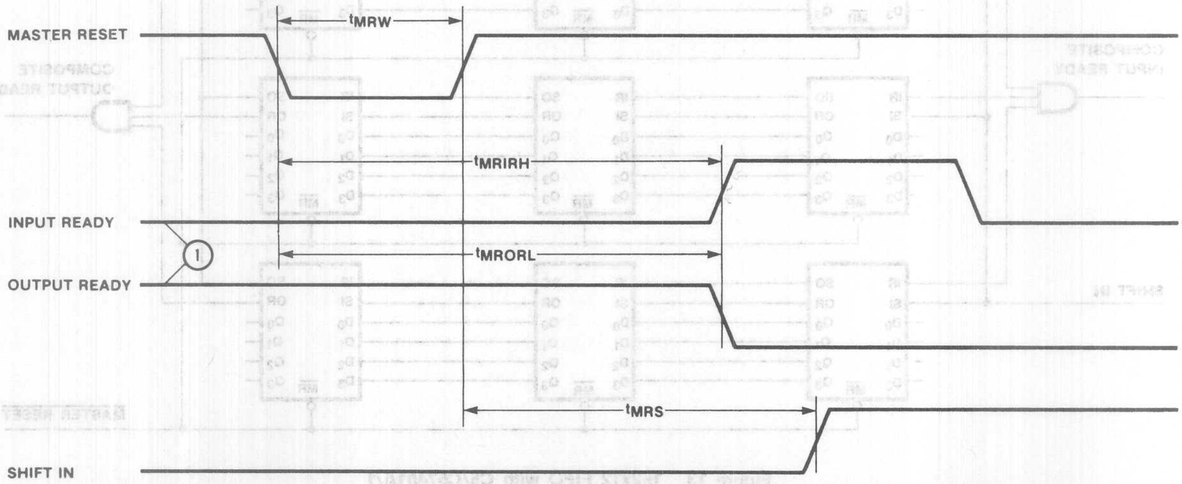


Figure 11. Master Reset Timing

1. FIFO initially full.

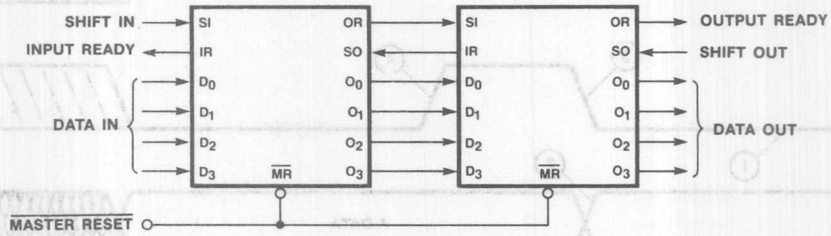


Figure 12. Cascading FIFOs to Form 128x4 FIFO with C5/C67401A/1

FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the FIFOs themselves.

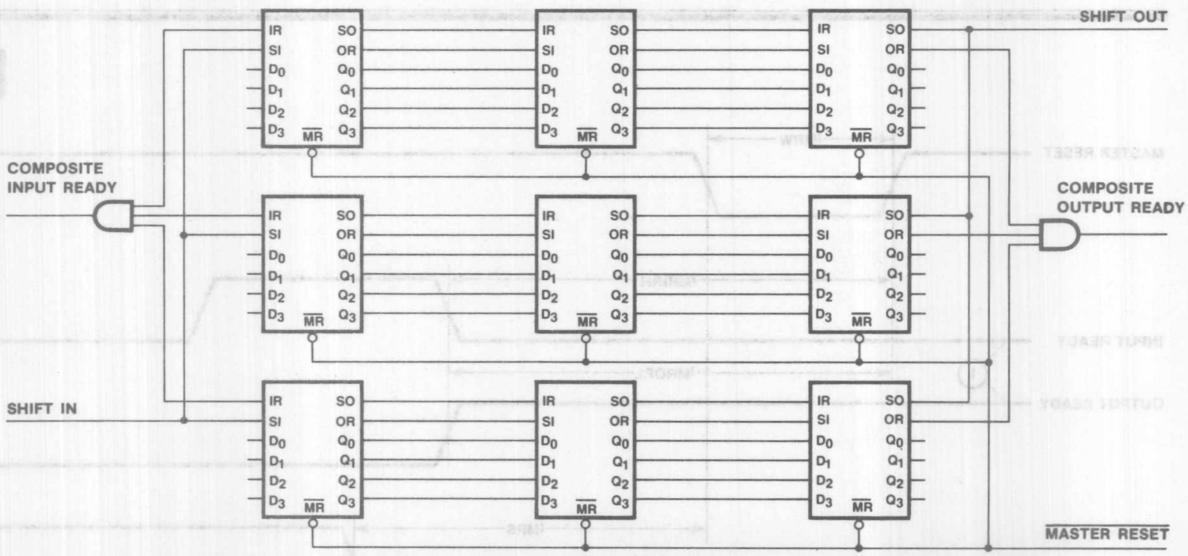


Figure 13. 192x12 FIFO with C5/C67401A/1

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall through times of the FIFOs.

First-In First-Out (FIFO) 64x4 64x5 Serial Stand-Alone Memory
5/67401A 5/67402A 5/67401 5/67402

Features/Benefits

- Choice of 15 and 10 MHz shift out guaranteed rates
- Choice of 4 bit or 5 bit data width
- TTL inputs and outputs
- Readily expandable in the word dimension only
- Output pins directly opposite corresponding input pins
- Asynchronous or synchronous operation
- Pin compatible with Fairchild's F3341 MOS FIFO and many times as fast

Description

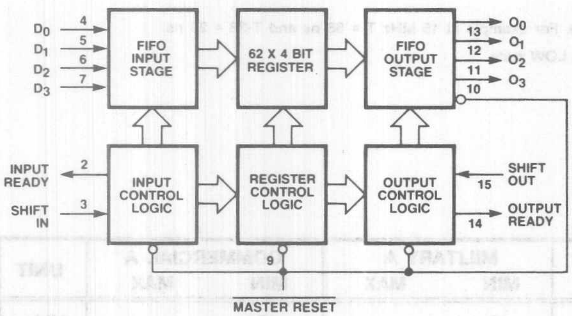
The 67401/2 are expandable "fall-through" high speed First-In First-Out (FIFO) memory organized 64 words by 4-bits and 64 words by 5 bits respectively. A 15 MHz data rate allows usage in high speed tape or disc controllers and communication buffer applications.

Ordering Information

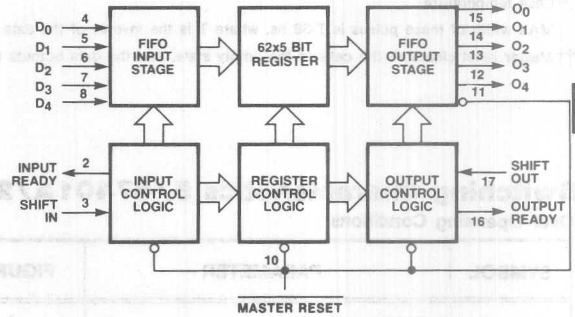
PART NUMBER	PKG	TEMP	DESCRIPTION
57401	J,F	MIL	7 MHz 64x4 FIFO
67401	J	COM	10 MHz 64x4 FIFO
57402	J,F	MIL	7 MHz 64x5 FIFO
67402	J	COM	10 MHz 64x5 FIFO
57401A	J,F	MIL	10 MHz 64x4 FIFO
67401A	J	COM	15 MHz 64x4 FIFO
57402A	J,F	MIL	10 MHz 64x5 FIFO
67402A	J	COM	15 MHz 64x5 FIFO

Block Diagrams

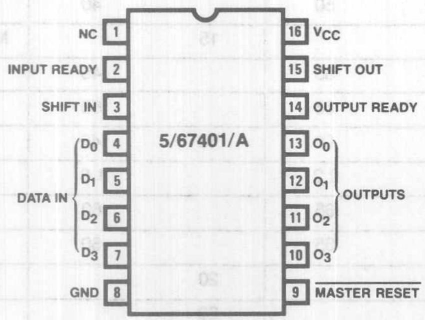
5/67401/A

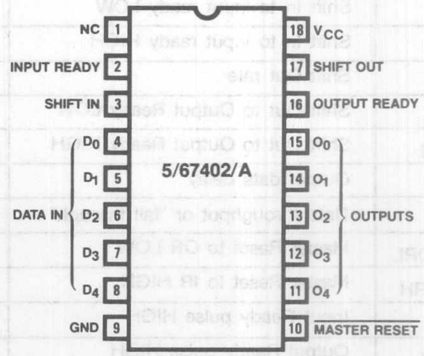


5/67402/A



Pin Configurations





1165 East Arques Avenue, Sunnyvale, CA 94086 Tel: (408) 739-3535 TWX: 910-339-9229

Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{CC} 7V
Input voltage 7V
Off-state output voltage 5.5V
Storage temperature .... −65° to +150°C

Operating Conditions 5/67401A/2A

SYMBOL	PARAMETER	FIGURE	MILITARY A MIN	MILITARY A NOM	MILITARY A MAX	COMMERCIAL A MIN	COMMERCIAL A NOM	COMMERCIAL A MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		*125	0		75	°C
t_{SIH}	Shift in HIGH time	1	35			23		28†	ns
t_{SIL}	Shift in LOW time	1	35			25			ns
t_{IDS}	Input data set up	1	5			5			ns
t_{IDH}	Input data hold time	1	45			40			ns
t_{SOH}	Shift Out HIGH time	6	35			23		28	ns
t_{SOL}	Shift Out LOW time	6	35			25			ns
t_{MRW}	Master Reset pulse††	11	40			35			ns
t_{MRS}	Master Reset to SI	11	45			35			ns

*Case temperature.
†MAX width of these pulses is T-38 ns, where T is the inverse of the data rate. For example at 15 MHz T = 66 ns and T-38 = 28 ns.
††Master reset clears all the cells to the empty state, and the data outputs to a LOW state.

Switching Characteristics 5/67401A/2A
Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY A MIN	MILITARY A MAX	COMMERCIAL A MIN	COMMERCIAL A MAX	UNIT
f_{IN}	Shift in rate	1	10		15		MHz
t_{IRL}	Shift In to input ready LOW	1		50		40	ns
t_{IRH}	Shift In to input ready HIGH	1		50		40	ns
f_{OUT}	Shift Out rate	6	10		15		MHz
t_{ORL}	Shift Out to Output Ready LOW	6		65		45	ns
t_{ORH}	Shift Out to Output Ready HIGH	6		65		50	ns
t_{OD}	Output data delay	6	10	60	10	45	ns
t_{PT}	Data throughput or "fall through"	4, 9		2.2		1.6	μs
t_{MRORL}	Master Reset to OR LOW	11		65		60	ns
t_{MRIRH}	Master Reset to IR HIGH	11		65		60	ns
t_{IPH}	Input Ready pulse HIGH	4	20		20		ns
t_{OPH}	Output Ready pulse HIGH	9	20		20		ns

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature .... −65° to +150°C

Operating Conditions 5/67401/2

SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		*125	0		75	°C
t_{SIH}	Shift in HIGH time		45			35			ns
t_{SIL}	Shift in LOW time	1	45			35			ns
t_{IDS}	Input data set up	1	10			5			ns
t_{IDH}	Input data hold time	1	55			45			ns
t_{SOH}	Shift Out HIGH time	6	45			35			ns
t_{SOL}	Shift Out LOW time	6	45			35			ns
t_{MRW}	Master Reset pulse†	11	30			35			ns
t_{MRS}	Master Reset to SI	11	45			35			ns

*Case temperature.

†Master reset clears all the cells to the empty state, and the data outputs to a LOW state.

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Switching Characteristics 5/67401/2

Over Operating Conditions

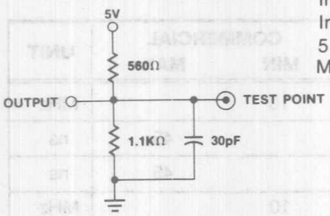
SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	7		10		MHz
t_{IRL}	Shift In to input ready LOW	1		60		45	ns
t_{IRH}	Shift In to input ready HIGH	1		60		45	ns
f_{OUT}	Shift Out rate	6	7		10		MHz
t_{ORL}	Shift Out to Output Ready LOW	6		65		55	ns
t_{ORH}	Shift Out to Output Ready HIGH	6		70		60	ns
t_{OD}	Output data delay	6	10	65	10	55	ns
t_{PT}	Data throughput or "fall through"	4, 9		4		3	μs
t_{MRORL}	Master Reset to OR LOW	11		65		60	ns
t_{MRIRH}	Master Reset to IR HIGH	11		65		60	ns
t_{IPH}	Input Ready pulse HIGH	4	20		20		ns
t_{OPH}	Output Ready pulse HIGH	9	20		20		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL1}	Low-level input current	D_0–D_4, $\overline{MR}$	V_{CC} = MAX	V_I = 0.45V			−0.8	mA
I_{IL2}		SI, SO					−1.6	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4V			50	μA
I_I	Maximum input current		VCC = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OH} = −0.9mA	2.4			V
I_{OS}	Output short-circuit current *		V_{CC} = MAX	V_0 = 0V	−20		−90	mA
I_{CC}	Supply current		V_{CC} = MAX Inputs low, outputs open.	57/67401			160	mA
				5/67402			180	mA
				5/67401A			170	mA
				5/67402A			190	mA

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Standard Test Load



Input Pulse Amplitude = 3 V
Input Rise and Fall Time
5 ns from 1 V to 2 V
Measurements made at 1.5 V

Functional Description

Data Input

After Power Up the Master Reset is pulsed LOW (Fig. 11) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH, the location is ready to accept data from the D_x inputs. Data then present at the four data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal cuases the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

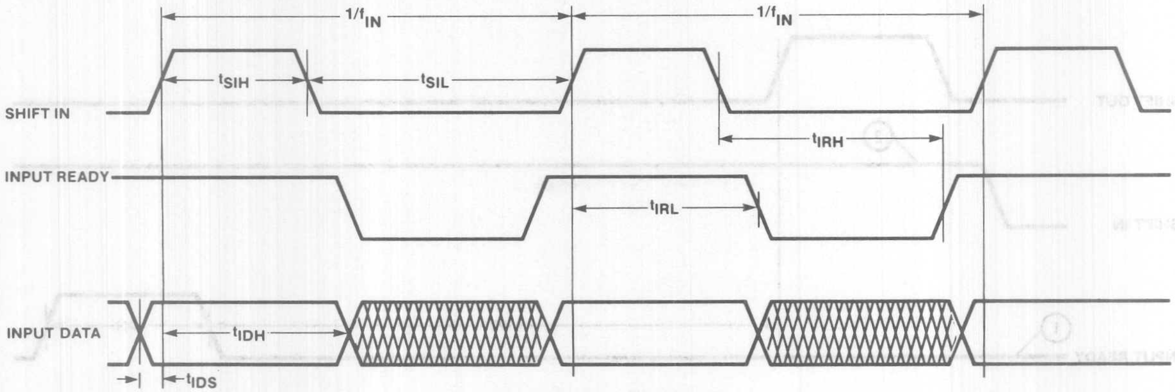


Figure 1. Input Timing

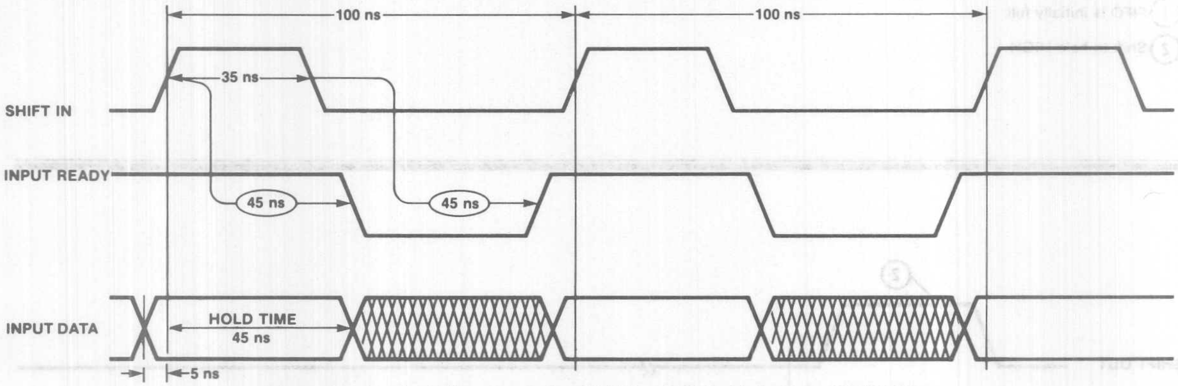


Figure 2. Typical Waveforms for 10 MHz Shift In Data Rate (67401/2)

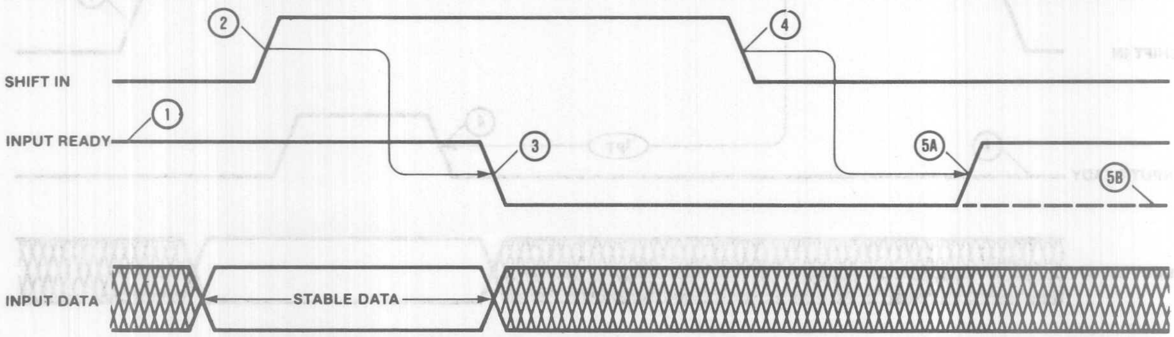


Figure 3. The Mechanism of Shifting Data into the FIFO

1. Input Ready HIGH indicates space is available and a Shift In pulse may be applied.
2. Input Data is loaded into the first word.
3. Input Ready goes LOW indicating the first word is full.
4. The Data from the first word is released for "fall-through" to second word.

5A. The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

5B. If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

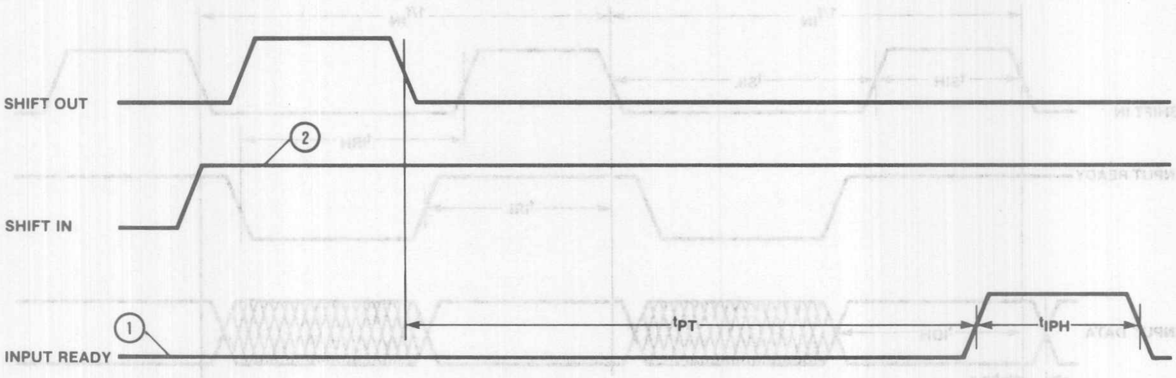


Figure 4. t_{IPH} Specification

1. FIFO is initially full.
2. Shift In held HIGH.

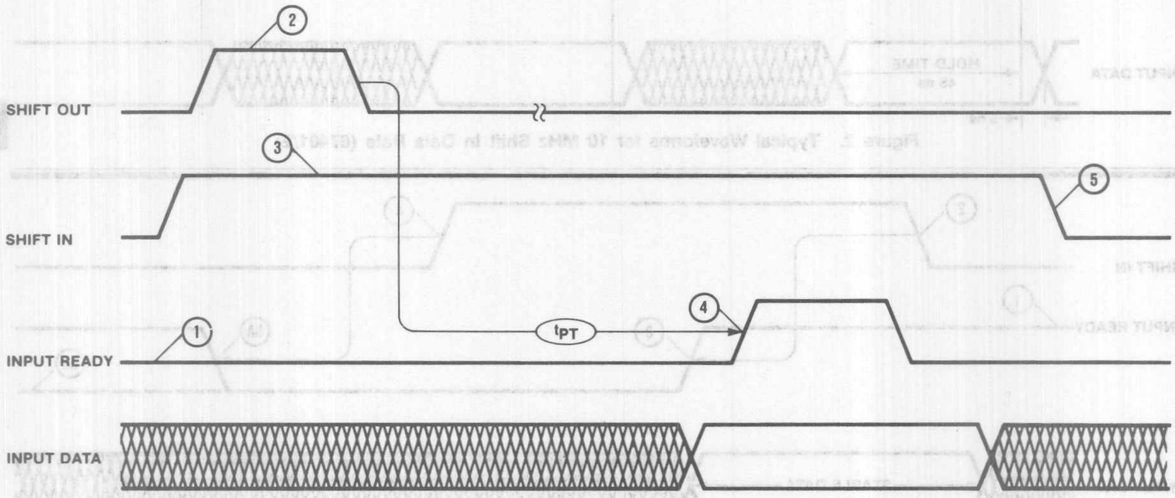


Figure 5. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

1. FIFO is initially full.
2. Shift Out pulse is applied. An empty location start "bubbling" to the front.
3. Shift In is held HIGH.
4. As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.
5. The Data from the first word is released for "fall through" to second word.

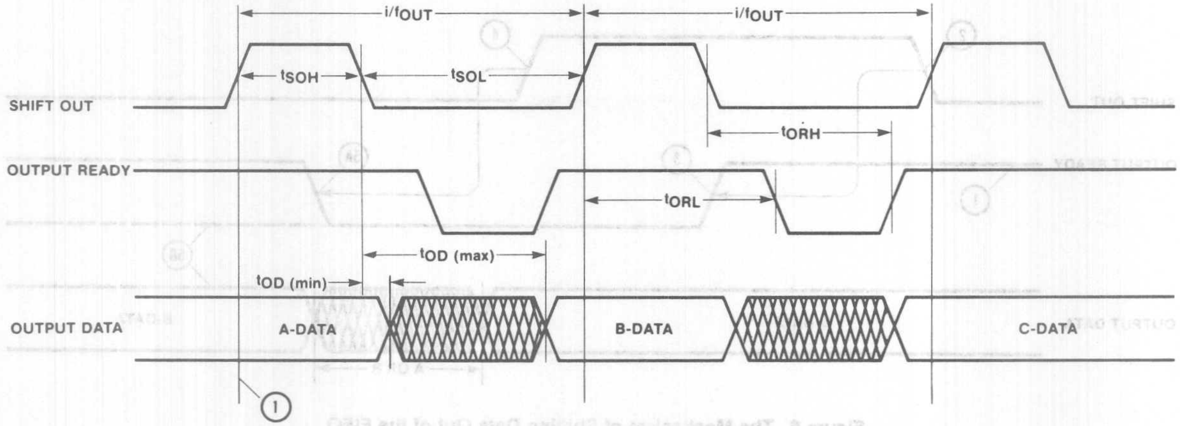


Figure 6. Output Timing

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

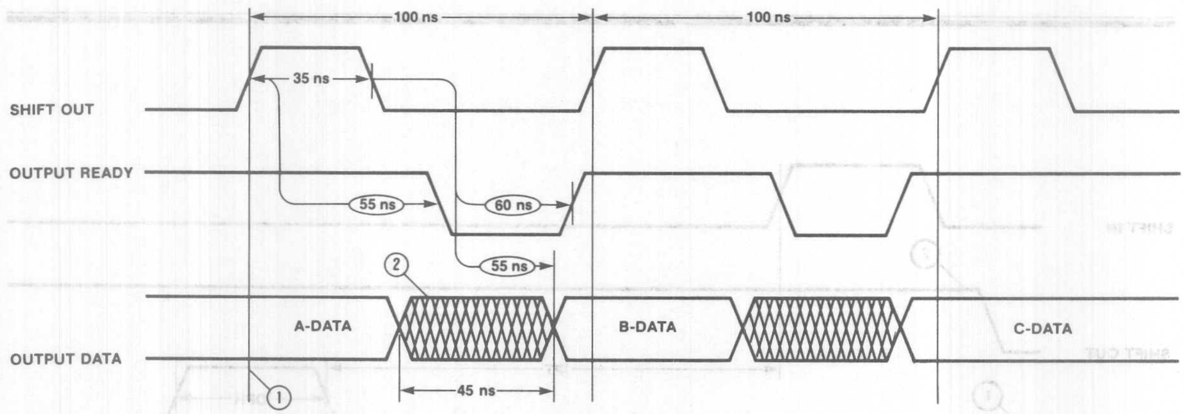


Figure 7. Typical Waveforms for 10 MHz Shift Out Data Rate (67401/2)

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

(2) Data in the crosshatched region may be A or B Data.

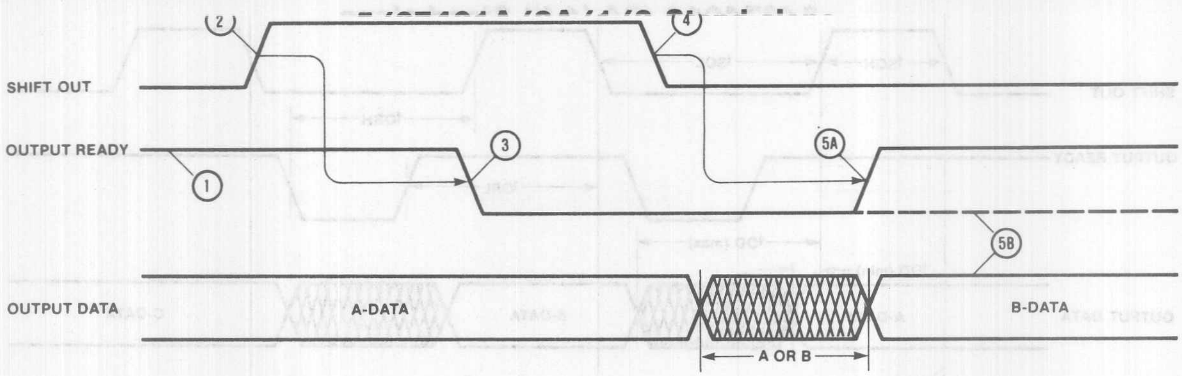


Figure 8. The Mechanism of Shifting Data Out of the FIFO.

(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.

(2) Shift Out goes HIGH causing the next step.

(3) Output Ready goes LOW.

(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.

(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.

(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.

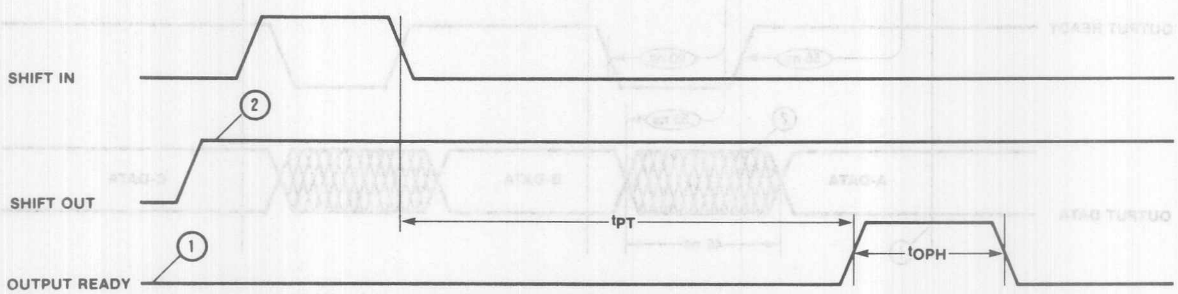


Figure 9. t_{PT} and t_{OPH} Specification

(1) FIFO initially empty.

(2) Shift Out held HIGH.

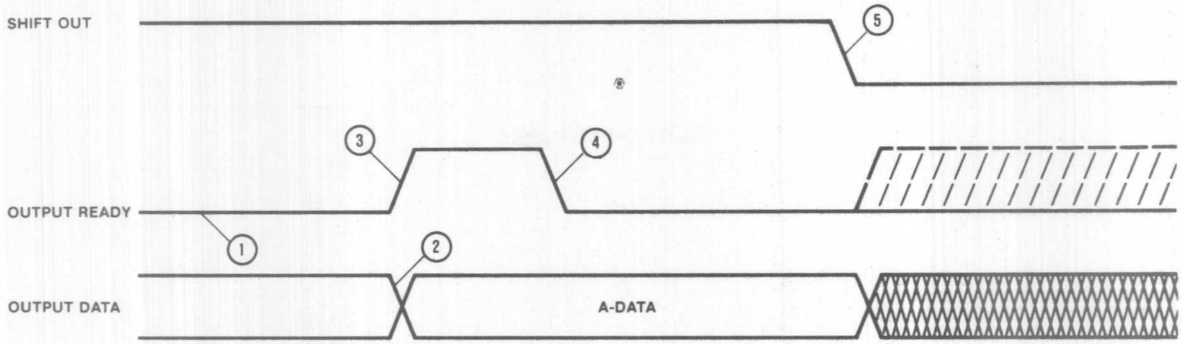


Figure 10. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

1 Word 63 is empty.

2 New data (A) arrives at the outputs (word 63).

3 Output Ready goes HIGH indicating the arrival of the new data.

4 Since Shift Out is held HIGH, Output Ready goes immediately LOW.

5 As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.

9

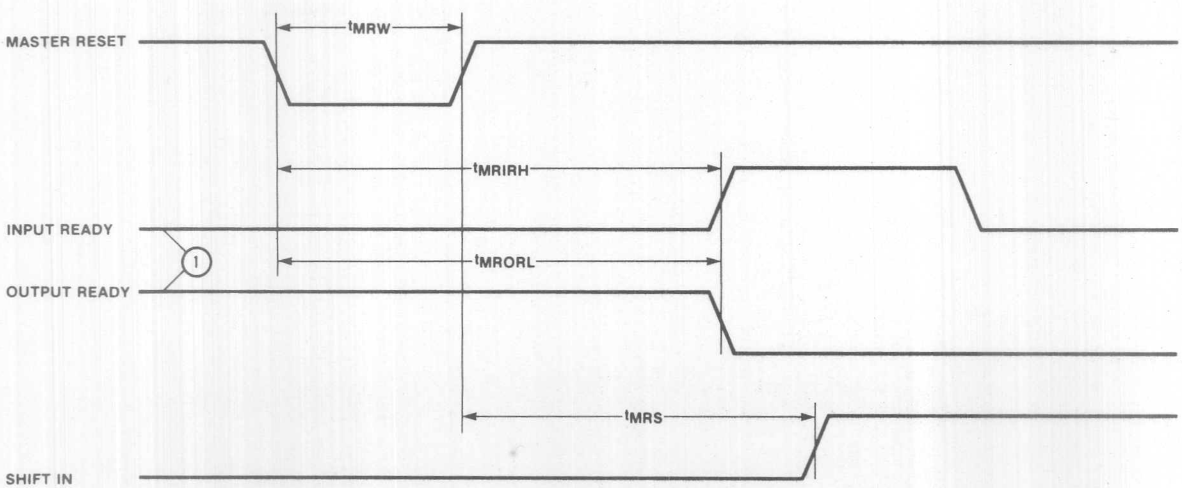


Figure 11. Master Reset Timing

1 FIFO initially full.

The following selection guides are designed to simplify the choice of the particular function to fit the specific application.

Arithmetic and Logic Elements

DESCRIPTION	PART NUMBER	MAX ADD TIME	MAX CARRY (OR GENERATE) TIME	PINS
4-bit ALU	5/74S381	27 ns	20 ns	20
4 Group carry-look-ahead generator	5/74S182		7 ns	16

Look-Up Tables

DESCRIPTION	PART NUMBER	MAX ACCESS TIME	PINS
Sine (0°-90°) Look-Up Table	6086/7	100 ns	24
	5086/7	150 ns	24

Arithmetic Logic Unit/ Function Generator
SN54S381 SN74S381

Features/Benefits

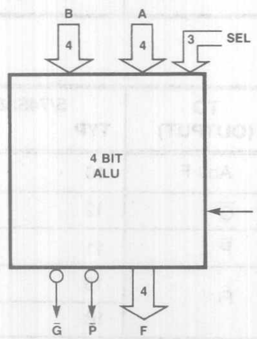
- A Fully Parallel 4-Bit ALU in 20-Pin Package for 0.300-inch Row Spacing
- Ideally Suited for High-Density Economical Processors
- Parallel Inputs and Outputs and Full Look-Ahead Provide System Flexibility
- Arithmetic and Logic Operations Selected Specifically to Simplify System Implementation:

  A Minus B
  B Minus A
  A Plus B
  and Five Other Functions

Description

The 'S381 is a Schottky TTL arithmetic logic unit (ALU)/function generator that performs eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. These operations are selected by the three function-select lines (S0, S1, S2). A fully carry look-ahead circuit is provided for fast, simultaneous carry generation by means of two cascade outputs ($\overline{P}$ and $\overline{G}$) for the four bits in the package.

Logic Symbol

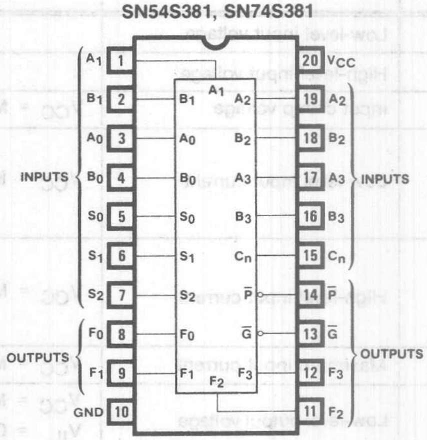


Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54S381	J20,F20	Military
SN74S381	J20	Commercial

Pin Configuration

SN54S381, SN74S381



Function Table

SELECTION			ARITHMETIC/LOGIC OPERATION
S2	S1	S0	
L	L	L	Clear †
L	L	H	B minus A
L	H	L	A minus B
L	H	H	A plus B
H	L	L	$A \oplus B$
H	L	H	A + B
H	H	L	AB
H	H	H	Preset ††

† Force all F outputs to be Lows.
†† Force all F outputs to be Highs.

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Storage Temperature Range .... −65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125	0		70	°C

Electrical Characteristics Over operating conditions

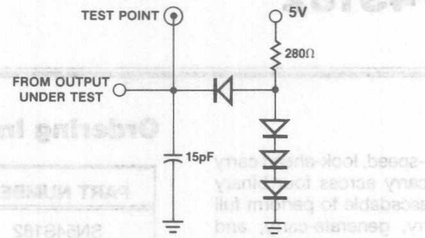
SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA				−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5V	Any S input			−2	mA
				Cn			−8	
				All others			−6	
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V	Any S input			50	μA
				Cn			250	
				All others			200	
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V	V_{IH} = 2V, I_{OL} = 20mA				0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V	V_{IH} = 2V, I_{OH} = −1mA	SN54S381	2.4	3.4		V
				SN74S381	2.7	3.4		
I_{OS}	Output short-circuit current*	V_{CC} = MAX			− 40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX				105	160	mA

* Not more than one output should be shorted at a time.

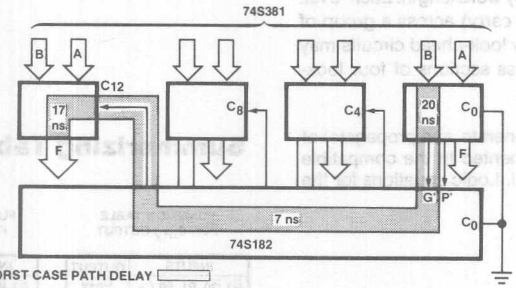
Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	5/74S381 TYP	5/74S381 MAX	UNIT
t_P	Propagation delay time	C_n	Any F	10	17	ns
t_P	Propagation delay time	Any A or B	$\overline{G}$	12	20	ns
t_P	Propagation delay time	Any A or B	$\overline{P}$	11	18	ns
t_{PLH}	Propagation delay, low-to-high	Ai or Bi	Fi	18	27	ns
t_{PHL}	Propagation delay, high-to-low			16	25	ns
t_P	Propagation delay time	Any S	Fi, $\overline{G}$, $\overline{P}$	18	30	ns

Standard Test Load



16-BIT ALU (USING 74S381)



MAXIMUM DELAY OF ADDITION/SUBTRACTION.

	74S381
1-4 bits	27ns
5-16 bits	44ns
17-64 bits	64ns

Look-Ahead Carry Generators

SN54S182 SN74S182

Description

The SN54S182, and SN74S182 are high-speed, look-ahead carry generators capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table below.

When used in conjunction with 74S381, 67S581, 74S181, 2901, 6701 arithmetic logic units (ALU), these generators provide high-speed carry lookahead capability for any word length. Each 'S182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits.

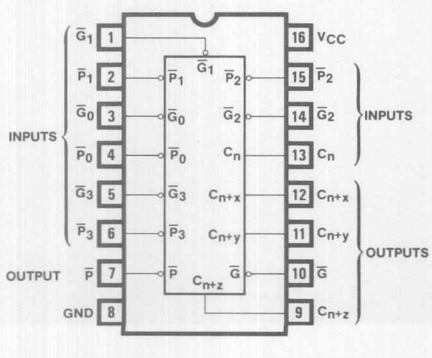
The carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Logic equations for the 'S182 are:

$$C_{n+x} = G0 + P0\ Cn$$
$$C_{n+y} = G1 + P1\ G0 + P1\ P0\ Cn$$
$$C_{n+z} = G2 + P2\ G1 + P2\ P1\ G0 + P2\ P1\ P0\ Cn$$
$$\overline{G} = \overline{G3 + P3\ G2 + P3\ P2\ G1 + P3\ P2\ P1\ G0}$$
$$\overline{P} = \overline{P3\ P2\ P1\ P0}$$

or

$$\overline{C}_{n+x} = \overline{Y0\ (X0 + Cn)}$$
$$\overline{C}_{n+y} = \overline{Y1\ [X1 + Y0\ (X0 + Cn)]}$$
$$\overline{C}_{n+z} = \overline{Y2\ \{X2 + Y1\ [X1 + Y0\ (X0 + Cn)]\}}$$
$$Y = Y3\ (X3 + Y2)\ (X3 + X2 + Y1)\ (X3 + X2 + X1 + Y0)$$
$$X = X3 + X2 + X1 + X0$$

Pin Configuration



Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54S182	J16,F16	Military
SN74S182	J16	Commercial

Summarizing Tables

FUNCTION TABLE FOR C_{n+y} OUTPUT

INPUTS					OUTPUT
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

FUNCTION TABLE FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{P}$
L	L	L	L	L
All other combinations				H

FUNCTION TABLE FOR C_{n+x} OUTPUT

INPUTS			OUTPUT
$\overline{G0}$	$\overline{P0}$	C_n	C_{n+x}
L	X	X	H
X	L	H	H
All other combinations			L

FUNCTION TABLE FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FUNCTION TABLE FOR C_{n+z} OUTPUT

INPUTS							OUTPUT
$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{C}_n$	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

H = High Level, L = Low Level, X = Irrelevant. Any inputs not shown in a given table are irrelevant with respect to that output.

Monolithic Memories

1165 East Arques Avenue, Sunnyvale, CA 94086 Tel: (408) 739-3535 TWX: 910-339-9229

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Storage Temperature Range .... −65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		70	°C

Electrical Characteristics Over operating conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA				−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5V	C_n input			−2	mA
				$\overline{P}_3$ input			−4	
				$\overline{P}_2$ input			−6	
				$\overline{P}_0$, $\overline{P}_1$, or $\overline{G}_3$ input			−8	
				$\overline{G}_0$ or $\overline{G}_2$			−14	
				$\overline{G}_1$ input			−16	
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V	C_n input			50	µA
				$\overline{P}_3$ input			100	
				$\overline{P}_2$ input			150	
				$\overline{P}_0$, $\overline{P}_1$, or $\overline{G}_3$ input			200	
				$\overline{G}_0$ or $\overline{G}_2$			350	
				$\overline{G}_1$ input			400	
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V	V_{IH} = 2V I_{OH} = −1mA				0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V	V_{IH} = 2V I_{OL} = 20mA	SN74S182	2.7	3.4		V
				SN54S182	2.5	3.4		
I_{OS}	Output short-circuit current *	V_{CC} = MAX			−40		−100	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = MAX	See Note 1	SN74S182		69	109	mA
				SN54S182		69	99	
I_{CCH}	Supply current, all outputs high	V_{CC} = 5V	See Note 2			35		mA

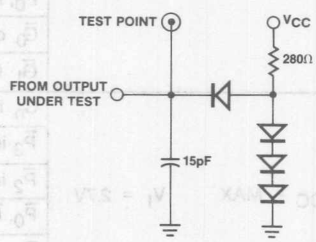
*Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

NOTES: 1. ICCL is measured with all outputs open; inputs $\overline{G}$0, $\overline{G}$1, and $\overline{G}$2 at 4.5 V; and all other inputs grounded.
2. ICCH is measured with all outputs open, inputs $\overline{P}$3 and $\overline{G}$3 at 4.5 V, and all other inputs grounded.

Switching Characteristics $V_{CC} = 5\text{ V}, T_A = 25°C$

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high	$\overline{G}0, \overline{G}1, \overline{G}2, \overline{G}3,$	$C_{n+x}, C_{n+y},$	4.5	7	ns
t_{PHL}	Propagation delay, high-to-low	$\overline{P}0, \overline{P}1, \overline{P}2,$ or $\overline{P}3$	or C_{n+z}	4.5	7	ns
t_{PLH}	Propagation delay, low-to-high	$\overline{G}0, \overline{G}1, \overline{G}2, \overline{G}3,$	$\overline{G}$	5	7.5	ns
t_{PHL}	Propagation delay, high-to-low	$\overline{P}1, \overline{P}2,$ or $\overline{P}3$		7	10.5	ns
t_{PLH}	Propagation delay, low-to-high	$\overline{P}0, \overline{P}1, \overline{P}2,$ or $\overline{P}3$	$\overline{P}$	4.5	6.5	ns
t_{PHL}	Propagation delay, high-to-low			6.5	10	ns
t_{PLH}	Propagation delay, low-to-high	C_n	$C_{n+x}, C_{n+y},$	6.5	10	ns
t_{PHL}	Propagation delay, high-to-low		or C_{n+z}	7	10.5	ns

Standard Test Load



Sine (0° to 90°) Look Up Table Using a 1024 X 10 ROM (5/6255 5/6256) 5/6086 5/6087

Features/Benefits

- Input angle increments of 90°/1024 = .0879°
- 10 bit binary outputs
- Low power dissipation. Typically 500 mw
- Fast access time 100 ns max.
- TTL compatible

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
5086/87	J24	Military
6086/87	J24	Commercial

Description

The 5255/6255, 1024 words by 10 bits Read Only Memory has been customized to make a sine θ look up table (5086/6086) for $0° \leq \theta < 90°$. The address inputs are used to divide the first 90° quadrant into angles increments of 90°/1024 words or .0879°/word. The memory outputs should be interpreted as binary weighted fractions where output 1 has a weight of 1/2 or .500, output 2 has a weight of 1/4 or .250, and so on until output 10 which has a weight of 1/1024 or .000976. The 10 bit output code has not been rounded off so that output error will always be positive and less than 1/1024 or .0009765. Round off error, in approximating the ROM input word, must be added or subtracted to the output error. For electrical characteristics and pin out refer to 6255 specifications (in ROM section).

Example 1:

Find the sine 45°

Let X = the ROM word where sine 45° is stored

$$\frac{X}{1024 \text{ words}} = \frac{45°}{90°}$$

X = word 512

Word 511 has the following stored data and interpretation:

Output #	0_1	0_2	0_3	0_4	0_5	0_6	0_7	0_8	0_9	0_{10}	
Stored Data	H	L	H	H	L	H	L	H	L	L	(H = TTL HIGH)
Binary Weight	$\frac{1}{2}$	$\frac{1}{4}$	$\frac{1}{8}$	$\frac{1}{16}$	$\frac{1}{32}$	$\frac{1}{64}$	$\frac{1}{128}$	$\frac{1}{256}$	$\frac{1}{512}$	$\frac{1}{1024}$	

Adding the fractions wherever an "H" appears given.

$$\frac{1}{2} + \frac{1}{8} + \frac{1}{16} + \frac{1}{64} + \frac{1}{256} = .50000 + .12500 + .06250 + .01562 + .00391 = .70507$$

Handbook Value = .70711

Our Error = .70711 − .70703 = .00008

Example 2:

Find the sine 210°

This value is in quadrant three, therefore, $\theta' = 210° - 180°$ or 30°

Let X = the ROM word where sine 30° is stored $\frac{X}{1024 \text{ words}} = \frac{30°}{90°}$

X = word 341.33 (round off to word 341)

Word 341 has the following stored data and interpretation:

Output #	0_1	0_2	0_3	0_4	0_5	0_6	0_7	0_8	0_9	0_{10}
Stored Data	L	H	H	H	H	H	H	H	H	H
Binary Weight	$\frac{1}{2}$	$\frac{1}{4}$	$\frac{1}{8}$	$\frac{1}{16}$	$\frac{1}{32}$	$\frac{1}{64}$	$\frac{1}{128}$	$\frac{1}{256}$	$\frac{1}{512}$	$\frac{1}{1024}$

Adding the fractions wherever an "H" appears gives 0.49902

The sine 210°, therefore, = −.49902 with the sign generated by external logic. Note that the address 341 to which we rounded off is actually the sine 29.97°.

1165 East Arques Avenue, Sunnyvale, CA 94086 Tel: (408) 739-3535 TWX: 910-339-9229 Monolithic Memories

The following selection guides are designed to simplify the choice of the particular function to fit the specific application.

Co-Processor Multiplier/Divider with Accumulator

DESCRIPTION	PART NUMBER	MAX MULTIPLICATION TIME/ MAX DIVISION TIME	PINS
8 Bits	74S508 54S508	.8 μs/2.2 μs	24

Cray Multipliers

DESCRIPTION	PART NUMBER	MAX DELAY	PINS
8x8 Multiplier	67558-1	125 ns	40
	57558-1	135 ns	40
	67558	150 ns	40
	57558	155 ns	40

8x8 Multiplier/Divider
SN54/74S508

Features/Benefits

- Co-processor for enhancing the arithmetic speed of all present 8-bit microprocessors
- Bus-oriented organization
- 24-pin package
- 8/8 or 16/8 division in less than 2.2 μsec
- 8x8 multiplication in less than .8 μsec
- 28 different multiplication instructions such as "fractional multiply and accumulate"
- 13 different divide instructions
- Self-contained and microprogrammable

Description

The SN54/74S508 ('S508) is a bus-organized 8x8 Multiplier/Divider. The device provides both multiplication and division of 2s-complement 8-bit numbers at high speed. There are 28 different multiply options, including: positive and negative multiply, positive and negative accumulation, multiplication by a constant, and both single-length and double-length addition in conjunction with multiplication. 13 different divide options allow single-length or double-length division, division of a previously-generated result, division by a constant, and continued division of a remainder or quotient.

The 'S508 is a time-sequenced device requiring a single clock. It loads operands from, and presents results to, a bidirectional 8-bit bus. Loading of the operands, reading of the results, and sequential control of the device is performed by a 3-bit instruction field.

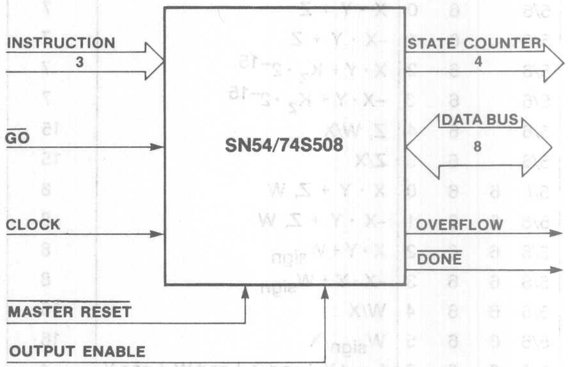
The 'S508 has the additional feature that operands and results can be either integers or fractions; when it deals with fractions, automatic scaling occurs. Results can be rounded if required, and an Overflow output indicates whenever a result is outside the normally-accepted number range.

For a simple multiplication of two operands and reading of the double-length result, the device takes five clock periods — one for initialization, and four for the actual multiplication. A typical clock period is 125 ns, which gives a multiplication time of 500 ns typical for 8x8 multiplication, plus 125 ns additionally for initialization, or 625 ns in all. More complex multiplications will take additional clock periods for loading the additional oper-; ands. A simple division operation requires 8 + 4 = 12 clock periods for a typical time of 1.5 μs (16 bits/8 bits), also plus 125 ns for initialization.

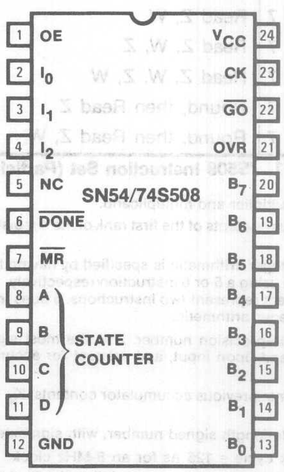
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54S508	TD24	Military
SN74S508	TD24	Commercial

Logic Symbol



Pin Configuration



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				ARITHMETIC OPERATIONS	
			0	$X1 \cdot Y$	5
			1	$-X1 \cdot Y$	5
			2	$X1 \cdot Y + K_Z, K_W$	5
			3	$-X1 \cdot Y + K_Z, K_W$	5
			4	$K_Z, K_W/X1$	13
		5/6	0	$X \cdot Y$	6
		5/6	1	$-X \cdot Y$	6
		5/6	2	$X \cdot Y + K_Z, K_W$	6
		5/6	3	$-X \cdot Y + K_Z, K_W$	6
		5/6	4	K_W/X	14
		5/6	5	K_Z/X	14
5/6		6	0	$X \cdot Y + Z$	7
5/6		6	1	$-X \cdot Y + Z$	7
5/6		6	2	$X \cdot Y + K_Z \cdot 2^{-15}$	7
5/6		6	3	$-X \cdot Y + K_Z \cdot 2^{-15}$	7
5/6		6	4	Z, W/X	15
5/6		6	5	Z/X	15
5/6	6	6	0	$X \cdot Y + Z, W$	8
5/6	6	6	1	$-X \cdot Y + Z, W$	8
5/6	6	6	2	$X \cdot Y + W_{sign}$	8
5/6	6	6	3	$-X \cdot Y + W_{sign}$	8
5/6	6	6	4	W/X	16
5/6	6	6	5	W_{sign}/X	16
5/6	6	6	6	Load X, Load Z, Load W, Load Y	4
5/6	6	6	7	Load X, Load Z, Load W, Read Z	3
				READING OPERATIONS	
			7	Read Z	1
		7	7	Read Z, W	2
	7	7	7	Read Z, W, Z	1
7	7	7	7	Read Z, W, Z, W	4
		5	7	Round, then Read Z	2
	5	7	7	Round, then Read Z, W	3

Figure 1 'S508 Instruction Set (Partial List)

NOTES:
1. X,Y are input multiplier and multiplicand.
2. X1 is the previous contents of the first rank of the X register, (either the old X or a new X).
3. Fractional or integer arithmetic is specified by having the next-to-the-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with "5/6" in effect represent *two* instructions. 5 does fractional arithmetic and 6 does integer arithmetic.
4. Z, W is a double-precision number. Z is the most significant half. Z, W represents addend upon input, and product (or accumulated sum) after multiplication.
5. K_Z, K_W represents previous accumulator contents. K_Z is the most-significant half.
6. W_{sign} is a single-length signed number, with sign extension.
7. Maximum clock cycle = 125 ns for an 8-MHz clock.
8. If n instruction codes are shown at the left under "instruction sequences," the number of clock cycles at the right is n+4 for multiplication and n+12 for division.
9. By presenting code 7 on the instruction lines at least one clock cycle before the last clock pulse of the operation cycles, the result (register Z) is available on the bus one clock earlier (see Figure 9).

I_0-I_2	Instruction (sequential control) input
A, B, C, D	Instruction (sequential control) inputs
CK	Clock pulse input
$\overline{GO}$	Chip activation input
OE	Output enable input
$\overline{MR}$	Master reset input
OVR	Arithmetic overflow output
$\overline{DONE}$	Arithmetic-operation completion output

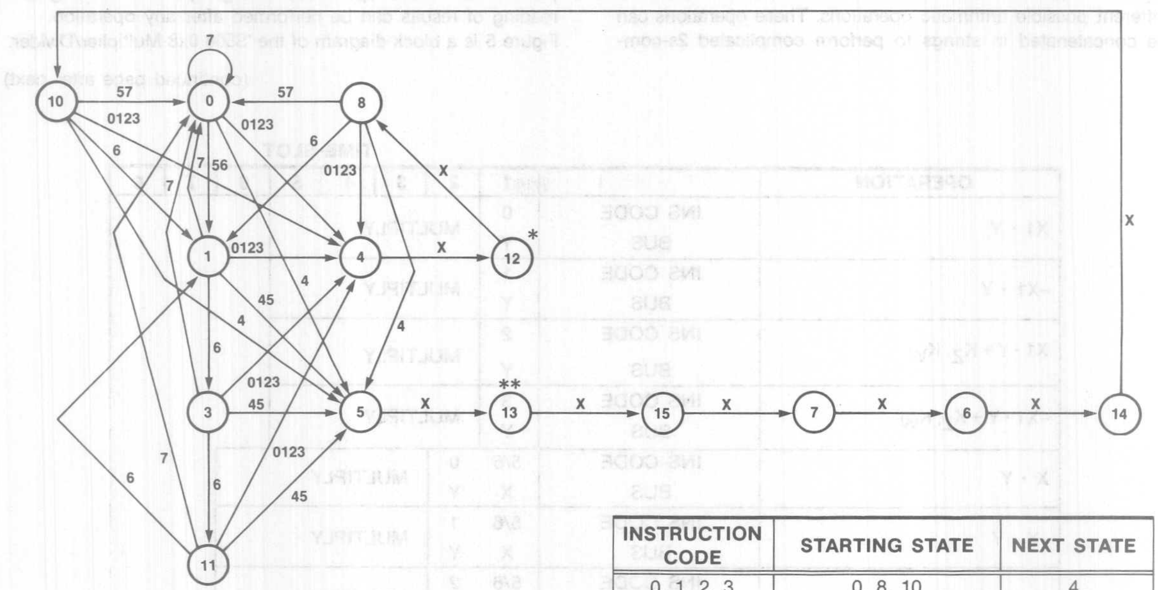
Description (continued)

The 'S508 device uses standard low-power Schottky technology, requires a single +5V power supply, and is fully TTL compatible. Bus inputs require at most 250 μA input current, and control and clock inputs require at most 1 mA input current. Bus outputs are three-state, and are capable of sinking 8 mA at the low logic level. The 'S508 is available in both commercial-temperature and military-temperature ranges, in a 24-pin dual-in-line ceramic package.

Device Operation

The 'S508 contains four 8-bit working registers. Y is the multiplier register; X is the multiplicand and divisor register; W is the least-significant half of a double-length accumulator, and holds the least-significant half of the product after a multiplication operation, or the remainder after a division operation; and Z is the most-significant half of this same accumulator. In addition to these registers, there is a high-speed arithmetic unit which performs addition, subtraction, and shifting steps in order to accomplish the various arithmetic operations; a loading sequencer; and a PLA control network.

Operands are loaded into the working registers in time sequence at each clock period, under the control of this sequencer. The chip-activation signal $\overline{GO}$ must be LOW in order to begin the loading process and continue to the next step in the loading operation. If $\overline{GO}$ is continually held HIGH, the 'S508 remains in a wait state with its outputs held in their high-impedance states, so that the other devices attached to the bus may drive it. In this condition, the 'S508 does not respond to any codes on its instruction inputs; in effect, it does not "wake up" until $\overline{GO}$ goes LOW. Also, $\overline{GO}$ may change only when the clock input CK is HIGH. After all of the operands are loaded, the 'S508 jumps to the multiply routine, or to the divide routine, and performs the required operations as indicated in Figure 1. After 5 clock periods for a simple multiply or 13 clock periods for a simple divide, for example, the device is ready to place the result on the bus in time sequence.



∗Loop 3 times for multiplication.
∗∗Loop 6 times for fractional division, or 7 times for integer division.

INSTRUCTION CODE	STARTING STATE	NEXT STATE
0, 1, 2, 3	0, 8, 10	4
4	0, 8, 10	5
5	0	1
5, 7	8, 10	0
6	0, 8, 10	1
7	0, 8, 10	0

Figure 2 Transition Diagram for the 'S508 Multiplier/Divider

KEY:

The numbers inside the circles indicate the *state* of the 'S508 multiplier/divider. These states are represented by a four-bit state counter, where A is the least-significant bit of this state counter and D is the most-significant bit. These four bits are available externally on the 'S508.

The next state of the 'S508 is a function of the present state and the instruction lines. For example if the 'S508 is at state 0 and the instruction is 0, 1, 2, or 3, then the next state is state 4 (multiply instruction); if the instruction is 4, the next state is state 5 (divide instruction); and so forth. The instructions which take the 'S508 from one state to another are indicated by the numbers written next to the state-transition path lines. "0123," for instance, implies that *any* of instructions 0, 1, 2, or 3 will take the 'S508 along the path marked "0123."

"X" next to a path implies that the path will be followed regardless of the value of the instruction inputs at that time. In other words, for the purpose of state transitions, X means "don't care." There are cases, however, where the particular instruction used may affect when the contents of the registers are available on the bus — see Figures 9 and 10 for contrasting examples of how this effect operates.

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Three instruction inputs I_0, I_1, I_2, which may change only when the clock input CK is HIGH, select the required function and drive the sequencer from state to state. Thus, the action of the multiplier/divider at any clock period is a function of the machine state and the state of the control inputs. Figure 2 shows the multiply/divide state table, and all possible operations. After a Read or Round operation, the machine is driven back to state 0, and a new sequence of arithmetic operations is assumed. If a chain operation is being performed, such as accumulation of products, state 0 is bypassed, and loading of an operand or jumping to the next arithmetic operation occurs at the end of the previous arithmetic operation — at state 8 for a multiplication instruction, or at state 10 for a division instruction.

Register X is a dual-rank register, which allows the loading of an operand X during the multiplication or division process. If the machine enters the loading sequence and a new X operand has not been loaded, then the machine proceeds with the previously-loaded X, denoted in this text as "X1." This loading-while-processing capability allows a cycle to be saved during "chained" calculations, and also allows multiplication and division by a constant. (See Figure 13).

(continued next page)

Figures 3 and 4 show the codes and durations for the 41 different possible arithmetic operations. These operations can be concatenated in strings to perform complicated 2s-complement arithmetic operations at high-speed. Rounding and reading of results can be performed after any operation. Figure 5 is a block diagram of the 'S508 8x8 Multiplier/Divider.

(continued page after next)

		TIME-SLOT							
OPERATION		1	2	3	4	5	6	7	8
$X1 \cdot Y$	INS CODE	0	MULTIPLY						
	BUS	Y							
$-X1 \cdot Y$	INS CODE	1	MULTIPLY						
	BUS	Y							
$X1 \cdot Y + K_Z, K_W$	INS CODE	2	MULTIPLY						
	BUS	Y							
$-X1 \cdot Y + K_Z, K_W$	INS CODE	3	MULTIPLY						
	BUS	Y							
$X \cdot Y$	INS CODE	5/6	0	MULTIPLY					
	BUS	X	Y						
$-X \cdot Y$	INS CODE	5/6	1	MULTIPLY					
	BUS	X	Y						
$X \cdot Y + K_Z, K_W$	INS CODE	5/6	2	MULTIPLY					
	BUS	X	Y						
$-X \cdot Y + K_Z, K_W$	INS CODE	5/6	3	MULTIPLY					
	BUS	X	Y						
$X \cdot Y + Z$	INS CODE	5/6	6	0	MULTIPLY				
	BUS	X	Z	Y					
$-X \cdot Y + Z$	INS CODE	5/6	6	1	MULTIPLY				
	BUS	X	Z	Y					
$X \cdot Y + K_Z \cdot 2^{-7}$	INS CODE	5/6	6	2	MULTIPLY				
	BUS	X	—	Y					
$-X \cdot Y + K_Z \cdot 2^{-7}$	INS CODE	5/6	6	3	MULTIPLY				
	BUS	X	—	Y					
$X \cdot Y + Z, W$	INS CODE	5/6	6	6	0	MULTIPLY			
	BUS	X	Z	W	Y				
$-X \cdot Y + Z, W$	INS CODE	5/6	6	6	1	MULTIPLY			
	BUS	X	Z	W	Y				
$X \cdot Y + W_{sign}$	INS CODE	5/6	6	6	2	MULTIPLY			
	BUS	X	—	W	Y				
$-X \cdot Y + W_{sign}$	INS CODE	5/6	6	6	3	MULTIPLY			
	BUS	X	—	W	Y				

Figure 3 Multiplication Codes and Times for 8x8 Multiplication in the 'S508

NOTES: 1) X1 is the previous contents of the first rank of the X register (either old X or a new X).
2) $K_Z \cdot 2^{-7}$ is a single-length signed number comprising the most-significant half of the previous double-length product and here gets added in at the least-significant end of the new result.
3) W_{sign} is a single-length signed number, with sign-extension as needed.
4) Fractional or integer arithmetic is specified by having the next-to-the-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with "5/6" in effect represent *two* instructions. 5 does fractional arithmetic and 6 does integer arithmetic.

OPERATION		TIME-SLOT 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
K_Z, K_W/X_1	INS CODE	4	DIVIDE											1			
	BUS	—															
K_W/X	INS CODE	5/6	4	DIVIDE											1		
	BUS	X	—														
K_Z/X	INS CODE	5/6	5	DIVIDE											1		
	BUS	X	—														
Z, W/X	INS CODE	5/6	6	4	DIVIDE											1	
	BUS	X	Z	W													
Z/X	INS CODE	5/6	6	5	DIVIDE											1	
	BUS	X	Z	—													
W/X	INS CODE	5/6	6	6	4	DIVIDE											1
	BUS	X	—	W	—												
W_{sign}/X	INS CODE	5/6	6	6	5	DIVIDE											1
	BUS	X	O	W	—												

Figure 4 Division Codes and Time for 16/8 Division in 'S508

NOTES: 1) X1 is the previous contents of the first rank of the X register (either old X or a new X).
2) Fractional division divides a 31-bit 2s-complement number in 1 clock period less than integer division.
3) W_{sign} is a single-length signed number, with sign-extension as needed.
4) Division operation W_{sign}/X requires that the Z register be initialized with all-zero contents at the time Z is loaded.
5) Fractional or integer arithmetic is specified by having the next-to-the-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with "5/6" in effect represent *two* instructions, one of which does fractional arithmetic and one of which does integer arithmetic.

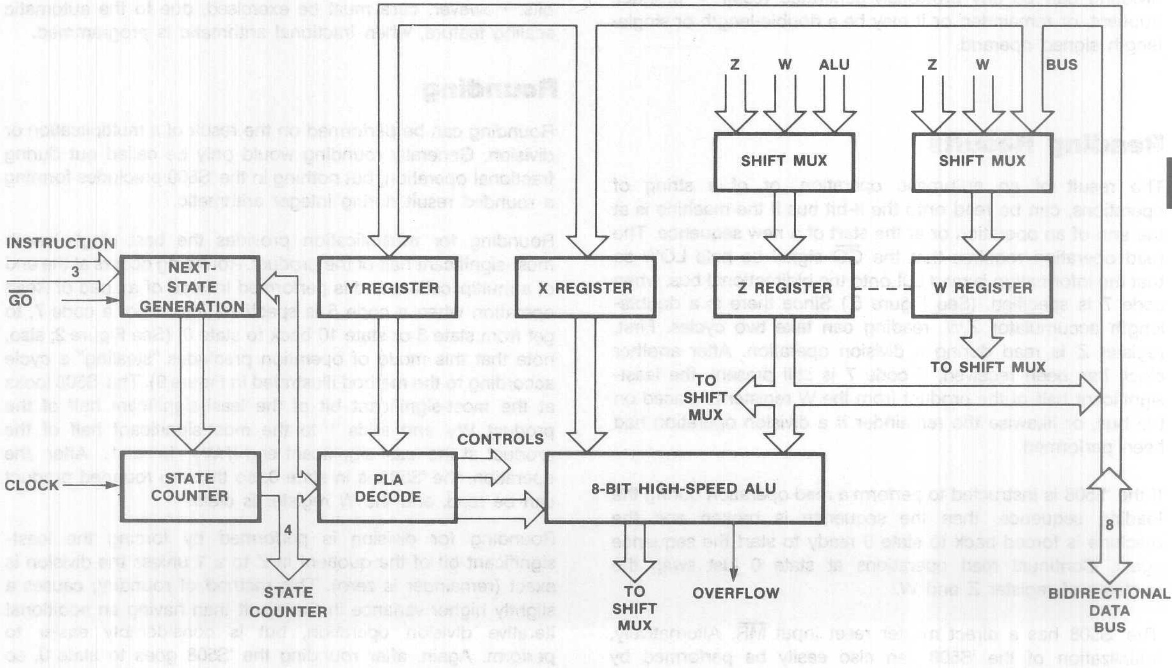

Figure 5 Internal Architecture of the 'S508

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Multiplication

The 'S508 provides 2s-complement 8-bit multiplication, and can also accumulate previously-generated double-length products. No time penalty is incurred for accumulation, since the machine accumulates while the multiplication operation is proceeding. In addition to accumulation, the device can add into a product either a single-length or a double-length number. It can also use a previously-loaded operand as a constant, so that constant multiplication and accumulation is possible.

One key feature is the ability to perform both positive multiplications and negative multiplications, again without any speed penalty. This feature allows complex-arithmetic multiplications to be programmed with very little overhead. Another important feature is the ability to work with either fractions or integers.

Division

The 'S508 also provides a range of division operations. A double-length number in Z,W is divided by X; the result Q is stored in Z, and the remainder R in W. Again all numbers are in the 2s-complement number representation, with the most significant bit of an operand (whether single-length or double-length) having a negative weight. In order to facilitate repeated division, with the multiple-length quotient always keeping the same sign, the remainder is always the same sign as the dividend. Fractional or integer operation is possible, and division and multiplication operations can be concatenated. For example, the operations (AxB)/C,(A+B)/C can easily be performed. The dividend can be any previously-generated result — product, quotient, or remainder; or it may be a double-length or single-length signed operand.

Reading Results

The result of an arithmetic operation, or of a string of operations, can be read onto the 8-bit bus if the machine is at the end of an operation or at the start of a new sequence. The read operation requires that the $\overline{GO}$ signal be held LOW so that the information is read out onto the bidirectional bus, when code 7 is specified. (See Figure 6.) Since there is a double-length accumulator Z,W, reading can take two cycles. First, register Z is read during a division operation. After another clock has been received, if code 7 is still present, the least-significant half of the product from the W register is placed on the bus, or likewise the remainder if a division operation had been performed.

If the 'S508 is instructed to perform a read operation during the loading sequence, then the sequence is broken and the machine is forced back to state 0 ready to start the sequence again. Continual read operations at state 0 just swap the contents of register Z and W.

The 'S508 has a direct master reset input $\overline{MR}$. Alternatively, initialization of the 'S508 can also easily be performed by continually presenting instruction code 7, which after a maximum of 13 clock periods forces the machine back to state 0.

Integer and Fractional Arithmetic

The 'S508 can work with either fractional or integer number representations. When working with integers, all numbers are scaled from the least-significant end and the least-significant bit is assumed to have a weight of 2^0. For integer multiplication, accumulation, and division, all numbers are scaled from this least-significant weight, and results are correct if interpreted in this manner. The double-length register Z,W can therefore hold numbers in the range -2^{15} to $+2^{15}-1$; the operands X and Y, and single-length results, are in the range -2^7 to $+2^7-1$.

When working with fractions, the machine automatically performs scaling so that input operands and results have a consistent format. All numbers in the fractional representation are scaled from the most significant end, which has a weight of -2^0 *(negative)*. The binary point is one place to the right of this most-significant bit, so that the next bit has a weight of 2^{-1}. The double-length register Z,W therefore holds numbers in the range -1 to $+1-2^{-15}$ and the operands X and Y and single-length results are in the range -1 to $+1-2^7$. Since automatic scaling occurs, the product of two numbers always has the least-significant bit as a 0, unless an accumulation is performed with the least-significant bit being a 1.

During a chain operation with the partial results not being read onto the bus, the 'S508 will stay in either the fractional or integer mode. At the start of a sequence of operations, fractional or integer operation is designated by loading operands using instruction code 5 or instruction code 6 respectively.

Mixed fractional and integer arithmetic is also possible, by redefining the weight of the least-significant or most-significant bits. However, care must be exercised, due to the automatic scaling feature, when fractional arithmetic is programmed.

Rounding

Rounding can be performed on the result of a multiplication or division. Generally rounding would only be called out during fractional operation, but nothing in the 'S508 precludes forming a rounded result during integer arithmetic.

Rounding for multiplication provides the best single-length most-significant half of the product. Rounding occurs at the end of a multiplication, and is performed instead of a Load or Read operation when a code 5 is specified, instead of a code 7, to get from state 8 or state 10 back to state 0. (See Figure 2; also, note that this mode of operation precludes "stealing" a cycle according to the method illustrated in Figure 9). The 'S508 looks at the most-significant bit of the least-significant half of the product W_7 and adds 1 to the most-significant half of the product at the least-significant end if W_7 is a 1. After the operation, the 'S508 is in state 0, so that the rounded product can be read, and the W register is clear.

Rounding for division is performed by forcing the least-significant bit of the quotient in Z to a 1 unless the division is exact (remainder is zero). This method of rounding causes a slightly higher variance in the result than having an additional iterative division operation, but is considerably easier to perform. Again, after rounding the 'S508 goes to state 0, so that a read operation can be performed, and the W register is clear.

Overflow

The 'S508 has an overflow output OVR which is cleared prior to each operation, and is set during an operation if the product or quotient goes outside the normally-accepted range.

For multiplication, overflow can only occur if the most negative number in the operand range is used: (–1)x(–1)=+1, which cannot be held in the 'S508's internal registers. Overflow can more easily occur during either positive or negative accumulation of products. For fractional arithmetic, if the product or accumulation goes outside the range of -1 to $+1-2^{-15}$, then the overflow flipflop will be set.

Overflow may also occur during division if the quotient goes outside the generally-accepted number range of -1 to $+1-2^{-7}$ during fractional operation. This would occur if the divisor is less than the dividend, or equal to the dividend if a positive quotient is being generated. For integer arithmetic the numbers must be scaled by 2^7.

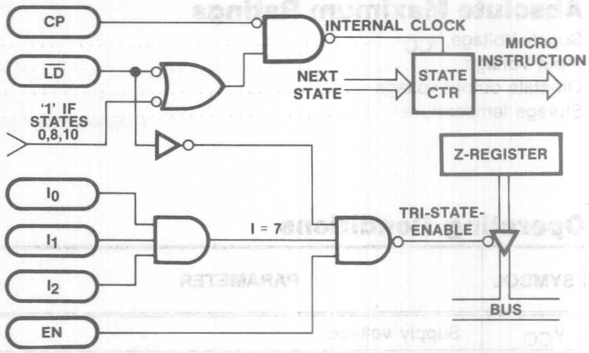


Figure 6 'S508 Internal Circuitry of "$\overline{GO}$" Line and Three-State-Enable.

During the beginning and ending states (0, 8, and 10) if the "GO" line ($\overline{GO}$) is logic HIGH then the machine will be in a wait state until $\overline{GO}$ goes to logic LOW.

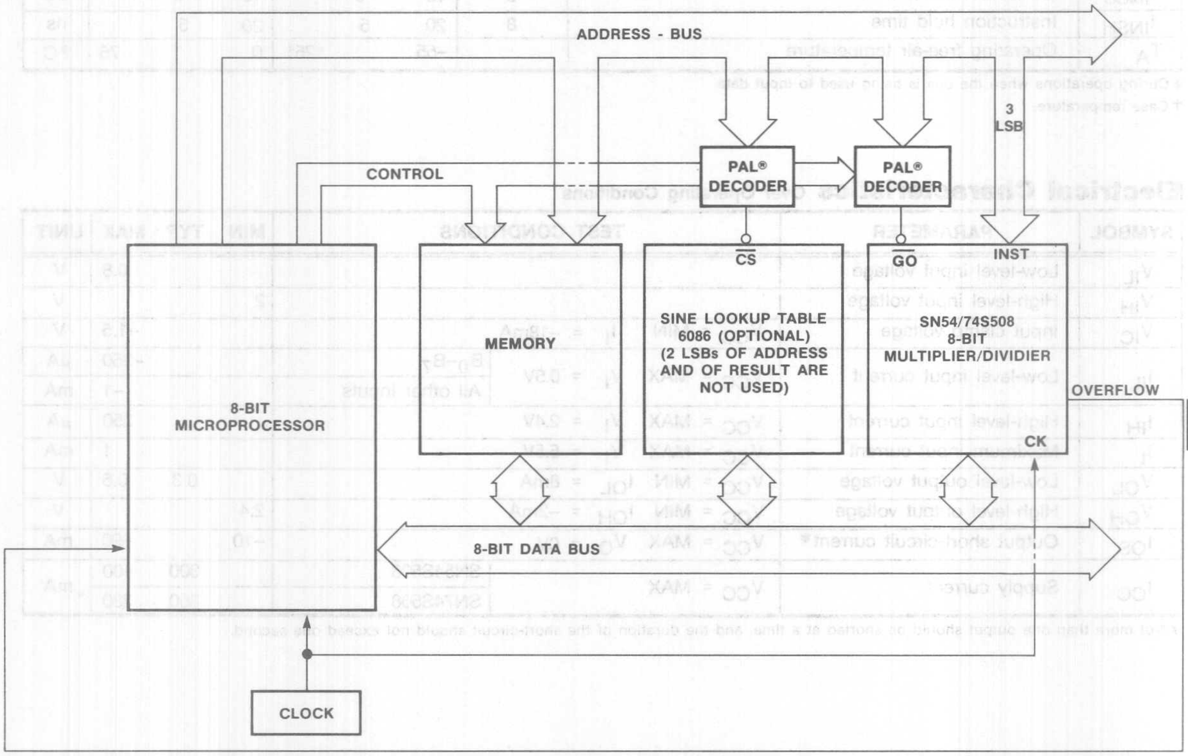


Figure 7 Interfacing the 'S508 to an 8-bit Microprocessor

Figure 7 shows the block diagram of a minimum 8-bit microprocessor system with its arithmetic capabilities enhanced by the use of a 'S508 8x8 multiplier/divider. The relatively small number of instruction lines (only 3) of the 'S508 provides a unique way to control the multiplier/divider. As may be seen from Figure 7, these three instruction lines are assigned to the three least-significant bits (LSBs) of the address bus, while the remaining address bits are decoded by a Programmable Array Logic (PAL®) circuit to determine when the multiplier/divider is selected. For example, suppose the 'S508 is assigned address 100; then any address in the range of 100-107 will enable the 'S508 (i.e., the $\overline{GO}$ line is LOW). Thus, if the address is 100 the 'S508 instruction is 0; if the address is 106 the 'S508 instruction is 6; and so forth.

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
f_{MAX}	Clock frequency	8	5	8		6	8		MHz
t_{CWP}	Positive clock pulse width	8	90	45		70	45		ns
t_{CWN}	Negative clock pulse width	8	60	35		50	35		ns
t_{BS}	Bus set-up time for inputting data *	8	60	30		50	30		ns
t_{BH}	Bus hold time for inputting data *	8	45	30		35	25		ns
t_{INSS}	Instruction setup time	8	10	−5		10	−5		ns
t_{INSH}	Instruction hold time	8	20	5		20	5		ns
T_A	Operating free-air temperature		−55		125†	0		75	°C

* During operations when the bus is being used to input data.
† Case temperature.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5V	B_0–B_7			−250	μA
				All other inputs			−1	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V				250	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8mA			0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −2mA		2.4			V
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0V		−10		−90	mA
I_{CC}	Supply current	V_{CC} = MAX		SN54S508		300	400	mA
				SN74S508		300	380	

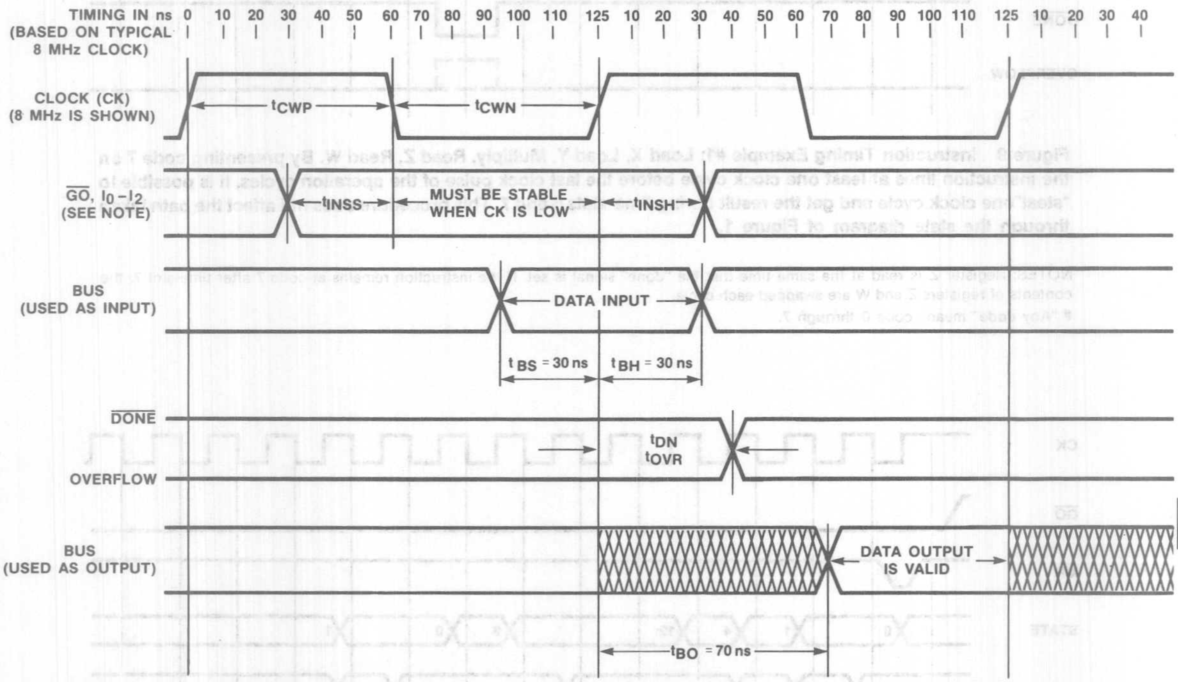
* Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

Switching Characteristics

Over Operating Conditions

SYMBOL	PARAMETER		FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{BO}	Bus output delay for outputting data*		8		70	120		70	95	ns
t_{PXZ}	Output disable delay	From I_0–I_2 to bus			40	70		40	65	ns
		From EN, $\overline{GO}$ to bus			20	50		20	40	
t_{PZX}	Output enable delay	From I_0–I_2 to bus			45	90		45	80	ns
		From EN, $\overline{GO}$ to bus			25	55		25	45	
t_{OVR}	Overflow output delay		8		70	120		70	95	ns
t_{DN}	$\overline{\text{Done}}$ output delay		8		30	90		30	70	ns

*During operations when the bus is being used to output data.



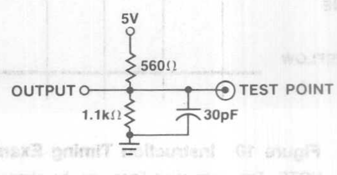
NOTE: $\overline{GO}$ and I_0–I_2 can change only when CK is high.

Figure 8 Timing diagram of the 'S508

Timing

Timing waveforms are shown in Figure 8. Specific instruction timing examples are shown in Figures 9 through 13.

Standard Test Load



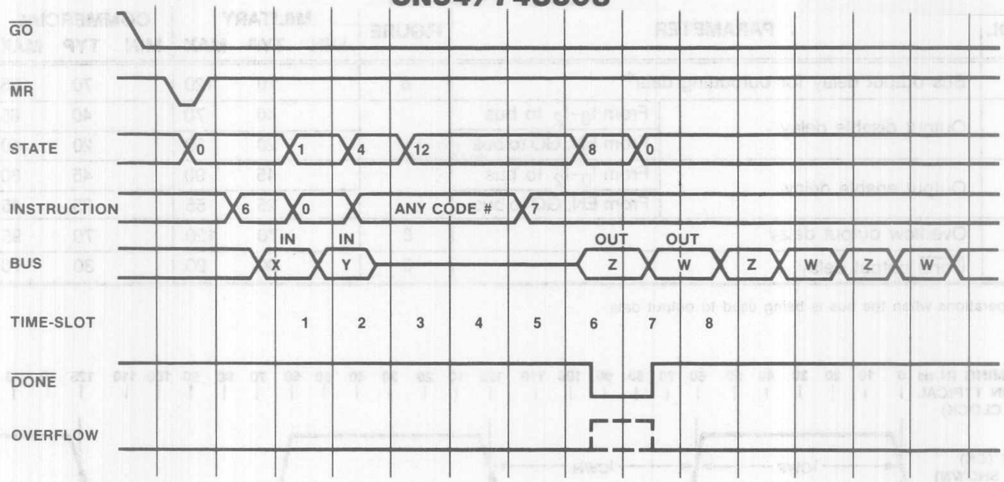


Figure 9 Instruction Timing Example #1: Load X, Load Y, Multiply, Read Z, Read W. By presenting code 7 on the instruction lines at least one clock cycle before the last clock pulse of the operation cycles, it is possible to "steal"one clock cycle and get the result during time-slots 6 and 7. This procedure does not affect the path taken through the state diagram of Figure 1.

NOTES: Register Z is read at the same time that the "done" signal is set. If the instruction remains at code 7 after time-slot 7, the contents of registers Z and W are swapped each cycle.
"Any code" means code 0 through 7.

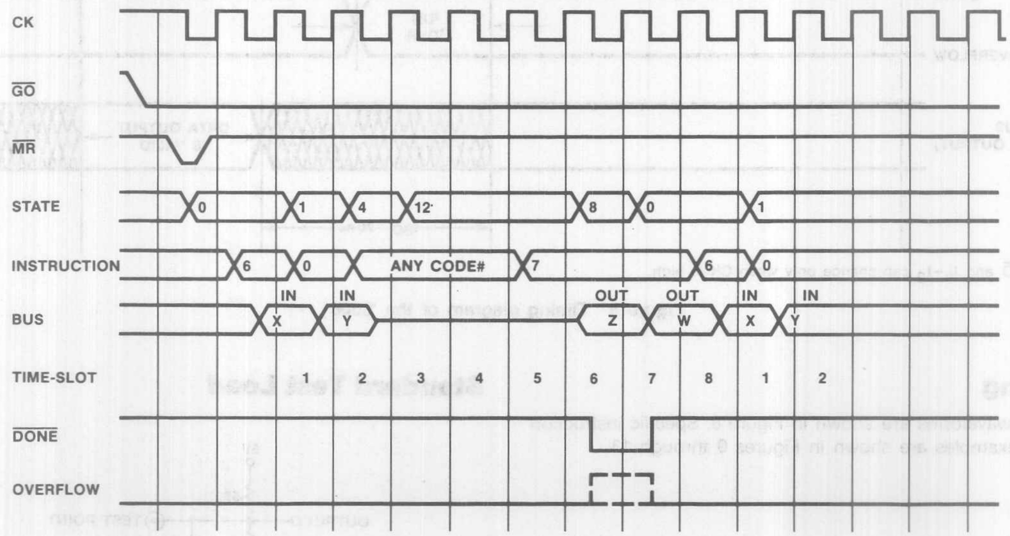


Figure 10 Instruction Timing Example #2: Repeat: "Load X, Load Y, Multiply, Read Z, Read W".
NOTE: The instruction lines may be changed only when CK is high.
#"Any code" means code 0 through code 7.

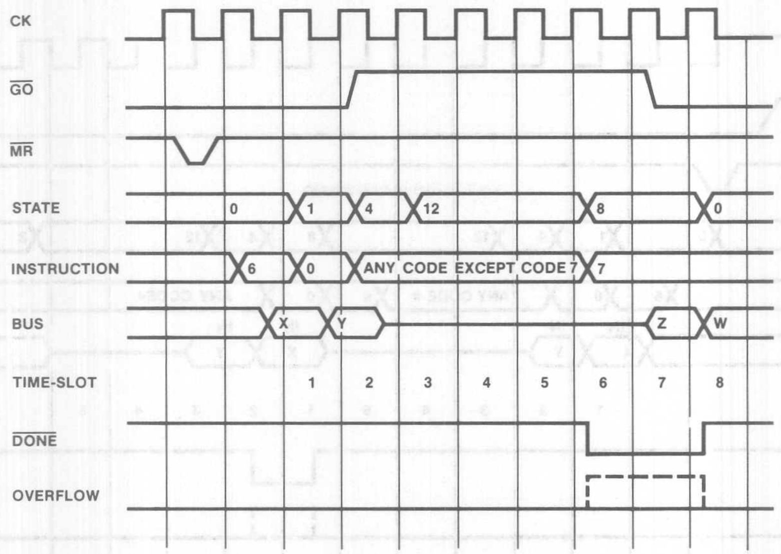


Figure 11 Instruction Timing Example #3: Load X, Load Y, Multiply, Read Z, Read W. This timing diagram corresponds to Table 1. Only after the "Done" signal is set (after four clock pulses of the operation cycles), the result is read — Z during time-slot 7, and W during time-slot 8.

NOTE: If code 7 is given (instead of code 0 through 6), the first data that is read from the bus after the DONE signal is set (time-slot 7) is W and not Z. However, Z is read at time-slot 8.
"Any code except 7" means code 0 through code 6.

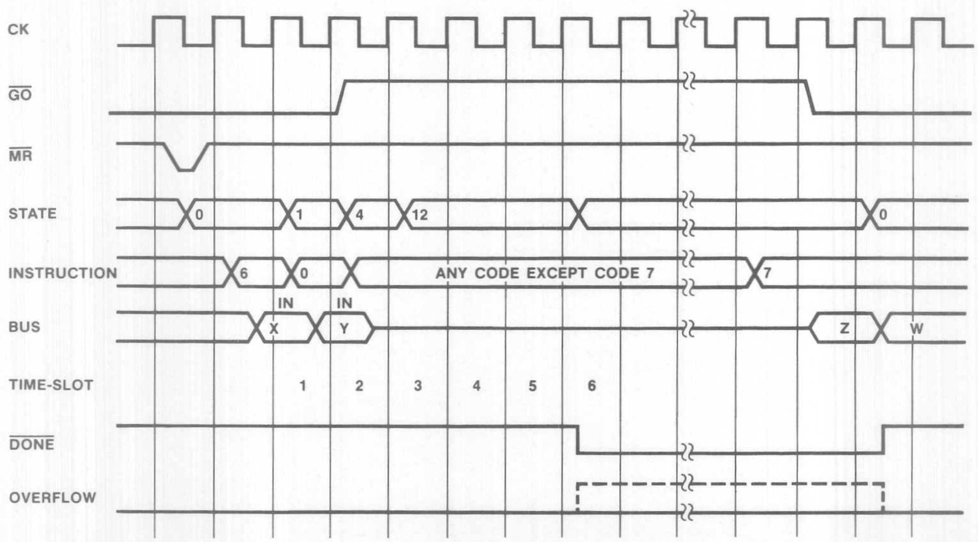


Figure 12 Instruction Timing Example #4: Load X, Load Y, Multiply, Wait, Read Z, Read W.

NOTE:
"Any code except 7" means code 0 through code 6.

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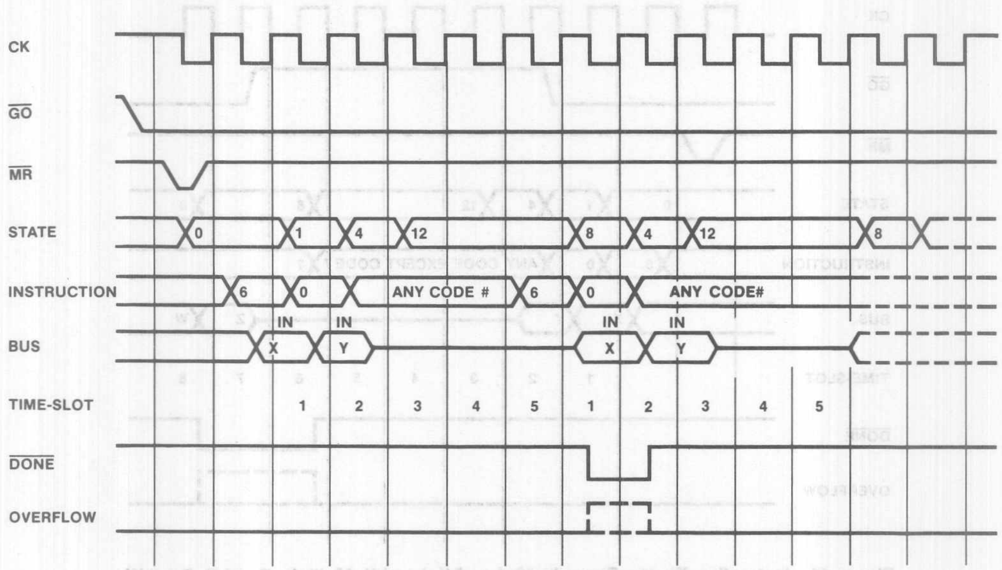


Figure 13 Instruction Timing Example #5: Sum of Products

NOTES: This sequence of operations is suitable for use when reading is to be done only at the very end of the operation sequence. New X and Y values are loaded during the time that the previous multiplication is being performed. See Programming Example #3 for

$$\sum_{i=1}^{N} X_i \cdot Y_i$$

#"Any code" means code 0 through code 7.

Programming Samples

In the following examples assume that each line with a separate instruction corresponds to one clock pulse. Instruction codes are 0, 1, 2, 3, 4, 5, 6, 7 and x according to the usage explained in the key to Figure 2.

Programming Example 1

Calculating X · Y (A · B)

INST 6 X ← A
INST 0 Y ← B
INST X MULT
INST X MULT
INST X MULT
INST 7 MULT and READ Z = 8 MSB OF (A·B)
INST 7 READ W = 8 LSB OF (A·B)

Programming Example 2

Calculating X1 · Y (A · C)

X1 is a previous multiplier value. It was previously loaded (in example 1) with A.

INST 0 Y ← C
INST X MULT
INST X MULT
INST X MULT
INST 7 MULT and READ Z = 8 MSB OF (A·C)
INST 7 READ W = 8 LSB OF (A·C)

Programming Example 3

Calculating $\sum_{i=1}^{N} X_i \cdot Y_i$ (A · B + C · D + E · F + ...)

In this case we read only after N multiplications. A new X_{i+1} is loaded during the multiplication process for X_iY_i.
Assume N = 3.
The sequence of instructions and operations for calculating

$\sum_{i=1}^{3} X_i \cdot Y_i$ is: (A · B + C · D + E · F)

N = 1
INST 6 X ← A
INST 0 Y ← B
INST X MULT
INST X MULT } Perform A · B
INST X MULT

N = 2
INST 6 MULT and LOAD X ← C
Z ← 8 MSB of (A·B)
W ← 8 LSB of (A·B)
INST 2 Y ← D
INST X MULT
INST X MULT } Perform C · D + (K_Z, K_W)
INST X MULT

N = 3
INST 6 MULT and LOAD X ← E
Z ← 8 MSB of (C·D + A·B)
W ← 8 LSB of (C·D + A·B)
INST 2 Y ← F
INST X MULT
INST X MULT } Perform E · F + (K_Z, K_W)
INST X MULT

READ Z
INST 7 MULT and
READ Z = 8 MSB of (E·F + C·D + A·B)

READ W
INST 7 READ W = 8 LSB of (E·F + C·D + A·B)

Programming Example 4

Multiplication plus a constant (A · B + Constant (16 bits))

Assume that the constant is a 16-bit 2s-complement number.

INST 6 X ← A
INST 6 Z ← C LOAD 8 MSB of constant
INST 6 W ← D LOAD 8 LSB of constant
INST 0 Y ← B
INST X MULT
INST X MULT } Perform A · B + (Z, W)
INST X MULT
INST 7 MULT and READ Z = 8 MSB of (A·B + (C, D))
INST 7 READ W = 8 LSB of (A·B + C, D)

Programming Example 5

Double-precision multiplication ((A, B) · (C, D))

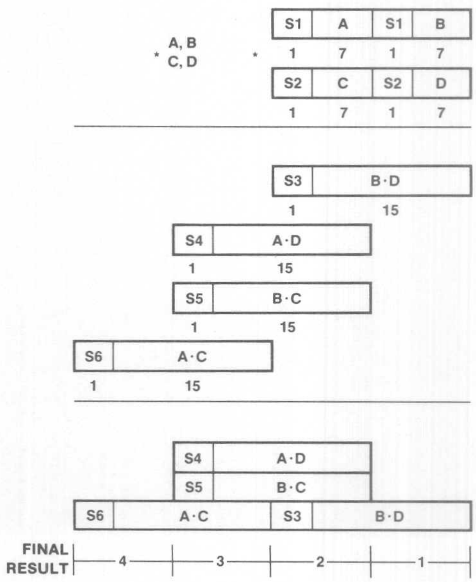
It is possible, using the 74S508, to multiply two numbers having up to 14 significant bits each.

Let S1 be the sign bit of the multiplier;
A be the 7 most-significant bits of the multiplier; and
B be the 7 least-significant bits of the multiplier.

S1 must be *duplicated* into the sign bit which goes with the 7 least significant bits, since the 7 most-significant bits and the 7 least-significant bits are used independently as two 2s-complement numbers.

Likewise let S2 be the sign bit of the multiplicand;
C be the 7 most-significant bits of the multiplicand; and
D be the 7 least-significant bits of the multiplicand.

S2 must be duplicated into the sign bit of the least-significant half in this case also, just as S1 was. The final result consists of a sign bit, plus 28 significant numeric bits, plus three "empty" bit positions. Such double-precision multiplication is common in floating-point operations. The following example will illustrate:



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INST 6	$X \leftarrow B$	
INST 0	$Y \leftarrow D$	
INST X	MULT	
INST X	MULT	Perform $X \cdot Y$
INST X	MULT	
INST 6	MULT and LOAD $X \leftarrow D$	
	Z = 8 MSB of $B \cdot D$	
	W = 8 LSB of $B \cdot D$	
	W = part 1 of final result and can be read now	
INST 6	NO-OP	
INST 2	$Y \leftarrow A$	
INST X	MULT	
INST X	MULT	Perform $X \cdot Y + K_Z \cdot 2^{-7}$
INST X	MULT	
INST 6	MULT and LOAD $X \leftarrow C$	
	Z = 8 MSB of $(A \cdot D + (B \cdot D) \cdot 2^{-7})$	
	W = 8 LSB of $(A \cdot D + (B \cdot D) \cdot 2^{-7})$	
	When $B \cdot D$ is shifted right 7 places, the sign bit S3 is extended.	
INST 2	$Y \leftarrow B$	
INST X	MULT	
INST X	MULT	Perform $X \cdot Y + (K_Z, K_W)$
INST X	MULT	
INST 6	MULT and LOAD $X \leftarrow A$	
	Z = 8 MSB of $(B \cdot C + \underbrace{(A \cdot D + (B \cdot D) \cdot 2^{-7})}_{K_Z})$	
	W = 8 LSB of $(B \cdot C + \underbrace{(A \cdot D + (B \cdot D) \cdot 2^{-7})}_{K_W})$	
	W = part 2 of the final result and can be read now.	
INST 6	NO-OP	
INST 2	$Y \leftarrow C$	
INST X	MULT	
INST X	MULT	Perform $X \cdot Y + K_Z \cdot 2^{-7}$
INST X	MULT	
INST 7	MULT and READ part 4 of the final result.	
	Z = 8 MSB of $(A \cdot C + (B \cdot C + (A \cdot D + (B \cdot D) \cdot 2^{-7})) \cdot 2^{-7})$	
INST 7	READ part 3 of the final result.	
	W = 8 LSB of $(A \cdot C + (B \cdot C + (A \cdot D + (B \cdot D) \cdot 2^{-7})) \cdot 2^{-7})$	

Programming Example 6

Dividing a 16-bit number by an 8-bit number ((B, C)/A)

INST 6	$X \leftarrow A$	
INST 6	$Z \leftarrow B$	
INST 4	$W \leftarrow C$	
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		Perform Division $\frac{(Z, W)}{X}$
INST X		
INST X		
INST X		
INST X		
INST X		
INST 7	DIVIDE and READ the quotient $Z = \frac{(B, C)}{A}$	
INST 7	READ the remainder W of $\frac{(B, C)}{A}$	

8 x 8 Multiplier

57/67558 57/67558-1

U.S. Patent 4153938

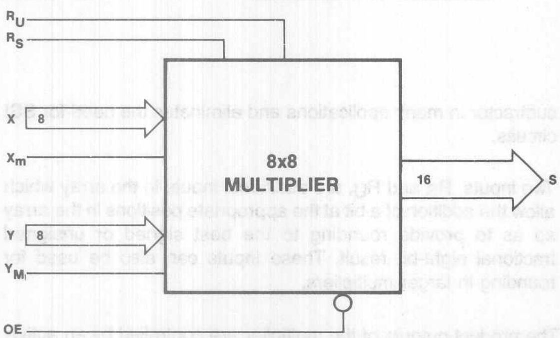
Features/Benefits

- Industry Standard
- Easy to Use; Combinatorial
- Unsigned, Signed, or Mixed Multiplication
- Rounding Inputs for Signed or Unsigned Operation
- Three-State Outputs for Bus Operation
- High Speed — 125 ns Max

Description

The 57558/67558 is a high speed 8 x 8 combinatorial Multiplier which can multiply two eight-bit unsigned or signed 2s complement numbers and generate the sixteen-bit unsigned or signed product. Each input operand X and Y has an associated Mode control line, X_M and Y_M respectively. When a Mode control line is at a Low logic level the operand is treated as an unsigned eight-bit number while if the Mode control is at a High logic level the operand is treated as an eight-bit signed 2s complement number. Two additional inputs R_S and R_U allow the addition of a bit in the multiplier array at the appropriate bit positions for rounding signed or unsigned fractional numbers. The most significant product bit is available in both True and Complement form to assist in expansion to larger signed multipliers. The product outputs are three-state, controlled by an active Low Output Enable which allows several Multipliers to be connected to a parallel bus or be used in a pipelined system. The device uses a single +5V power supply and is packaged in a standard 40-pin DIP.

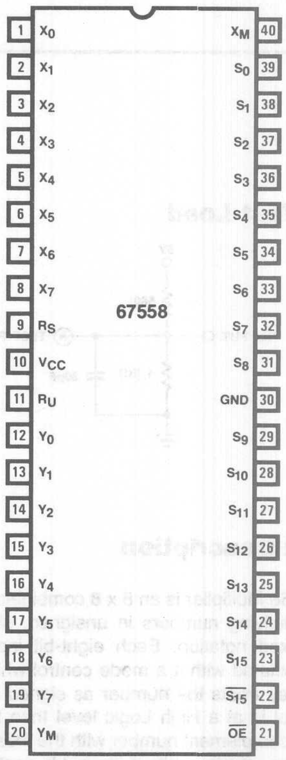
Logic Symbol



Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
57558, 57558-1	J40, F42	Military
67558, 67558-1	J40, F42	Commercial

Pin Configuration



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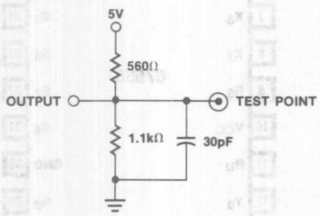
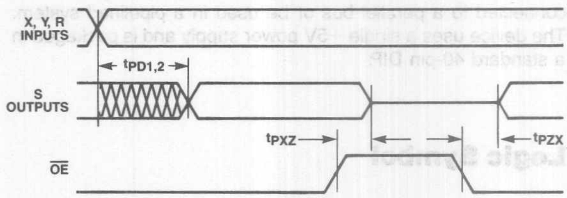
1165 East Arques Avenue, Sunnyvale, CA 94086 Tel: (408) 739-3535 TWX: 910-339-9229

SYMBOL	PARAMETER	DEVICE	TYP	MAX	UNIT
t_{PXZ}	Delay from OE to S High Impedance State	67558	30	40	ns
		57558	30	50	
		67558-1	30	40	
		57558-1	30	50	
t_{PZX}	Delay from OE to S Active State	67558	30	40	ns
		57558	30	50	
		67558-1	30	40	
		57558-1	30	50	
t_{PD1}	Delay from Y, X to S_{0-4}	67558	80	135	ns
		57558	80	140	
		67558-1	80	115	
		57558-1	80	125	
t_{PD2}	Delay from Y, X to S_{5-15}, $\overline{S}_{15}$	67558	100	150	ns
		57558	100	155	
		67558-1	100	125	
		57558-1	100	135	

Standard Test Load



Timing Waveform



Functional Description

The 57558/67558 Multiplier is an 8 x 8 combinatorial logic array capable of multiplying numbers in unsigned, signed 2s complement, or mixed notation. Each eight-bit input operand X and Y has associated with it a mode control which determines whether the array treats the number as signed or unsigned. If the mode control is at a High Logic level then the operand is treated as a 2s complement number with the most significant bit having a negative weight, while if the mode control is at a Low Logic level then the operand is treated as an unsigned number.

The multiplier provides all 16 product bits generated by the multiplication. For expansion during signed or mixed multiplication the most significant product bit has both true and complement available. This allows an adder to be used as a subtractor in many applications and eliminates the need for SSI circuits.

Two inputs, R_S and R_U, are additional inputs to the array which allow the addition of a bit at the appropriate positions in the array so as to provide rounding to the best signed or unsigned fractional eight-bit result. These inputs can also be used for rounding in larger multipliers.

The product outputs of the multiplier are controlled by an active Low Output Enable control. When this control is at a Low Logic level the multiplier outputs are active, while if the control is at a High Logic level then the outputs are placed in a high-impedance state. This three-state capability allows multipliers to be placed on a common bus and also allows pipelining of multiplications for higher speed systems.

Off-state output voltage 5.5V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125†	0		75	°C

†Case temperature

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5V			−1	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V			100	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −2mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.5V			−100	μA
I_{OZH}	Off-state output current	V_{CC} = MAX	V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0V	−10		−90	mA
I_{CC}	Supply current	V_{CC} = MAX			180	280	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Rounding

Multiplication of two n-bit operands results in 2n-bit product†. Therefore, in n-bit system it is necessary to convert the double-length product into a single-length product. This can be accomplished by truncating or rounding. The following examples, illustrate the difference between the two conversion techniques in decimal arithmetic.

$$\left.\begin{array}{l} 39.2 \rightarrow 39 \\ 39.6 \rightarrow 39 \end{array}\right\} \text{Truncating}$$

$$\left.\begin{array}{l} 39.2 + 0.5 = 39.7 \rightarrow 39 \\ 39.6 + 0.5 = 40.1 \rightarrow 40 \end{array}\right\} \text{Rounding}$$

Obviously, rounding maintains more precision then truncating, but it may take one more step to implement. The additional step involves adding one-half of the weight of the single length LSB to the MSB of the discarded part e.g. in decimal arithmetic rounding 39.28 to one decimal point is accomplished by adding 0.05 to the number and truncating the LSB.

$$39.28 + 0.05 = 39.33 \rightarrow 39.3$$

The situation in binary arithmetic is quite similar, but two cases need to be considered; signed and unsigned data representation. In signed multiplication, the two MSBs are identical (except when both operands are −1) therefore, the best single length product is shifted one position to the right with respect to the unsigned multiplications. Figure 1 illustrates these two cases for the 8x8 multiplier. In the signed case, adding one-half of the S_7 weight is accomplished by adding 1 in bit position 6, and in the unsigned case 1 is added to bit position 7. Therefore, the 67558 multiplier has two rounding inputs, R_S and R_U. Thus, to get a rounded single length result the appropriate R input is tied to V_{CC} (logic one) and the other R input is grounded. If double length result is desired both R inputs are grounded.

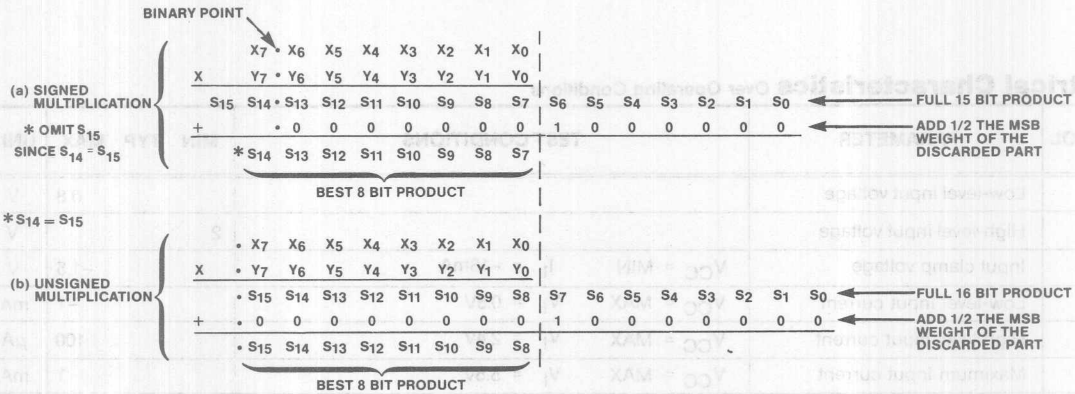


Figure 1. Rounding the Result of Binary Fractional Multiplication.

(a) In signed (2's complement) notation, the MSB of each operand is the sign bit, and the binary point is to the right of the MSB. The resulting product has a redundant sign bit and the binary point is to the right of the second MSB of the product. The best eight-bit product is from S_{14} through S_7, and rounding is performed by adding "1" to bit position S_6.

(b) In unsigned notation the best 8-bit product, is the most significant half of the product, corrected by adding "1" to bit position S_7.

† In general: multiplication of M-bit operand by N-bit operand results in M + N bit product.

Signed Expansion

The most significant product bit has both true and complement outputs available. When building larger signed multipliers the partial products except at the lower stages are signed numbers. These unsigned and signed partial products must be added together to give the correct signed product. Having both the true and complement of the most significant product bit available assists in this addition. For example, say that two signed partial products must be added and MSI adders are used; we then have the situation of adding together the Carry from the previous adder stage plus the addition of the two negative most significant partial product bits. The result of adding these variables must be a positive sum and a negative carry (borrow). The equations for this are:

$$S = A \oplus B \oplus C$$

$$C_0 = AB + BC + CA$$

where C is the Carry In and A and B the sign bits of the two partial products.

Now an adder produces the equations:

$$S = A \oplus B \oplus C$$

$$C_0 = AB + BC + CA$$

Examining these equations it can be seen that if the inversion of A and B are used then the adder produces the inversion of the negative carry since

$$AB + B\bar{C} + \bar{C}A = \overline{\bar{A}\bar{B} + BC + C\bar{A}},$$

and the sum remains the same.

16 x 16 Two's Complement Multiplication

The 16-bit X operand is broken into two 8-bit operands (X_0-X_7 and X_8-X_{15}), and so is the Y operand. Since the situation is that of a cross product, four partial products are generated as follows:

$$A = X_L * Y_L$$
$$B = X_L * Y_H$$
$$C = X_H * Y_L$$
$$D = X_H * Y_H$$

where the subscript L stands for bits 0-7, and the subscript H stands for bits 8-15.

Expanding in two's complement multiplication requires a sign extension of the B and C partial products. Thus, B_{15} and C_{15} need to be extended eight positions to the left (to align with D_{15}). In this approach two more adders are required. But the complement of the MSB (S_{15}) on the 67558 can be used to save these two adders. The Figure shows the implementation of such a 16x16 signed two's complement multiplication.

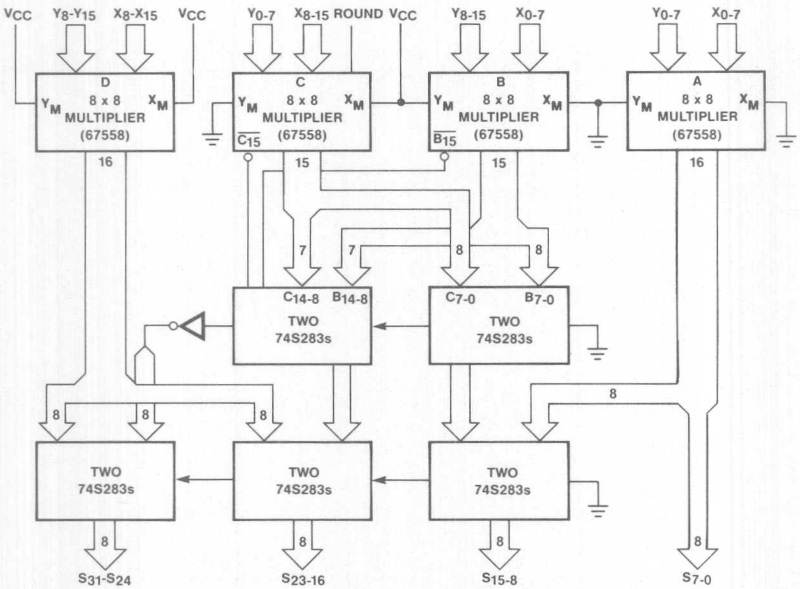


Figure 2. 16 x16 Two's Complement Signed Multiplication.

																X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0
																Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
								B_{15}	B_{14}	B_{13}	B_{12}	B_{11}	B_{10}	B_9	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0								
D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
								C_{15}	C_{14}	C_{13}	C_{12}	C_{11}	C_{10}	C_9	C_8	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0								
S_{31}	S_{30}	S_{29}	S_{28}	S_{27}	S_{26}	S_{25}	S_{24}	S_{23}	S_{22}	S_{21}	S_{20}	S_{19}	S_{18}	S_{17}	S_{16}	S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

$\underbrace{S_{31} \ldots S_{16}}_{\text{ROUNDED RESULT}}$

Figure 3. Unsigned Expansions of the 8x8 Multiplier to 16x16 Multiplication.

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Octal Interface Selection Guide

Buffer	LS	Non-invert	—	SN74LS241	SN54LS241
			Schmitt Trigger	SN74LS344	SN54LS344
			Schmitt Trigger	SN74LS341	SN54LS341
		Invert	—	SN74LS210	SN54LS210
			—	SN74LS240	SN54LS210
			Schmitt Trigger	SN74LS310	SN54LS310
			Schmitt Trigger	SN74LS340	SN54LS340
	S	Non-invert	—	SN74S244	SN54S244
			—	SN74S241	SN54S241
		Invert	—	SN74S210	SN54S210
			—	SN74S240	SN54S240
Transceiver	LS	Non-invert	—	SN74LS245	SN54LS245
			—	SN74LS645	SN54LS645
			48mA I_{OL}	SN74LS645-1	—
Latch	LS	Non-invert	—	SN74LS373	SN54LS373
		Invert	—	SN74LS533	SN54LS533
	S	Non-invert	—	SN74S373	SN54S373
			32mA I_{OL}	SN74S531	—
		Invert	—	SN74S533	SN54S533
			32mA I_{OL}	SN74S535	—
Register	LS	Non-invert	Master Reset	SN74LS273	SN54LS273
			—	SN74LS374	SN54LS374
			Clock Enable	SN74LS377	SN54LS377
		Invert	—	SN74LS534	SN54LS534
	S	Non-invert	—	SN74S374	SN54S374
			32mA I_{OL}	SN74S532	—
		Invert	—	SN74S534	SN54S534
			32mA I_{OL}	SN74S536	—

Conversion Guide — Monolithic Memories Interface Part Numbers

OLD → NEW

Old 57/67	New SN54/74	Description
'LS300	**'LS340**	Octal Buffer, Invert, Schmitt Trigger
'LS301	**'LS341**	Octal Buffer, Schmitt Trigger
'LS304	**'LS344**	Octal Buffer, Schmitt Trigger
'LS376	**'LS534**	Octal Register, Invert
'LS380	**'LS533**	Octal Latch, Invert
'S373	**'S531**	Octal Latch, Hi-Drive
'S374	**'S532**	Octal Register, Hi-Drive
'S376	**'S534**	Octal Register, Invert
'S378	**'S536**	Octal Register, Invert, Hi-Drive
'S380	**'S533**	Octal Latch, Invert
'S382	**'S535**	Octal Latch, Invert, Hi-Drive

NEW → OLD

New SN54/74	Old 57/67	Description
'LS340	'LS300	Octal Buffer, Invert, Schmitt Trigger
'LS341	'LS301	Octal Buffer, Schmitt Trigger
'LS344	'LS304	Octal Buffer, Schmitt Trigger
'LS533	'LS380	Octal Latch, Invert
'LS534	'LS376	Octal Register, Invert
'S531	'S373	Octal Latch, Hi-Drive
'S532	'S374	Octal Register, Hi-Drive
'S533	'S380	Octal Latch, Invert
'S534	'S376	Octal Register, Invert
'S535	'S382	Octal Latch, Invert, Hi-Drive
'S536	'S378	Octal Register, Invert, Hi-Drive

Octal Buffers

SN54/74LS210 SN54/74S210
SN54/74LS240 SN54/74S240
SN54/74LS241 SN54/74S241
SN54/74LS244 SN54/74S244

Features/Benefits

- Three-state outputs drive bus lines
- Low current PNP inputs reduce loading
- 20-pin SKINNYDIP® saves space
- 8 bits matches byte boundaries
- Ideal for microprocessor interface
- Complementary-enable '210 and '241 types combine multiplexer and driver functions

Description

These octal buffers provide high speed and high current interface capability for bus organized digital systems. The three-state drivers will source a termination to ground (up to 133Ω) or sink a pull-up to V_{CC} as in the popular 220Ω/330Ω computer peripheral termination. The PNP inputs provide improved fan-in with 0.2 mA I_{IL} on the low-power Schottky buffers and 0.4 mA I_{IL} on the Schottky buffers.

The '240 and '244 provide inverting and non-inverting outputs respectively with assertive low enables. The '210 and '241 also provide inverting and non-inverting outputs respectively, but with complementary (both assertive-low and assertive-high) enables, to allow transceive or multiplexer operation.

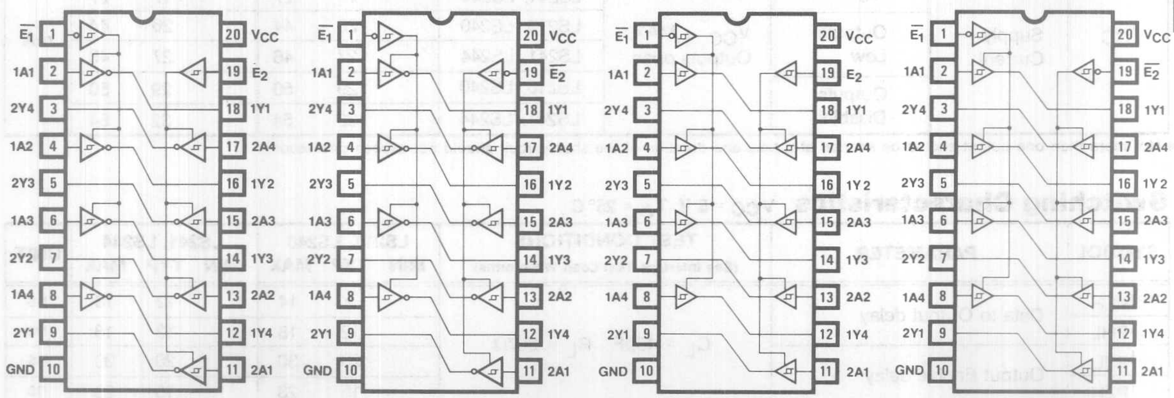
All of the octal devices are packaged in the popular 20-pin SKINNYDIP®.

Ordering Information

PART NUMBER	PKG	TEMP.	ENABLE	POLARITY	POWER
SN54LS210 SN74LS210	J,F N,J	mil com	HIGH- LOW	Invert	LS
SN54LS240 SN74LS240	J,F N,J	mil com	LOW		
SN54LS241 SN74LS241	J,F N,J	mil com	HIGH- LOW	Non- invert	
SN54LS244 SN74LS244	J,F N,J	mil com	LOW		
SN54S210 SN74S210	J,F N,J	mil com	HIGH- LOW	Invert	S
SN54S240 SN74S240	J,F N,J	mil com	LOW		
SN54S241 SN74S241	J,F N,J	mil com	HIGH- LOW	Non- Invert	
SN54S244 SN74S244	J,F N,J	mil com	LOW		

Logic Symbols

210 Octal Buffer 240 Octal Buffer 241 Octal Buffer 244 Octal Buffer



SKINNYDIP is a registered trademark of Monolithic Memories

1165 East Arques Avenue, Sunnyvale, CA 94086 Tel: (408) 739-3535 TWX: 910-339-9229

Monolithic Memories

Absolute Maximum Ratings

Supply Voltage V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature .... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA			−1.5			−1.5	V
ΔV_T	Hysteresis $(V_{T+} - V_{T-})$	V_{CC} = MIN		0.2	0.4		0.2	0.4		V
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			−0.2			−0.2	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V			20			20	μA
I_I	Maximum input current	V_{CC} = MAX,	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 12mA			0.4			0.4	V
			I_{OL} = 24mA						0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.5V, V_{IH} = 2V	I_{OH} = −3mA	2.4	3.4		2.4	3.4		V
			I_{OH} = −12mA	2						
			I_{OH} = −15mA				2			
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4V			−20			−20	μA
I_{OZH}			V_O = 2.7V			20			20	μA
I_{OS}	Output short-circuit current*	V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply Current — Outputs High	V_{CC} = MAX, Outputs open	LS210, LS240		17	27		17	27	mA
			LS241, LS244		17	27		17	27	
	Supply Current — Outputs Low		LS210, LS240		26	44		26	44	
			LS241, LS244		27	46		27	46	
	Supply Current — Outputs Disabled		LS210, LS240		29	50		29	50	
			LS241, LS244		32	54		32	54	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	LS210, LS240 MIN	LS210, LS240 TYP	LS210, LS240 MAX	LS241, LS244 MIN	LS241, LS244 TYP	LS241, LS244 MAX	UNIT
t_{PLH}	Data to Output delay	C_L = 45pF R_L = 667Ω		9	14		12	18	ns
t_{PHL}				12	18		12	18	ns
t_{PZL}	Output Enable delay			20	30		20	30	ns
t_{PZH}				15	23		15	23	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		15	25		15	25	ns
t_{PHZ}				10	18		10	18	ns

Absolute Maximum Ratings

Supply Voltage V_{CC} 7V
Input Voltage 5.5V
Off-state output voltage 5.5V
Storage temperature .... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125 *	0		75	°C

* The SN54S241/244J operating at free air temperature above 116°C requires a heat sink such that $R_{\theta CA}$ is not more than 40°C/W.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = –18mA			–1.2			–1.2	V
ΔV_T	Hysteresis ($V_{T+}-V_{T-}$)		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
I_{IL}	Low-level input current	Any A	V_{CC} = MAX	V_I = 0.5V			–0.4			–0.4	mA
		Any E					–2			–2	
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7V			50			50	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5V			1			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 48mA			0.55				V
				I_{OL} = 64mA						0.55	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = –1mA				2.7			V
				I_{OH} = –3mA	2.4	3.4		2.4	3.4		
				I_{OH} = –12mA	2						
				I_{OH} = –15mA				2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			–50			–50	μA
I_{OZH}				V_O = 2.4V			50			50	μA
I_{OS}	Output short-circuit current †		V_{CC} = MAX		–50		–225	–50		–225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX Outputs open	S210,S240		80	123		80	135	mA
				S241,S244		95	147		95	160	
		Outputs Low		S210,S240		100	145		100	150	
				S241,S244		120	170		120	180	
		Outputs Disabled		S210,S240		100	145		100	150	
				S241,S244		120	170		120	180	

† Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)		S210, S240 MIN	S210, S240 TYP	S210, S240 MAX	S241, S244 MIN	S241, S244 TYP	S241, S244 MAX	UNIT
t_{PLH}	Data to Output delay	C_L = 50pF R_L = 90Ω			4.5	7		6	9	ns
t_{PHL}					4.5	7		6	9	ns
t_{PZL}	Output Enable delay				10	15		10	15	ns
t_{PZH}			S210		6.5	12		8	12	ns
			S240			10				ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 90Ω			10	15		10	15	ns
t_{PHZ}					6	9		6	9	ns

Features/Benefits

- Schmitt trigger guarantees high noise margin
- 3-state outputs drive bus lines
- Low current PNP inputs reduce loading
- 20-pin SKINNYDIP® saves space
- 8 bits matches byte boundaries
- Ideal for microprocessor interface
- Complementary-enable '310 and '341 types combine multiplexer and driver functions
- Pin-compatible with SN54/74LS210/240/1/4 — can be direct replacement in systems with noise problems

Ordering Information

PART NUMBER	PKG	TEMP.	ENABLE	POLARITY	POWER
SN54LS310	J,F	mil	HIGH-LOW	Invert	LS
SN74LS310	N,J	com			
SN54LS340	J,F	mil	LOW		
SN74LS340	N,J	com			
SN54LS341	J,F	mil	HIGH-LOW	Non-invert	
SN74LS341	N,J	com			
SN54LS344	J,F	mil	LOW		
SN74LS344	N,J	com			

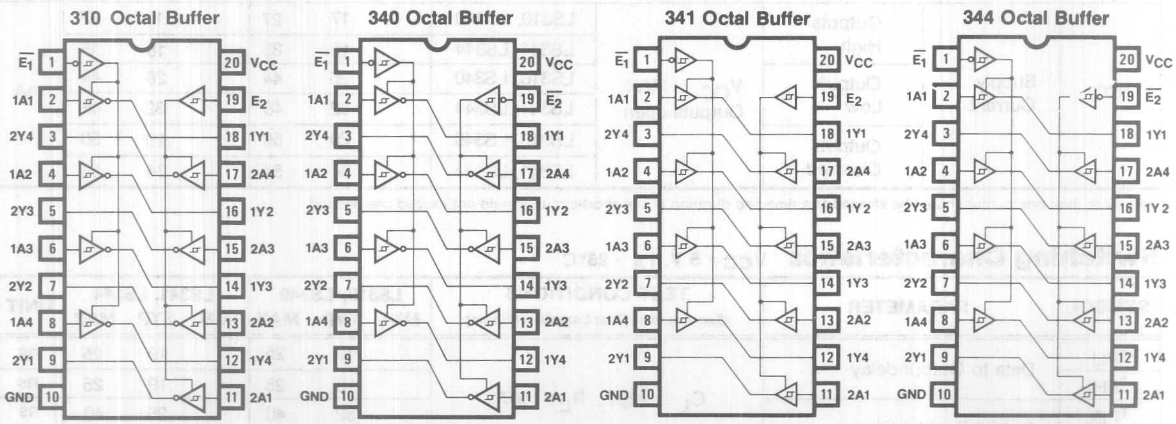
Description

In addition to the standard Schottky and low-power Schottky octal buffers, Monolithic Memories provides full hysteresis with a "true" Schmitt-trigger circuit. The improved performance characteristics are designed to be consistent with the SN54/74LS14 hex Schmitt-trigger and guarantee a full 400 mV noise immunity. The Schmitt-trigger operation makes the LS buffers ideal for bus receivers in a noisy environment.

The octal buffers provide high-speed and high-current interface capability for bus-organized digital systems. The PNP inputs provide improved fan-in with 0.2 mA I_{IL}. The '340 and '344 provide inverting and non-inverting outputs respectively, with assertive-low enables. The '310 and '341 also provide inverting and non-inverting outputs respectively, but with complementary (both assertive-low and assertive-high) enables, to allow transceiver or multiplexer operation.

All of the octal devices are packaged in the popular 20-pin SKINNYDIP®.

Logic Symbols



SKINNYDIP is a registered trademark of Monolithic Memories

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Absolute Maximum Ratings

Supply Voltage V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature .... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{T+}	Positive threshold voltage	V_{CC} = 5V		1.5	1.7	2.0	1.5	1.7	2.0	V
V_{T-}	Negative threshold voltage	V_{CC} = 5V		0.6	0.9	1.1	0.6	0.9	1.1	V
V_{IC}	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA			−1.5			−1.5	V
ΔV_T	Hysteresis $(V_{T+}-V_{T-})$	V_{CC} = 5V		0.4	0.8		0.4	0.8		V
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			−0.2			−0.2	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V			20				μA
I_I	Maximum input current	V_{CC} = MAX,	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{T+} = 2V, V_{T-} = 0.6V	I_{OL} = 12mA			0.4			0.4	V
			I_{OL} = 24mA						0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{T+} = 2V, V_{T-} = 0.6V	I_{OH} = −3mA	2.4	3.4		2.4	3.4		V
			I_{OH} = −12mA	2						
			I_{OH} = −15mA				2			
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{T+} = 2V, V_{T-} = 0.6V	V_O = 0.4V			−20			−20	μA
I_{OZH}			V_O = 2.7V			20			20	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply Current — Outputs High	V_{CC} = MAX, Outputs open	LS310, LS340		17	27		17	27	mA
			LS341, LS344		18	35		18	35	
	Supply Current — Outputs Low		LS310, LS340		26	44		26	44	
			LS341, LS344		32	46		32	46	
	Supply Current — Outputs Disabled		LS310, LS340		29	50		29	50	
			LS341, LS344		34	54		34	54	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	LS310, LS340 MIN	LS310, LS340 TYP	LS310, LS340 MAX	LS341, LS344 MIN	LS341, LS344 TYP	LS341, LS344 MAX	UNIT
t_{PLH}	Data to Output delay	C_L = 45pF R_L = 667Ω		19	25		19	25	ns
t_{PHL}				19	25		19	25	ns
t_{PZL}	Output Enable delay			32	40		25	40	ns
t_{PZH}				23	35		24	35	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		18	30		21	30	ns
t_{PHZ}				15	25		18	25	ns

Octal Transceiver

SN54/74LS245

Features/Benefits

- **3-state outputs drive bus lines**
- **Low current PNP inputs reduce loading**
- **Symmetric -- equal driving capability in each direction**
- **20-pin SKINNYDIP® saves space**
- **8 bits matches byte boundaries**
- **Ideal for microprocessor interface**
- **Pin-compatible with SN54/74LS645 -- improved speed, I_{IL} and I_{OZL} specifications**

Ordering Information

PART NUMBER	TYPE	TEMP	POLARITY	POWER
SN54LS245	J, F	mil	Non-	LS
SN74LS245	N,J	com	invert	

Description

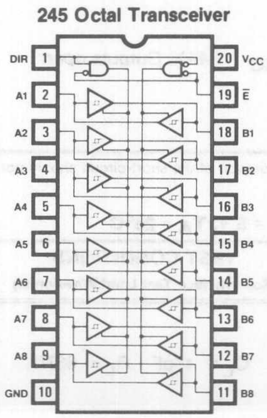
These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\bar{E}$) can be used to disable the device so that the buses are effectively isolated. All of the octal devices are packaged in the popular 20-pin SKINNYDIP®.

Function Table

ENABLE $\bar{E}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolated

Logic Symbol



Absolute Maximum Ratings

Supply Voltage V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage				0.7			0.8	V
V_{IH}	High-level input voltage		2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN, I_I = −18mA			−1.5			−1.5	V
ΔV_T	Hysteresis ($V_{T+}-V_{T-}$) A or B	V_{CC} = MIN	0.2	0.4		0.2	0.4		V
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V			−0.2			−0.2	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V			20			20	μA
I_I	Maximum input current, A or B	V_{CC} = MAX, V_I = 5.5V			0.1			0.1	mA
	Maximum input current, DIR or $\bar{E}$	V_{CC} = MAX, V_I = 7.0V			0.1			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V, I_{OL} = 12mA		0.25	0.4		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V, I_{OL} = 24mA					0.35	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V, I_{OH} = −3mA	2.4	3.4		2.4	3.4		V
		I_{OH} = −12mA	2			2			V
		I_{OH} = −15mA				2			V
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V, V_O = 0.4V			−200			−200	μA
I_{OZH}	Off-state output current	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V, V_O = 2.7V			10			10	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX	−40		−225	−40		−225	mA
I_{CC}	Supply Current, Outputs High	V_{CC} = MAX, Outputs open		48	70		48	70	mA
	Supply Current, Outputs Low	V_{CC} = MAX, Outputs open		62	90		62	90	mA
	Supply Current, Outputs Disabled	V_{CC} = MAX, Outputs open		64	95		64	95	mA

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	A to B DIRECTION MIN	A to B DIRECTION TYP	A to B DIRECTION MAX	B to A DIRECTION MIN	B to A DIRECTION TYP	B to A DIRECTION MAX	UNIT
t_{PLH}	Data to Output delay	C_L = 45pF R_L = 667Ω		8	12		8	12	ns
t_{PHL}	Data to Output delay	C_L = 45pF R_L = 667Ω		8	12		8	12	ns
t_{PZL}	Output Enable delay	C_L = 45pF R_L = 667Ω		27	40		27	40	ns
t_{PZH}	Output Enable delay	C_L = 45pF R_L = 667Ω		25	40		25	40	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		15	25		15	25	ns
t_{PHZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		15	25		15	25	ns

Octal Transceivers

SN54/74LS645 SN74LS645-1

Features/Benefits

- 3-state outputs drive bus lines
- Low current PNP inputs reduce loading
- Symmetric — equal driving capability in each direction
- 20-pin SKINNYDIP® saves space
- 8 bits matches byte boundaries
- Ideal for microprocessor interface
- SN74LS645-1 rated at I_{OL} = 48 mA

Ordering Information

PART NUMBER	TYPE	TEMP	POLARITY	POWER
SN54LS645	J,F	mil	Non-invert	LS
SN74LS645	N,J	com		
SN74LS645-1	N,J	com		

Description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

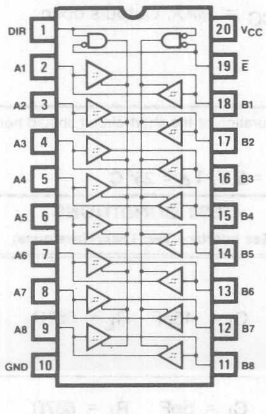
The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{E}$) can be used to disable the device so that the buses are effectively isolated. All of the octal devices are packaged in the popular 20-pin SKINNYDIP®.

Function Table

ENABLE $\overline{E}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolated

Logic Symbol

645/645-1 Octal Transceiver



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Absolute Maximum Ratings

Supply Voltage V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.5			0.6	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA			−1.5			−1.5	V
	Hysteresis $(V_{T+} - V_{T-})$ A or B	V_{CC} = MIN		0.1	0.4		0.2	0.4		V
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			−0.4			−0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V			20			20	μA
I_I	Maximum input current	V_{CC} = MAX,	V_I = 5.5V			0.1			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 12mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24mA					0.35	0.5	
			I_{OL} = 48mA†					0.4	0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OH} = −3mA	2.4	3.4		2.4	3.4		V
			I_{OH} = −12mA	2						
			I_{OH} = −15mA				2			
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4V			−400			−400	μA
I_{OZH}			V_O = 2.7V			20			20	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply Current — Outputs High	V_{CC} = MAX, Outputs open			48	70		48	70	mA
	Supply Current — Outputs Low				62	90		62	90	
	Supply Current — Outputs Disabled				64	95		64	95	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† This specification applies only to the SN74LS645-1.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	A TO B DIRECTION MIN	A TO B DIRECTION TYP	A TO B DIRECTION MAX	B TO A DIRECTION MIN	B TO A DIRECTION TYP	B TO A DIRECTION MAX	UNIT
t_{PLH}	Data to Output delay	C_L = 45pF R_L = 667Ω		8	15		8	15	ns
t_{PHL}				11	15		11	15	ns
t_{PZL}	Output Enable delay			31	40		31	40	ns
t_{PZH}				26	40		26	40	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		15	25		15	25	ns
t_{PHZ}				15	25		15	25	ns

Octal Registers With Master Reset and Clock Enable

SN54/74LS273 SN54/74LS377

Features

- 20-Pin Skinny DIP™ Saves Space
- 8 Bits Matches Byte Boundaries
- Ideal for Microprogram Instruction Registers
- Ideal for Microprocessor Interface
- Suitable for Pipeline Data Registers
- Useful in Timing, Sequencing, and Control Circuits
- 3 LS273s May Replace 4 LS174s
- 3 LS377s May Replace 4 LS378s

Description

These octal registers contain 8 D-type flip-flops and feature very low I_{CC} (17 mA typ). The LS273 register is loaded on the rising edge of the clock (CK) and asynchronously cleared whenever the master reset line, $\overline{MR}$, is low. The LS377 register is loaded on the rising edge of the clock provided that the clock enable line, $\overline{CK\ EN}$, is low.

Function Table LS273

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

Function Table LS377

INPUTS			OUTPUT
$\overline{CK\ EN}$	CLOCK	DATA	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0

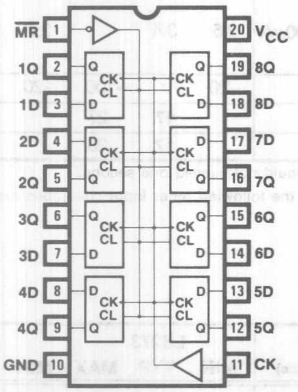
Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	CONTROL OPTION	POWER
SN54LS273	J,F	mil	Non-invert	Register	Clear	LS
SN74LS273	N,J	com				
SN54LS377	J,F	mil			Clock Enable	
SN74LS377	N,J	com				

Logic Symbols

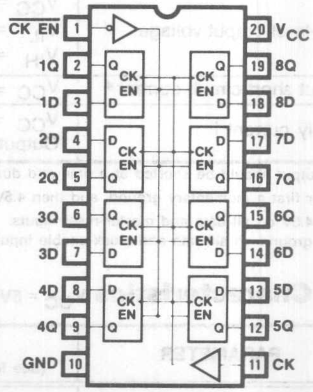
Octal Register with Master Reset

LS273



Octal Register with Clock Enable

LS377



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Off-state output voltage 5.5V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of Clock/Master Reset	High	20			20			ns
		Low	20			20			ns
t_{su}	Setup time	Data input	20↑			20↑			ns
		Reset inactive state ('LS273 only)	25↑			25↑			ns
		Clock enable active state ('LS377 only)	25↑			25↑			ns
		Clock enable inactive state ('LS377 only)	10↑			10↑			ns
t_h	Hold time	Data input	5↑			5↑			ns
		Clock enable ('LS377 only)	5↑			5↑			ns
T_A	Operating free air temperature		−55		125	0		75	°C

↑↓The arrow indicates the transition of the clock/enable input used for reference. ↑ for the low-to-high transition, ↓ for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.5			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			−0.4			−0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			20			20	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 4mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8mA					0.35	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OH} = −400μA	2.5	3.4		2.7	3.4		V
I_{OS}	Output short-circuit current *	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current †	V_{CC} = MAX, Outputs open	LS273		17	27		17	27	mA
			LS377		17	28		17	28	mA

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
†I_{CC} is measured after first a momentary ground, and then 4.5V, is applied to clock, while the following other input conditions are held:
(a) for the 'LS273 — 4.5V on all data and master-reset inputs.
(b) for the 'LS377 — ground on all data and clock-enable inputs.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	LS273 MIN	LS273 TYP	LS273 MAX	LS377 MIN	LS377 TYP	LS377 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 2kΩ	30	40		30	40		MHz
t_{PLH}	Clock/Reset to output delay				27			27	ns
t_{PHL}					27			27	ns

Octal Latches, Octal Registers

SN54/74LS373 SN54/74S373
SN54/74LS374 SN54/74S374

Features/Benefits

- 3-state outputs drive bus lines
- 20-pin SKINNYDIP® saves space
- 8 bits matches byte boundaries
- Hysteresis improves noise margin
- Low current PNP inputs reduce loading
- Ideal for microprocessor interface

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN54LS373 SN74LS373	J,F N,J	mil com	Non-invert	Latch	LS
SN54LS374 SN74LS374	J,F N,J	mil com		Register	
SN54S373 SN74S373	J,F N,J	mil com		Latch	S
SN54S374 SN74S374	J,F N,J	mil com		Register	

Description

The latch passes eight (octal) bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight (octal) bits of input data and passes it to the output on the "rising edge" of the clock.

The three-state outputs are active when $\overline{OE}$ is low, and high-impedance when $\overline{OE}$ is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the octal devices are packaged in the popular 20-pin SKINNYDIP®.

Function Tables

373 Octal Latch

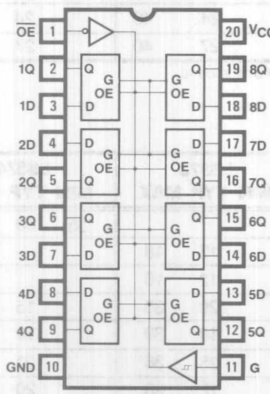
$\overline{OE}$	G	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

374 Octal Register

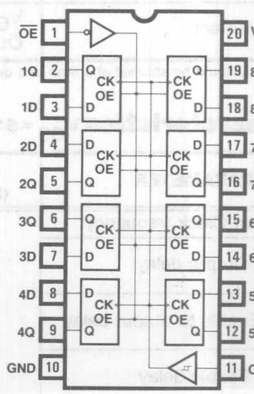
$\overline{OE}$	CK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

Logic Symbols

373 Octal Latch



374 Octal Register



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Monolithic Memories MMI

Absolute Maximum Ratings

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Off-state output voltage	5.5V
Storage temperature	-65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature		–55		125	0		75	°C
t_w	Width of Clock/Gate	High	15			15			ns
		Low	15			15			
t_{su}	Setup time		0↓			20↑			ns
t_h	Hold time		10↓			0↑			ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA			–1.5			–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			–0.4			–0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			20			20	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 12mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24mA					0.35	0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OH} = –1mA	2.4	3.4					V
			I_{OH} = –2.6mA				2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4V			–20			–20	μA
I_{OZH}			V_O = 2.7V			20			20	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX		-30		–130	-30		–130	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	LS373		24	40		24	40	mA
			LS374		27	40		27	40	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Charcteristics $V_{CC} = 5V, T_A = 25°C$

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	LS373 MIN	LS373 TYP	LS373 MAX	LS374 MIN	LS374 TYP	LS374 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 45pF R_L = 667Ω				35	50		MHz
t_{PLH}	Data to Output delay			12	18				ns
t_{PHL}				12	18				ns
t_{PLH}	Clock/Enable to output delay			20	30		15	28	ns
t_{PHL}				18	30		19	28	ns
t_{PZL}	Output Enable delay			25	36		21	28	ns
t_{PZH}				15	28		20	28	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		15	25		14	25	ns
t_{PHZ}				12	20		12	20	ns

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Off-state output voltage 5.5V
Storage temperature .... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature		–55		125	0		75	°C
t_w	Width of Clock/Gate	High	6			6			ns
		Low	7.3			7.3			
t_{su}	Set up time	S373	0↓			0↓			ns
		S374	5↑			5↑			
t_h	Hold time	S373	10↓			10↓			ns
		S374	2↑			2↑			

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA			–1.2			–1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5V			–0.25			–0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			50			50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 20mA			0.5			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OH} = –2mA	2.4	3.4					V
			I_{OH} = –6.5mA				2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX V_{IL} = 0.8V V_{IH} = 2V	V_O = 0.5V			–50			–50	μA
I_{OZH}			V_O = 2.4V			50			50	μA
I_{OS}	Output short-circuit current*	V_{CC} = MAX		–40		–100	–40		–100	mA
I_{CC}	Supply current	V_{CC} = MAX Outputs open	S373		105	160		105	160	mA
			S374		90	140		90	140	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	S373 MIN	S373 TYP	S373 MAX	S374 MIN	S374 TYP	S374 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 280Ω				75	100		MHz
t_{PLH}	Data to Output delay			7	12				ns
t_{PHL}				7	12				ns
t_{PLH}	Clock/Enable to output delay			7	14		8	15	ns
t_{PHL}				12	18		11	17	ns
t_{PZL}	Output Enable delay			11	18		11	18	ns
t_{PZH}				8	15		8	15	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 280Ω		8	12		7	12	ns
t_{PHZ}				6	9		5	9	ns

SN54/74LS533 SN54/74S533
SN54/74LS534 SN54/74S534

Features/Benefits

- Inverting outputs
- 3-state outputs drive bus lines
- 20-pin SKINNYDIP® saves space
- 8 bits matches byte boundaries
- Hysteresis improves noise margin
- Low current PNP inputs reduce loading
- Ideal for microprocessor interface
- Pin-compatible with SN54/74LS373/4 — can be direct replacement when bus polarity must be changed

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
54LS533 74LS533	J,F N,J	mil com	Invert	Latch	LS
54LS534 74LS534	J,F N,J	mil com	Invert	Register	LS
54S533 74S533	J,F N,J	mil com	Invert	Latch	S
54S534 74S534	J,F N,J	mil com	Invert	Register	S

Description

In addition to the standard S and LS latches and registers, Monolithic Memories provides inverting outputs instead of non-inverting outputs. The inverting outputs are intended for bus applications that require inversion an in interfacing the Am2901A 4-Bit Slice to an assertive-low bus.

The latch passes eight (octal) bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight (octal) bits of input data and passes it to the output on the "rising edge" of the clock.

The three-state outputs are active when $\overline{OE}$ is low, and high-impedance when OE is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the octal devices are packaged in the popular 20-pin SKINNYDIP®.

Function Tables

533 Octal Latch (Inverting)

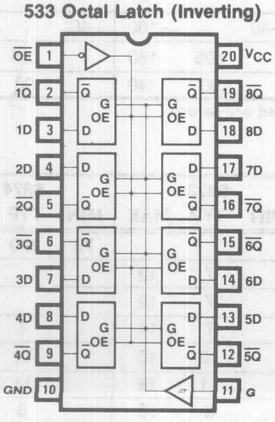
$\overline{OE}$	G	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

534 Octal Register (Inverting)

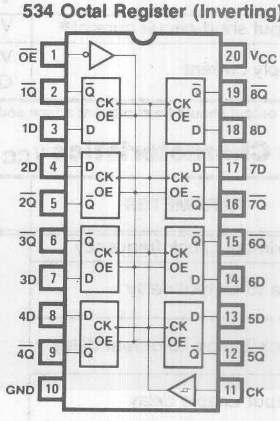
$\overline{OE}$	CK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	Q_0
H	X	X	Z

Logic Symbols

533 Octal Latch (Inverting)



534 Octal Register (Inverting)



1165 East Arques Avenue, Sunnyvale, CA 94086 Tel: (408) 739-3535 TWX: 910-339-9229

Monolithic Memories

. . . 7V
Input Voltage . . . 7V
Off-state output voltage . . . 5.5V
Storage temperature . . . -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of Clock/Gate	High	15			15			ns
		Low	15			15			
t_{su}	Set up time	LS533	0↓			0↓			ns
		LS534	20↑			20↑			
t_h	Hold time	LS533	10↓			0↑			ns
		LS534	0↑			0↑			
T_A	Operating free air temperature		-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18mA			-1.5			-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			-0.4			-0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			20			20	µA
I_I	Maximum input current	V_{CC} = MAX	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 12mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24mA					0.35	0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OH} = -1mA	2.4	3.4					V
			I_{OH} = -2.6mA				2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4V						-20	µA
I_{OZH}			V_O = 2.7V			20			20	µA
I_{OS}	Output short-circuit current *	V_{CC} = MAX		-30		-130	-30		-130	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	LS533		36	48		36	48	mA
			LS534		27	48		27	48	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	LS533 MIN	LS533 TYP	LS533 MAX	LS534 MIN	LS534 TYP	LS534 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 45pF R_L = 667Ω				35	50		MHz
t_{PLH}	Data to Output delay			17	25				ns
t_{PHL}				12	25				ns
t_{PLH}	Clock/Enable to output delay			20	35		19	30	ns
t_{PHL}				18	35		15	30	ns
t_{PZL}	Output Enable delay			25	36		21	30	ns
t_{PZH}				17	30		20	30	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		18	29		18	29	ns
t_{PHZ}				16	24		16	24	ns

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Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Off-state output voltage 5.5V
Storage temperature .... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of Clock/Gate	High	15			15			ns
		Low	15			15			
t_{su}	Set up time	S533	0↓			0↓			ns
		S534	5↑			5↑			
t_h	Hold time	S533	10↓			0↑			ns
		S534	5↑			5↑			
T_A	Operating free air temperature		–55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN,	I_I = –18mA			–1.2			–1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5V			–0.25			–0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V			50			50	μA
I_I	Maximum input current	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 20mA			0.5			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = –2mA	2.4	3.4					V
			I_{OH} = –6.5mA				2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			–50			–50	μA
I_{OZH}			V_O = 2.4V			50			50	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX		–40		–100	–40		–100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	S533		105	160		105	160	mA
			S534		90	140		90	140	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	S533 MIN	S533 TYP	S533 MAX	S534 MIN	S534 TYP	S534 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 280Ω				75	100		MHz
t_{PLH}	Data to Output delay			9	18				ns
t_{PHL}				5	16				ns
t_{PLH}	Clock/Enable to output delay			12	22		11	20	ns
t_{PHL}				7	20		8	18	ns
t_{PZL}	Output Enable delay			11	20		11	20	ns
t_{PZH}				8	17		8	17	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 280Ω		8	16		7	16	ns
t_{PHZ}				6	13		5	13	ns

Octal Latches, Octal Registers With 32mA Outputs

SN74S531 SN74S532

Features/Benefits

- 32mA I_{OL}
- 3-state outputs drive bus lines
- 20-pin SKINNYDIP® saves space
- 8 bits matches byte boundaries
- Hysteresis improves noise margin
- Low current PNP inputs reduce loading
- Ideal for microprocessor interface
- Pin-compatible with SN74S373/4 — can be direct replacement when high drive capability is required

Description

In addition to the standard S and LS latches and registers, Monolithic Memories provides increased output sink current (I_{OL}) from the standard Schottky I_{OL} of 20 mA to an improved 32 mA.

The higher I_{OL} is intended for upgrading systems which presently satisfy 32 mA requirements with SN54/74365, 366, 367, 368, hex buffers.

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN74S531	N,J	com	Non-invert	Latch	S
SN74S532	N,J	com		Register	

The latch passes eight (octal) bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight (octal) bits of input data and passes it to the output on the "rising edge" of the clock.

The three-state outputs are active when $\overline{OE}$ is low, and high-impedance when OE is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the octal devices are packaged in the popular 20-pin SKINNYDIP®.

Function Tables

531 Octal Latch

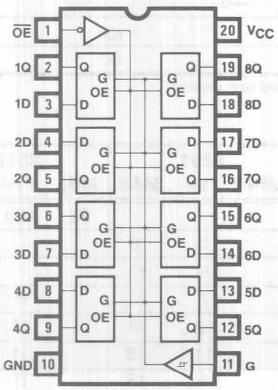
$\overline{OE}$	G	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

532 Octal Register

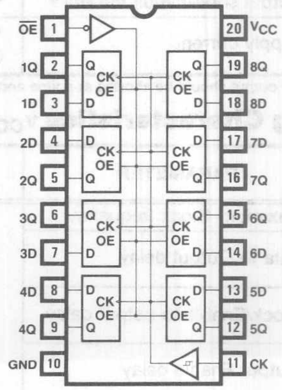
$\overline{OE}$	CK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

Logic Symbols

531 Octal Latch



532 Octal Register



Absolute Maximum Ratings

Supply Voltage, VCC 7V
Input Voltage 5.5V
Off-state output voltage 5.5V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free air temperature		0		75	°C
t_w	Width of Clock/Enable	High	6	6		ns
		Low	7.3	7.3		
t_{su}	Setup time	S531	0↓	0↓		ns
		S532	5↑	5↑		
t_h	Hold time	S531	10↓	10↓		ns
		S532	2↑	2↑		

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V			50	μA
I_I	Maximum input current	V_{CC} = MAX,	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 32mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −6.5mA	2.4	3.1		V
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			−50	μA
I_{OZH}			V_O = 2.4V			50	μA
I_{OS}	Output short-circuit current*	V_{CC} = MAX,		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	S531		105	160	mA
			S532		90	140	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	S531 MIN	S531 TYP	S531 MAX	S532 MIN	S532 TYP	S532 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 280Ω				75	100		MHz
t_{PLH}	Data to Output delay			5	9				ns
t_{PHL}				9	13				ns
t_{PLH}	Clock/Enable to output delay			7	14		8	15	ns
t_{PHL}				12	18		11	17	ns
t_{PZL}	Output Enable delay			11	18		11	18	ns
t_{PZH}				8	15		8	15	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 280Ω		8	12		7	12	ns
t_{PHZ}				6	9		5	9	ns

Octal Latches, Octal Registers With Inverting, 32 mA Outputs

SN74S535 SN74S536

Features/Benefits

- Inverting outputs
- 32mA I_{OL}
- 3-state outputs drive bus lines
- 20-pin SKINNYDIP® saves space
- 8 bits matches byte boundaries
- Hysteresis improves noise margin
- Low current PNP inputs reduce loading
- Ideal for microprocessor interface
- Pin-compatible with SN74S533/4 — can be direct replacement when hi-drive capability is required

Description

In addition to the standard S and LS latches and registers, Monolithic Memories provides increased output sink current (I_{OL}) from the standard Schottky I_{OL} of 20 mA to an improved 32 mA, also inverting outputs instead of the standard non-inverting outputs.

The higher I_{OL} is intended for upgrading systems which presently satisfy 32 mA requirements with SN54/74365, 366, 367, 368, hex buffers. The inverting outputs are intended for bus applications that require inversion as in interfacing the Am2901A 4-Bit Slice to an active low bus.

The latch passes eight (octal) bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight (octal) bits of input data and passes it to the output on the "rising edge" of the clock.

The three-state outputs are active when $\overline{OE}$ is low, and high-impedance when OE is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the octal devices are packaged in the popular 20-pin SKINNYDIP®.

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN74S535	N,J	com	Invert	Latch	S
SN74S536	N,J	com		Register	

Function Tables

535 Octal Latch (Inverting)

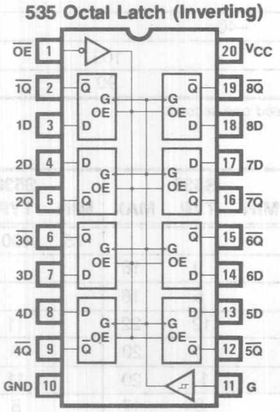
$\overline{OE}$	G	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

536 Octal Register (Inverting)

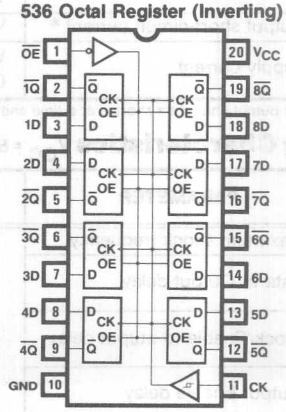
$\overline{OE}$	CK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	Q_0
H	X	X	Z

Logic Symbols

535 Octal Latch (Inverting)



536 Octal Register (Inverting)



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Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Off-state output voltage 5.5V
Storage temperature .... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free air temperature		0		75	°C
t_w	Width of Clock/Enable	High	6	6		ns
		Low	7.3	7.3		
t_{su}	Setup time	S535	0↓	0↓		ns
		S536	5↑	5↑		
t_h	Hold time	S535	10↓	10↓		ns
		S536	5↑	2↑		

Electrical Maximum Ratings Over Operating Conditions

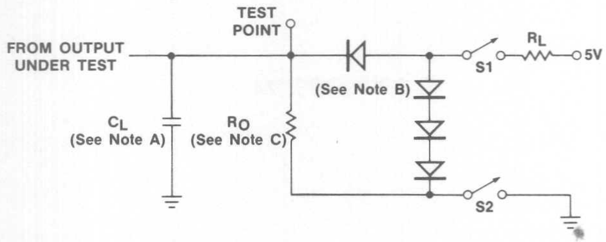
SYMBOL	PARAMETER	TEST CONDITIONS		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 32mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MAX V_{IL} = 0.8V V_{IH} = 2V	I_{OH} = −6.5mA	2.4	3.1		V
I_{OZL}	Off-state output current	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	V_O = 0.5V			−50	μA
I_{OZH}			V_O = 2.4V			50	μA
I_{OS}	Output short-circuit current *	V_{CC}		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX Outputs open	S535		105	160	mA
			S536		90	140	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

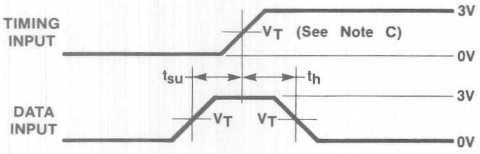
Switching Charcteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	S535 MIN	S535 TYP	S535 MAX	S536 MIN	S536 TYP	S536 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 280Ω				75	100		MHz
t_{PLH}	Data to Output delay			9	18				ns
t_{PHL}				5	16				ns
t_{PLH}	Clock/Enable to output delay			12	22		11	20	ns
t_{PHL}				7	20		8	18	ns
t_{PZL}	Output Enable delay			11	20		11	20	ns
t_{PZH}				8	17		8	17	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 280Ω		8	16		7	16	ns
t_{PHZ}				6	13		5	13	ns

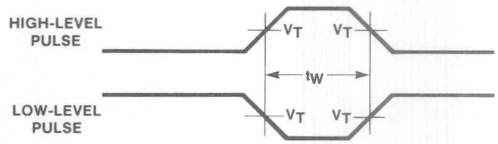
Test Load



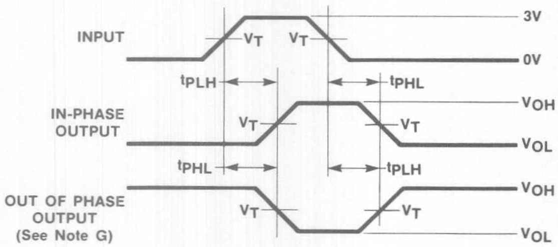
Test Waveforms



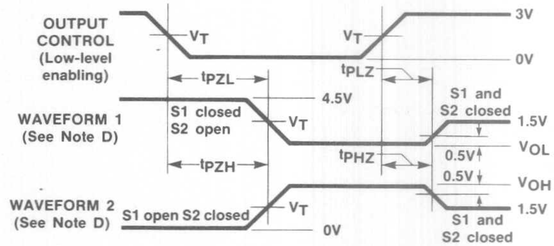
SETUP AND HOLD



PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE

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NOTES: A. C_L includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

C. For Series 54/74S, R_O = 1K, V_T = 1.5V.
For Series 54/74LS, R_O = 5K, V_T = 1.3V excepting 54/74LS310, 340, 341, 344.
For Series 54/74LS310, 340, 341, 344 R_O = 5K, $V_T = V_{T+}$ = 1.7V for low to high input transition.
For Series 54/74LS310, 340, 341, 344 R_O = 5K, $V_T = V_{T-}$ = 0.9V for high to low input transition.

D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

F. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, Z_{out} = 50Ω and:
For Series 54/74S, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.
For Series 54/74LS and PALs, $t_R \leq 15$ns, $t_F \leq 6$ ns.

G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

Leadless

Features

- 20-pin hermetically sealed three layer base with a gold lid and gold-tin brazed seal
- JEDEC outline leadless type B
- 50 MIL center spacing
- 75 MIL maximum package thickness
- MIL-STD-883 Level B
- Eutectic die attach

Applications

- Heavy military demand
- Automotive
- Telecommunications
- Computer mainframe
- Increased hybrid market demand
- VLSI technologies
- Data processing systems

Benefits

- Uses less space
- Weight reduction
- Reduces system cost
- Reduced lead resistance, capacitance and inductance, thereby, enhancing parameter performance
- Improved thermal resistance

Programmable Array Logic

PART NUMBER	DESCRIPTION
PAL10H8ML883B	Octal 10 Input And-Or Gate Array
PAL12H6ML883B	Hex 12 Input And-Or Gate Array
PAL14H4ML883B	Quad 14 Input And-Or Gate Array
PAL16H2ML883B	Dual 16 Input And-Or Gate Array
PAL16C1ML883B	16 Input And-Or/And-Or-Invert Gate Array
PAL10L8ML883B	Octal 10 Input And-Or-Invert Gate Array
PAL12L6ML883B	Hex 12 Input And-Or-Invert Gate Array
PAL14L4ML883B	Quad 14 Input And-Or-Invert Gate Array
PAL16L2ML883B	Dual 16 Input And-Or-Invert Gate Array
PAL16L8ML883B	Octal 16 Input And-Or-Invert Gate Array
PAL16R8ML883B	Octal 16 Input Registered And-Or Gate Array
PAL16R6ML883B	Hex 16 Input Registered And-Or Gate Array
PAL16R4ML883B	Quad 16 Input Registered And-Or Gate Array

Octal Interface

PART NUMBER[1]	FUNCTION	POLARITY	POWER
SN54LS240L883B	Octal Buffer	Invert	LS
SN54LS241L883B	Octal Buffer	Non-Invert	LS
SN54LS244L883B	Octal Buffer	Non-Invert	LS
SN54S240L883B	Octal Buffer	Invert	S
SN54S241L883B	Octal Buffer	Non-Invert	S
SN54S244L883B	Octal Buffer	Non-Invert	S
SN54LS373L883B	Octal Latch	Non-Invert	LS
SN54LS374L883B	Octal Register	Non-Invert	LS
SN54S373L883B	Octal Latch	Non-Invert	S
SN54S374L883B	Octal Register	Non-Invert	S
SN54LS245L883B	Transceiver	Non-Invert	LS
SN54LS273L883B	Octal Register with clear		LS
SN54LS377L883B	Octal Register with clock enable		LS

Bipolar PROM

PART NUMBER[2]	ORGANIZATION
5308-1L883B	256x8 OC
5309-1L883B	256x8 TS

NOTES:
1. 54 = Military Temperature Range of -55 to +125°C
2. 5 = Military Temperature Range of -55 to +125°C

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Die

Introduction

The Monolithic Memories Incorporated "Classic Die" program is a quality oriented comprehensive approach designed to serve a constantly expanding, quality demanding hybrid market.

We believe that quality and reliability are the natural results of our heavy emphasis in reliability at the design, in-product/process development and manufacturing stages.

The total quality concept, enhanced by our "Classic Test" tight test die probe strategy combine to produce a selected die with higher end user yields. We guarantee performance to the data sheet parameters limits and conditions specified for each fully packaged product, to the percent tested under Electrical guaranteed.

Testing

All die are 100% probed at 25°C to a temperature correlated test program. Temperature simulation is accomplished via V_{CC} variation and test limit guardband for DC parameters and functional to the following temperature ranges:

- Commercial = 0° to 75°C, i.e. 67401X
- Military = 55° to +125°C, i.e. 57401X

Packaged Product Electrical Guarantees:

"Classic Test" die probe at 25°C guarantees the following packaged product yields, when tested to the electrical parameters and conditions listed in the Monolithic Memories LSI Data book.

- 57401, LTPD 10 excluding assembly defects.
- 57402, LTPD 10 excluding assembly defects.
- 57558, LTPD 10 excluding assembly defects.

AC parameters are guaranteed by design and periodical statistical sampling in accordance with MIL-M-38510.

Available Part Types

PART NUMBER	DESCRIPTION
5/67558X	8x8 Multiplier
5/67401X	64x4 FIFO
5/67402X	64x5 FIFO

Visual Inspection

- 100% inspection to 2010B
- Silox Inspection
- X150 High Magnification
- Wafer saw completely through
- No ink on die

Physical Characteristics

- All die are passivated
- Aluminum metallization
- May be assembled by industry standard die attach, lead bond and sealing techniques for LSI Bi-Polar products.
- 20 mils thick typically (with no gold backing)

Quality Control: Lot Acceptance

2010B Visual Inspection

- .65 AQL for Commercial products lots
- .4 AQL for Military products lots
- Non-standard AQL's are negotiable.

NOTE: The visual criteria is guaranteed within the periphery of the bond pads unless otherwise negotiated.

Traceability

When specifically requested . . .

- Military to Fab production run
- Commercial to QA lot acceptance

Packaging

- Waffle pack; sized for the specific product.
- One waffle pack per plastic bag
- Vacuum seal with dessicant
- Moisture indicator
- As a minimum, each waffle pack is labeled with:
  - Monolithic Memories' part number
  - Date indicating lot acceptance

1165 East Arques Avenue, Sunnyvale, CA 94086 Tel: (408) 739-3535 TWX: 910-339-9229

Monolithic Memories

Handling

No additional cleaning is required when handled under the specified controlled environments delineated by MIL-STD-882 Method 2010.

Other Capabilities

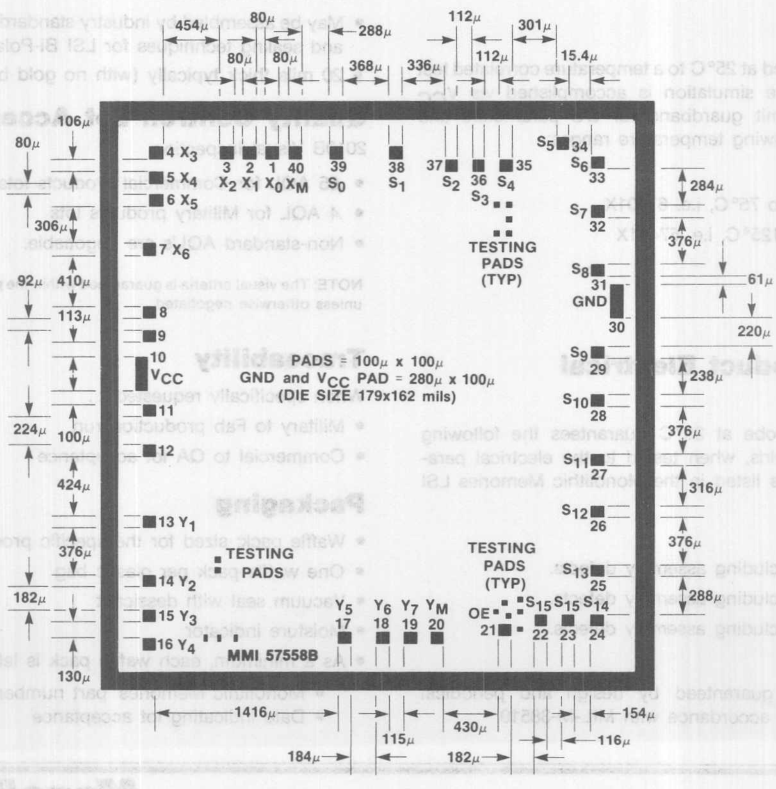
When required, the following options are available at additional cost, contact the factory.

- SEM, Method 2018
- Die lot qualification by sample
- Wafer lot qualification
- Fully documented custom flows
- Programming

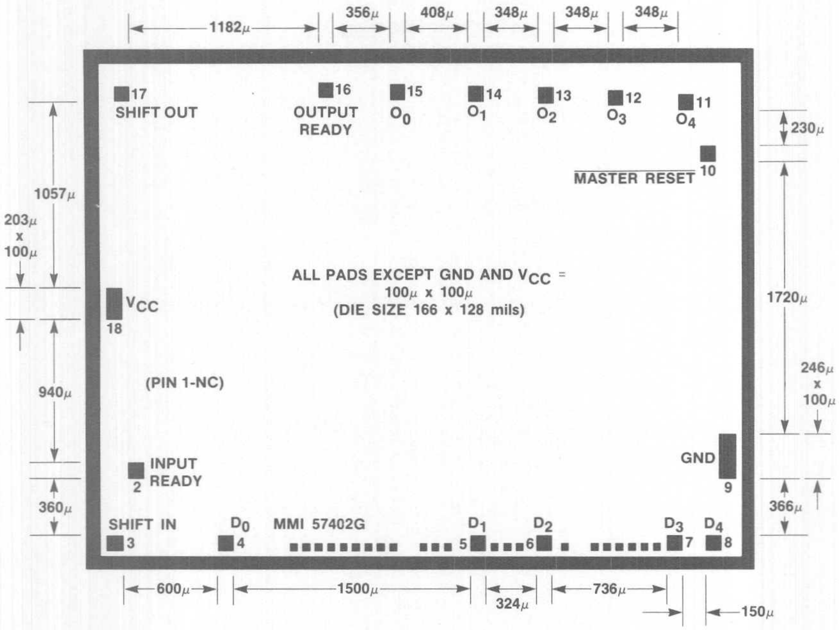
Ordering Information

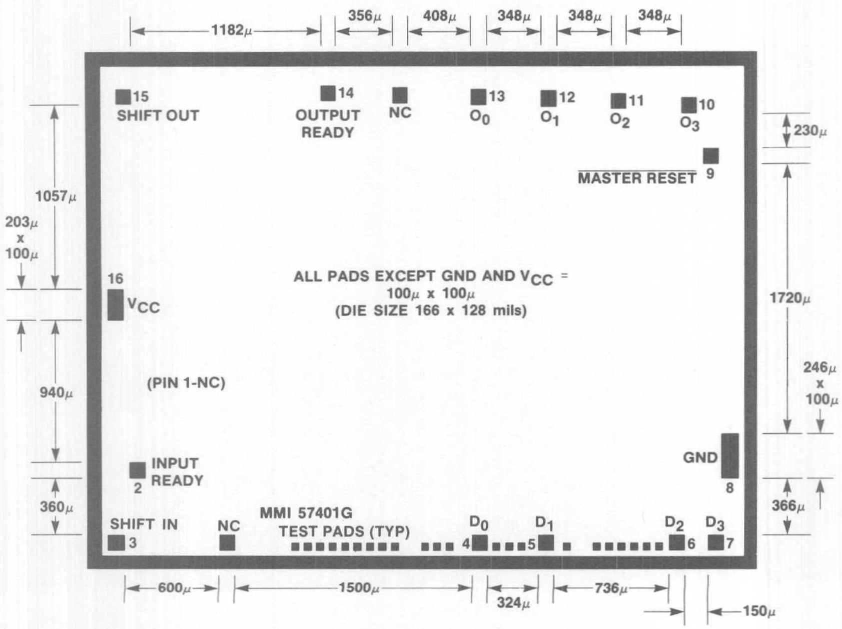
- Monolithic Memories part number plus "X" in lieu of package letter designation
- Please submit all applicable source control drawings, or documents for review.
- Specify all non-standard requirements.

Configuration



Configurations





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Setup Time

Setup time, t_{su}

The time interval between the application of a signal that is maintained at a specified input terminal and a consecutive active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time between two events and may be insufficient to accomplish the setup. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the logic element is guaranteed.

Voltage

High-level input voltage, V_{IH}

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least positive value of high-level voltage for which operation of the logic element within specification limits is guaranteed.

High-level output voltage, V_{OH}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.

Input clamp voltage, V_{IC}

An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

Low-level input voltage, V_{IL}

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

Low-level output voltage, V_{OL}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.

Negative-going threshold voltage, V_{T}

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

Positive-going threshold voltage, V_{T+}

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

Truth Table Explanations

H	=	high level (steady-state)
L	=	low level (steady-state)
↑	=	transition from low to high level
↓	=	transition from high to low level
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a..h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output.

Clock Frequency

Maximum clock frequency, f_{max}

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

Current

High-level input current, I_{IH}

The current into * an input when a high-level voltage is applied to that input.

High-level output current, I_{OH}

The current into * an output with input conditions applied that according to the product specification will establish a high level at the output.

High-level output current, I_{CEX}

The high-level leakage current of an open collector output.

Low-level input current, I_{IL}

The current into * an input when a low-level voltage is applied to that input.

Low-level output current, I_{OL}

The current into * an output with input conditions applied that according to the product specification will establish a low level at the output.

Off-state (high-impedance-state) output current (of a three-state output), I_{OZ}

The current into * an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

Short-circuit output current, I_{OS}

The current into * an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

Supply current, I_{CC}

The current into * the V_{CC} supply terminal of an integrated circuit.

*Current out of a terminal is given as a negative value.

Hold Time

Hold time, t_h

The interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES:
1. The hold time is the actual time between two events and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of data and the active transition) for which correct operation of the logic element is guaranteed.

Output Enable and Disable Time

Output enable time (of a three-state output) to high level, t_{PZH} (or low level, t_{PZL})

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high (or low) level.

Output enable time (of a three-state output) to high or low level, t_{PZX}

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

Output disable time (of a three-state output) from high level, t_{PHZ} (or low level, t_{PLZ})

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high (or low) level to a high-impedance (off) state.

Output disable time (of a three-state output) from high or low level, t_{PXZ}

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

t_{EA} is the output enable access time of memory devices.
t_{ER} is the output disable (enable recovery) time of memory devices.

Propagation Time

Propagation delay time, t_{PD}

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level.

Propagation delay time, low-to-high-level output, t_{PLH}

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

Propagation delay time, high-to-low-level output, t_{PHL}

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{AA} is the address (to output) access time of memory devices.

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Pulse Width

Pulse width, t_W

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

Programming Input Formats

Monolithic Memories can program your ROM or PROM from input data in any of several types: truth table, punched cards, paper tape or preprogrammed ROM or PROM. However, the preferred input data for PROMs is paper tape and for ROMs punched cards.

Truth Table Inputs

Devices are programmed at our facility from Monolithic Memories truth table forms (available on request). For customers desiring to make their own forms, examples are shown below:

4-BIT OUTPUT

		OUTPUTS			
WORD NUMBER	PIN	10	11	12	13
		O_4	O_3	O_2	O_1
0		H	H	H	L
1		L	H	L	H
⋮					
255		L	H	H	H

8-BIT OUTPUT

		OUTPUTS							
WORD NUMBER	PIN	17	16	15	14	13	11	10	9
		O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0		H	H	H	L	H	L	H	H
1		L	H	L	H	L	H	L	H
⋮									
511		L	H	H	H	H	H	H	L

NOTE: A high voltage on the data out lines is signified by an "H." A low voltage on the data out lines is signified by an "L." The word number assumes positive logic on the address pins, so for example, word 1023 = HHHHHHHHHH.

Paper Tape Format Inputs

Truth tables can also be sent Monolithic Memories in an ASCII tape in either a 7 or 8 level format. Send information air mail or TWX 910-339-9224. The tape reading equipment at Monolithic Memories only recognizes ASCII characters S, B, H, L, F and E interprets them respectively as Start, Begin a word, High data, Low data, Finish a word, and End of tape. All other characters such as carriage returns, line feeds, etc. are ignored so that comments and spaces may be sent in the data field to improve readability. Comments, however, should not use the characters S, B, H, L, F, E. Word addresses must begin with zero and count sequentially to word 31, 255, 511 or 1023 respectively.

In order to assist the machine operator in determining where the heading information stops and the data field begins, 25 bell characters or rubout characters should precede the start of the truth table. Any type of 8 level paper tape (mylar, fanfold, etc.) is acceptable. Channel 1 is the most significant bit and channel 8 (parity) is ignored. Sprocket holes are located between channels 3 and 4. Note that the order of the outputs between characters B and F is O_4, O_3, O_2, O_1, not O_1, O_2, O_3, O_4.

A typical list of characters and their machine interpretations is shown below:

4-BIT OUTPUT

START OF TAPE — END OF TAPE
BEGIN DATA FIELD
DATA FIELD (H = HIGH VOLTAGE, L = LOW)
FINISHED DATA FIELD

SBH H L H F   BHHHHF   BHLLHF -   etc. BHLLLFE
O_4 O_3 O_2 O_1
WORD 0   WORD 1   WORD 2   WORD 255, 511 or 1023

8-BIT OUTPUT

START OF TAPE — END OF TAPE
BEGIN DATA FIELD
DATA FIELD (H = HIGH VOLTAGE, L = LOW)
FINISHED DATA FIELD

SBHHHHLLLHHF   BHLHLHHLLF   BHLHLHLLF - etc. BHHHHLLLLFE
O_8 O_1
WORD 0   WORD 1   WORD 2   WORD 31, 255, 511 or 1023

The required heading information at the beginning of the tape is as follows:

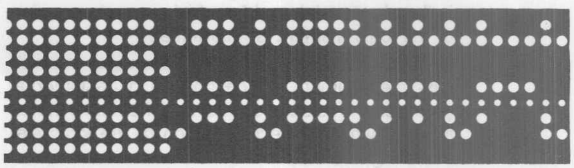
CUSTOMER'S NAME AND PHONE ______	TRUTH TABLE NUMBER ______
CUSTOMER'S TWX NUMBER ______	NUMBER OF TRUTH TABLES ______
PURCHASE ORDER NUMBER ______	TOTAL NUMBER OF PARTS ______
MONOLITHIC MEMORIES' PART NUMBER ______	NUMBER OF PARTS OF EACH TRUTH TABLE ______
CUSTOMER SYMBOLIZED PART NUMBER ______	25 BELL OR RUBOUT CHARACTERS ______

An example is shown below for a 256 x 4 PROM (6300)

SCOTT ELECTRONICS 408 426-6134
TWX 911-338-9225
PO142
6300
0431
12
1
3
3

SBLLLHF BLLLLF BLHLHF BLHHHF BLLHHF BHHHHF BLLLHF BLHLHF BLLLLF
BLLLLF BLHLHF BLLHHF BHHHLF BHHLLF BLHHHF BHHLLF BLLHHF BLHLHF

8 level
TWX



ROM Programming Punched Card

ROMs can be programmed using several input methods. These are truth table, punched cards in the format shown below, paper tape in the same format as cards, and paper tape in the ASCII BHLF format of the equivalent PROM.

Punched Card or Tape Input

First card or line (80 columns max.): enter Company Name, Part Number, Data, Number of "L's" in Pattern.

(Free Form Entry: no commas; Paper Tape Format: terminate each line with carriage return and linefeed).

Hexadecimal Format

In this format the heading required is identical to the BHLF format but the data is different. Instead of an "S," the hexadecimal data begins with the SOH character (control A). The data is then represented by the hexadecimal character (0-9 and A-F) which represents the output data of address 0, followed by a space. Next comes the output data of address 1 followed by a space, etc. The character ETX (control C) is used to end the data. Carriage return and the line feed may be included to format the data when the tape is printed.

CARD 1

COMPANY NAME CX 1816—2052 7—12—70 L = 796

2nd Card Or Line thru Last (80 Columns Max.)

ENTER WORD ADDRESS OF FIRST DATA FIELD IN COLUMNS 1 THRU 5

Enter First Data Field	(O_{10}—O_1)	in Columns 8 thru 17
Enter Second Data Field	(O_{10}—O_1)	in Columns 19 thru 28
Enter Third Data Field	(O_{10}—O_1)	in Columns 30 thru 39
Enter Fourth Data Field	(O_{10}—O_1)	in Columns 41 thru 50
Enter Fifth Data Field	(O_{10}—O_1)	in Columns 52 thru 61
Enter Sixth Data Field	(O_{10}—O_1)	in Columns 63 thru 72

CARD 2

00000 LHHHHLLHHH LHHHHHHHHH LLLLLLLLLH LLHHHHHHLL HLLLHHHHHL LHLLLLLLLL

WORD — ADDRESS OF — O_1

NOTE: Output 1 (O_1) is always in cols. 17,28,39,50,61,72

CARD 3

00006 LHLLLLLLLL HLHHHHHHHH LHLHHLLHHL HLHHHHLLLL LLLLHHHLHL HLHHHHHHLH

LAST CARD

01020 HLLLLLLLL HHLHHHHHLL LHLHLHLHLH LLHLHLLHHH

NOTES:

1. Leading edge zeroes in the word number may be eliminated. Columns 73 thru 80 are for comments.
2. Regardless of the number of outputs which a particular ROM has, the data for a specific output always goes in a specific column.

Output 1 (01)	Columns 17, 28, 39, 50, 61, 72
Output 2 (02)	Columns 16, 27, 38, 49, 60, 71
Output 3 (03)	Columns 15, 26, 37, 48, 59, 70
Output 4 (04)	Columns 14, 25, 36, 47, 58, 69
Output 5 (05)	Columns 13, 24, 35, 46, 57, 68
Output 6 (06)	Columns 12, 23, 34, 45, 56, 67
Output 7 (07)	Columns 11, 22, 33, 44, 55, 66
Output 8 (08)	Columns 10, 21, 32, 43, 54, 65
Output 9 (09)	Columns 9, 20, 31, 42, 53, 64
Output 10 (10)	Columns 8, 19, 30, 41, 52, 63

3. 0 and 1 may replace L and H, but the customer must define for MMI whether 0 = L or 0 = H.

Application Notes

- The PALTWX Brochure
- PAL Training Manual
- High level language for programmable array logic
- Medium speed multipliers trim cost, shrink band-width in speech transmission
- High speed Monolithic multipliers for real-time digital signal processing
- State-of-the-art in high speed arithmetic integrated circuits
- p/ROM card simplifies computer diagnosis
- Power switch ROMs and PROMs quickly
- An 8x8 multiplier and 8-bit microprocessor perform 16x16-bit multiplication
- A dedicated multiplier/divider speeds up multiplication and division for 8-bit microprocessors
- Real-time processing gains ground with fast digital multiplication
- Reduce random-logic complexity by using array of fuse-programmable circuits
- PAL engineering reference card
- Understanding FIFOs
- Programmable Array Logic leads to flexible application of 8-bit wide memories

Brochures

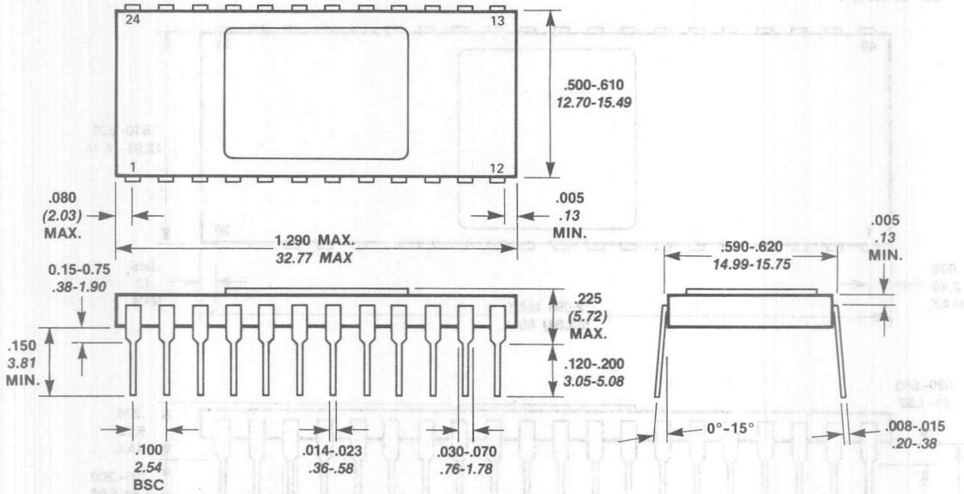
- Bipolar is our Business — company brochure
- PAL flyer
- LSI
- OEM price list
- Distributors cost list
- Product Assurance Manual
- Plastic Reliability Report
- Reliability Report
- Military Components

Available through the Advertising Department of Monolithic Memories.

D24 Side Brazed Ceramic DIP

θ_{JA} = 65° C/WATT

θ_{JC} = 30° C/WATT

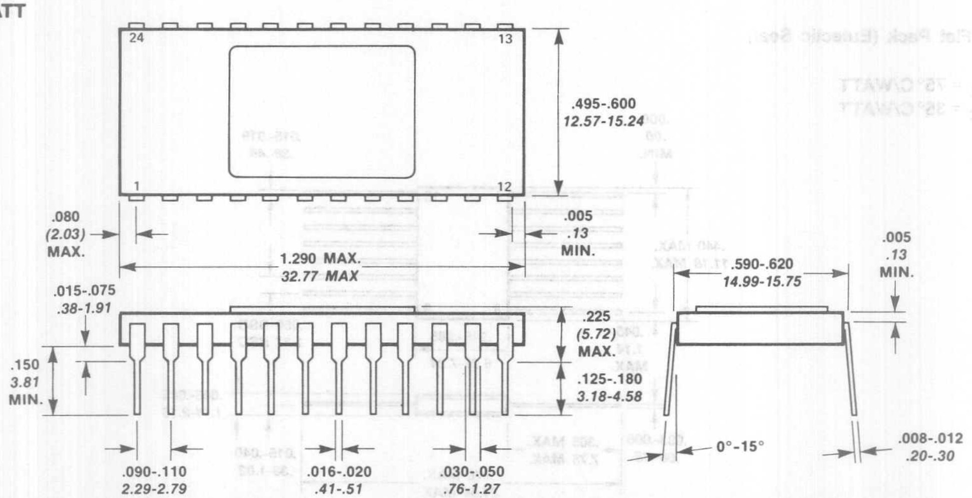


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

TD24 Side Brazed Ceramic DIP

θ_{JA} = 45° C/WATT

θ_{JC} = 15° C/WATT



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

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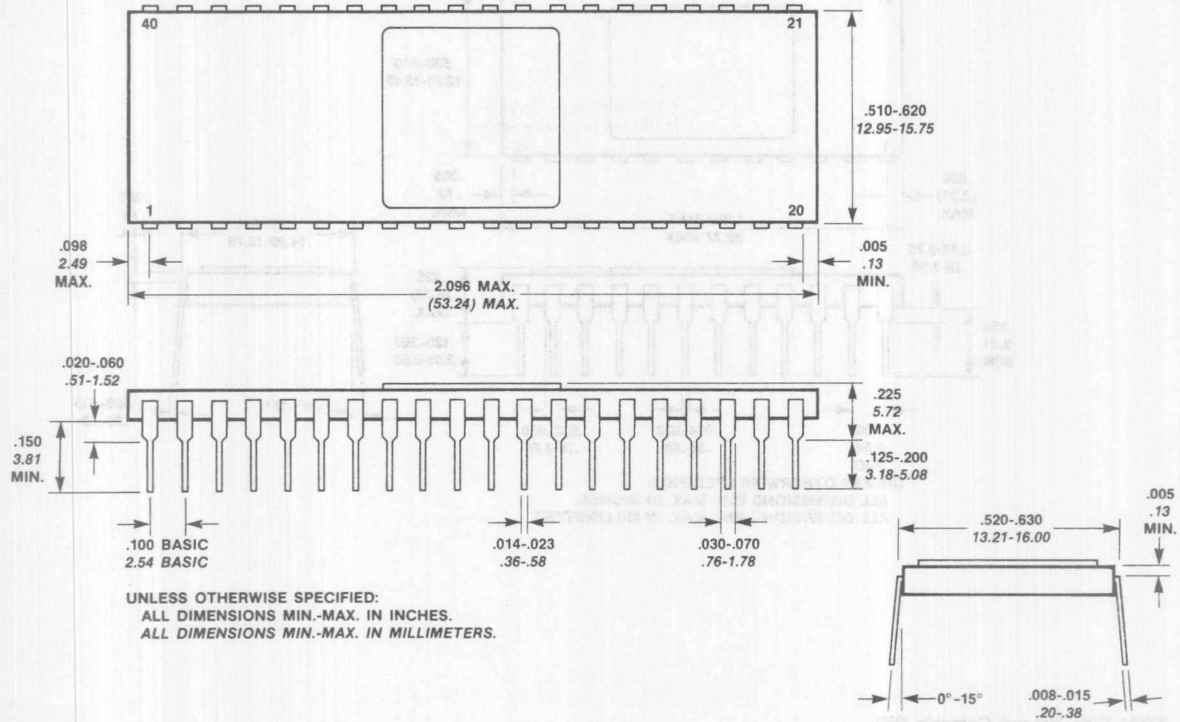
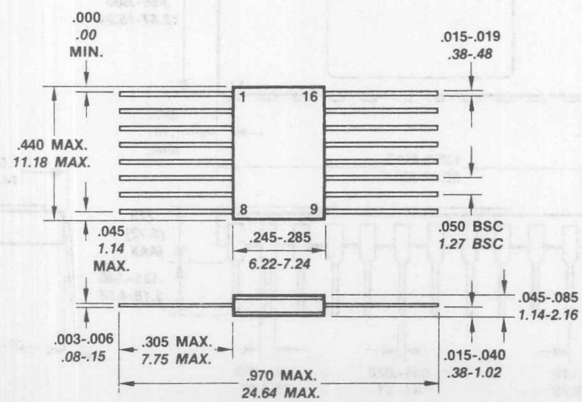
θ_{JA} = 60°C/WATT
θ_{JC} = 25°C/WATT



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

F16 Flat Pack (Eutectic Seal)

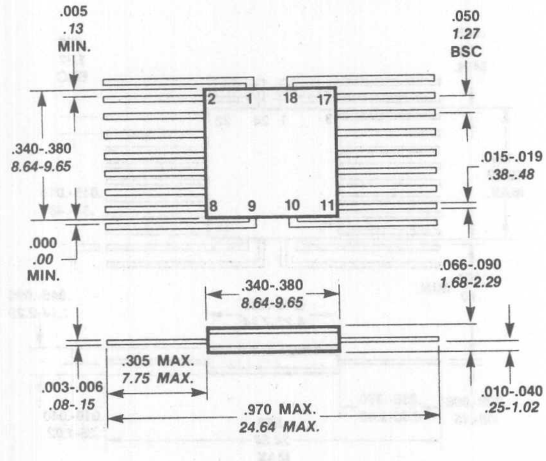
θ_{JA} = 75°C/WATT
θ_{JC} = 35°C/WATT



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

F18 Flat Pack (Eutectic Seal)

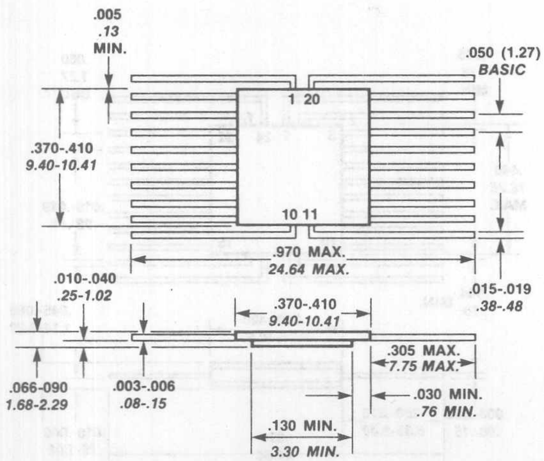
θ_{JA} = 75° C/WATT
θ_{JC} = 35° C/WATT



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX IN MILLIMETERS.

F20 Flat Pack (Eutectic Seal)

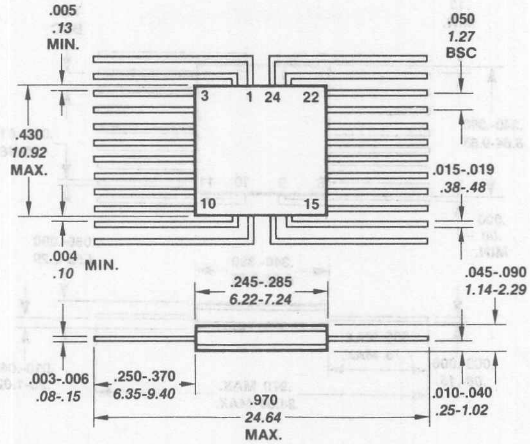
θ_{JA} = 75° C/WATT
θ_{JC} = 35° C/WATT



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

F24 Flat Pack (Eutectic Seal)

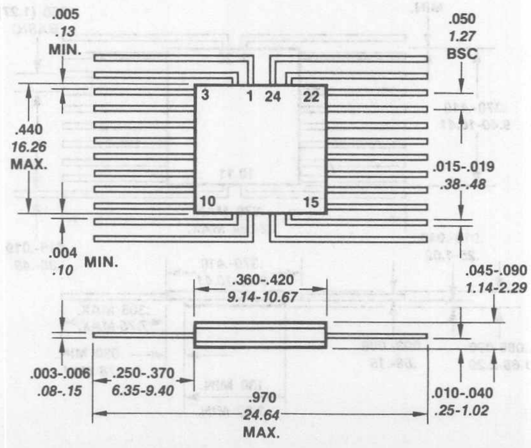
θ_{JA} = 75°C/WATT
θ_{JC} = 35°C/WATT



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS

F4-24 Flat Pack (Eutectic Seal)

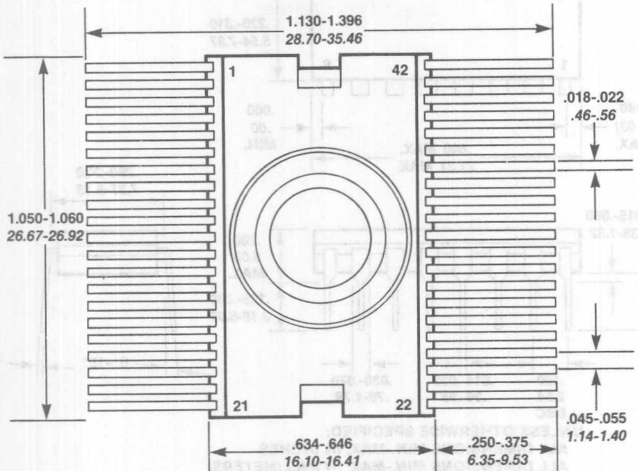
θ_{JA} = 75°C/WATT
θ_{JC} = 35°C/WATT

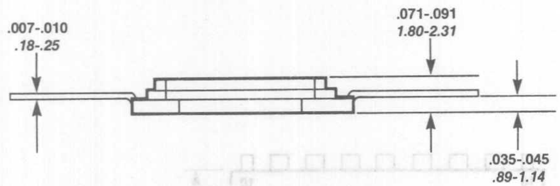


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS

F42 Flat Pack (Eutectic Seal)

θ_{JA} = 65° C/WATT
θ_{JC} = 30° C/WATT



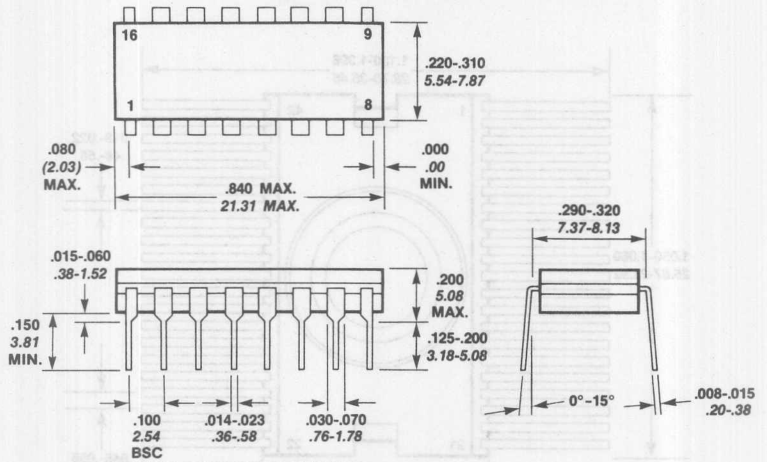


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS

15

J16 Ceramic DIP

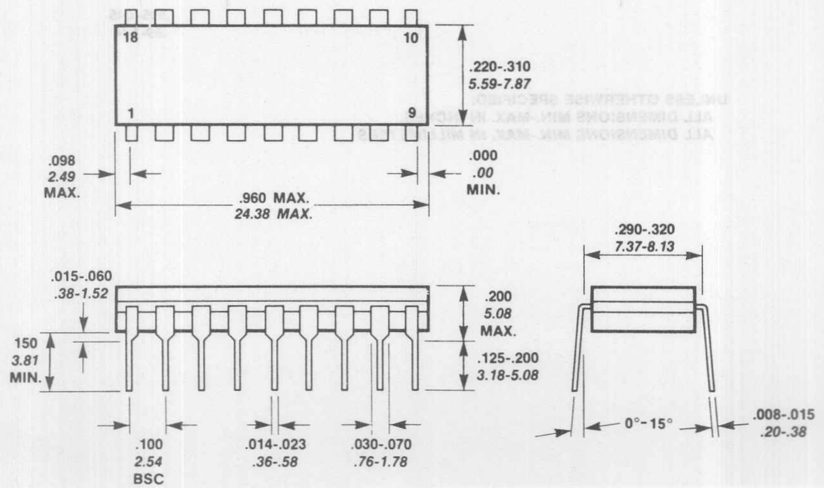
θ_{JA} = 75°C/WATT
θ_{JC} = 35°C/WATT



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

J18 Ceramic DIP

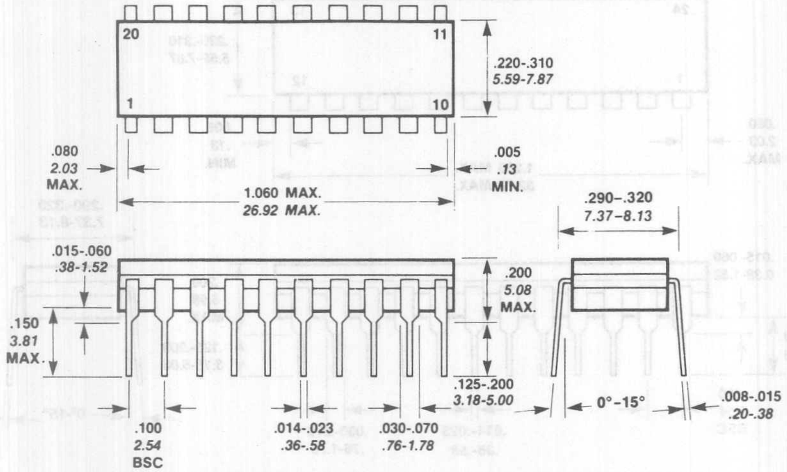
θ_{JA} = 75°C/WATT
θ_{JC} = 35°C/WATT



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

J20 Ceramic DIP

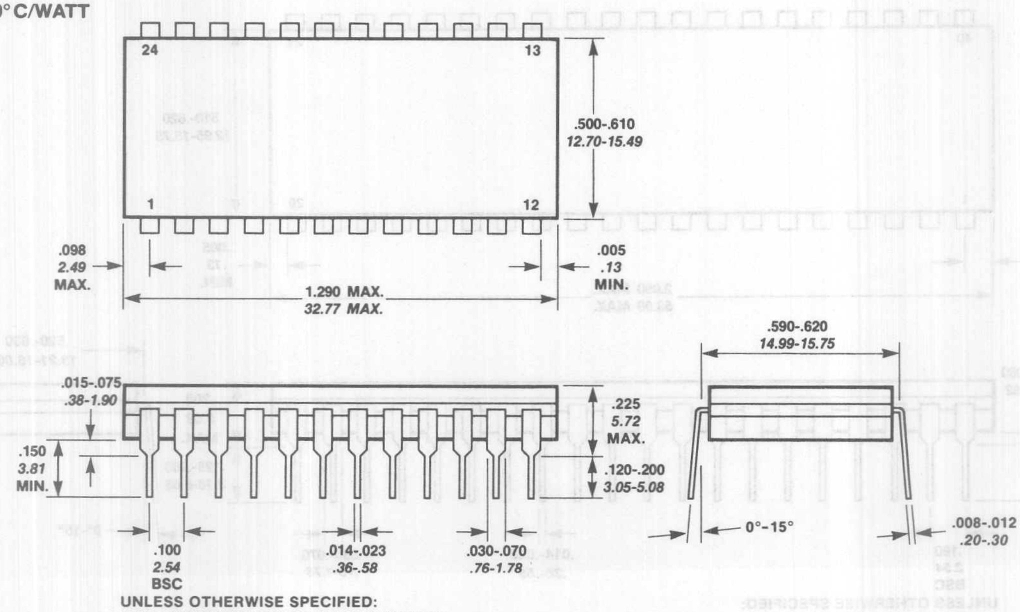
θ_{JA} = 75°C/WATT
θ_{JC} = 35°C/WATT



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

J24 Ceramic DIP

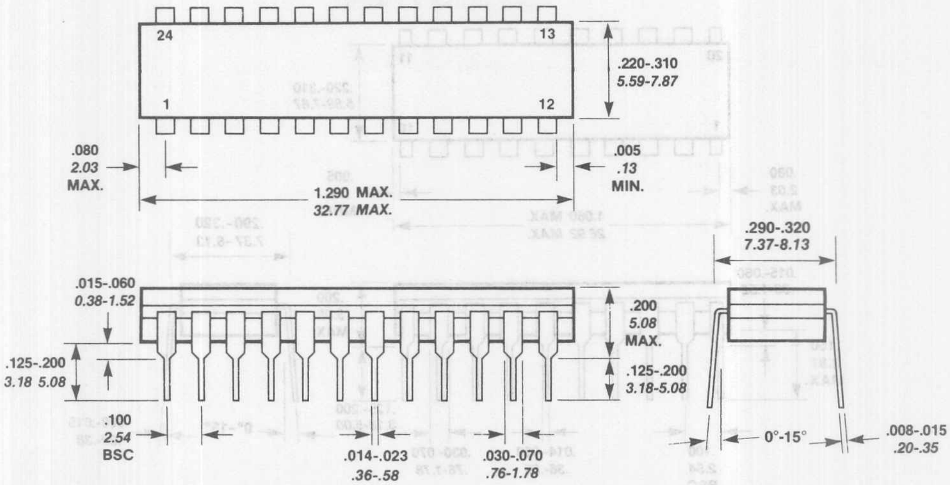
θ_{JA} = 65°C/WATT
θ_{JC} = 30°C/WATT



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS

J24S Ceramic SKINNYDIP™

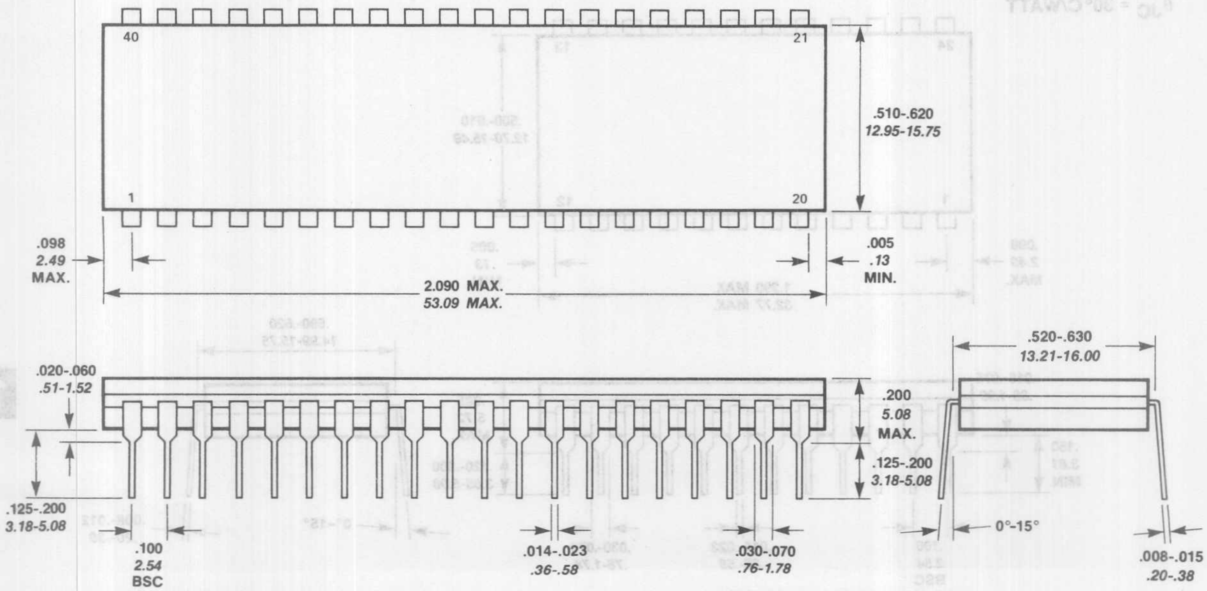
θ_{JA} = 75° C/WATT
θ_{JC} = 35° C/WATT



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS

J40 Ceramic DIP

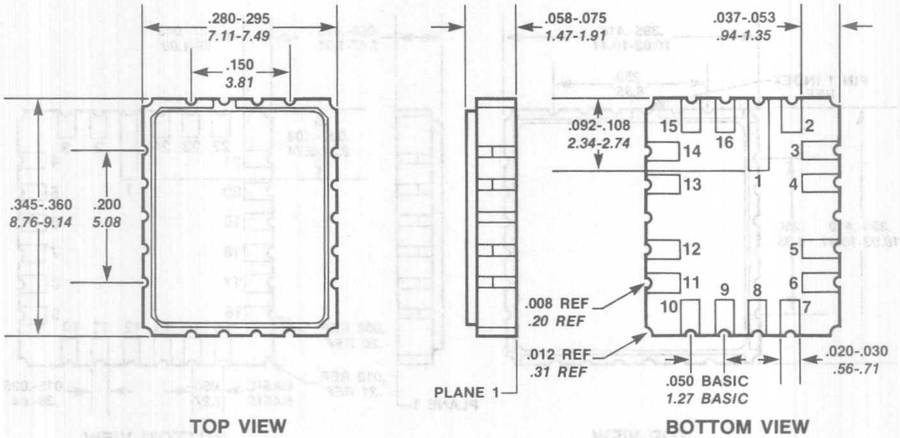
θ_{JA} = 60° C/WATT
θ_{JC} = 25° C/WATT



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS

L16 Leadless Chip Carrier

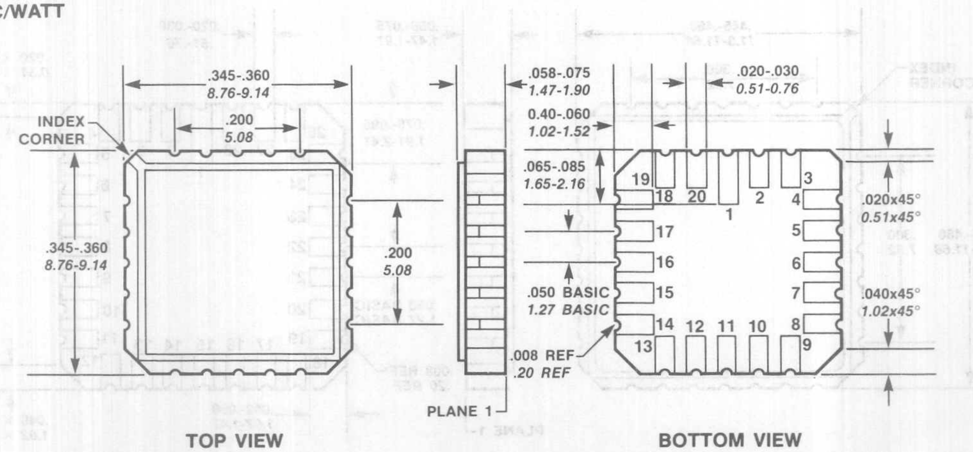
θ_{JA} - 63° C/WATT
θ_{JC} - 35° C/WATT



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
PLANE 1 IS THE PRIMARY HEAT RADIATING SURFACE

L20 Leadless Chip Carrier

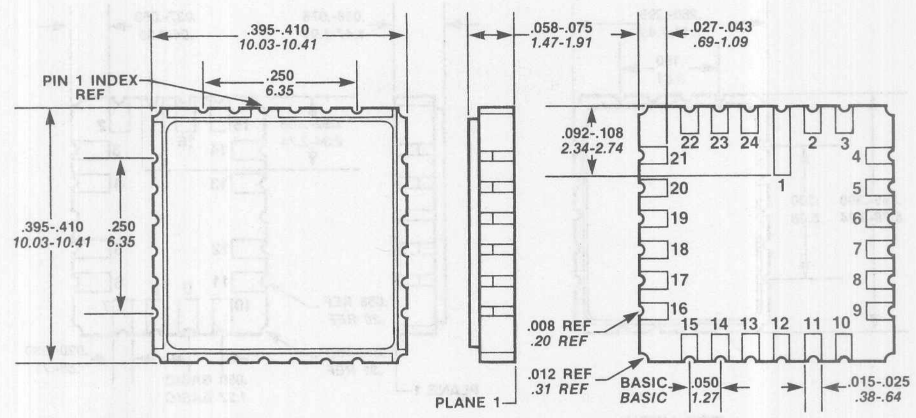
θ_{JA} - 63° C/WATT
θ_{JC} - 35° C/WATT



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
PLANE 1 IS THE PRIMARY HEAT RADIATING SURFACE

16

θ_{JA} - 63° C/WATT
θ_{JC} - 35° C/WATT

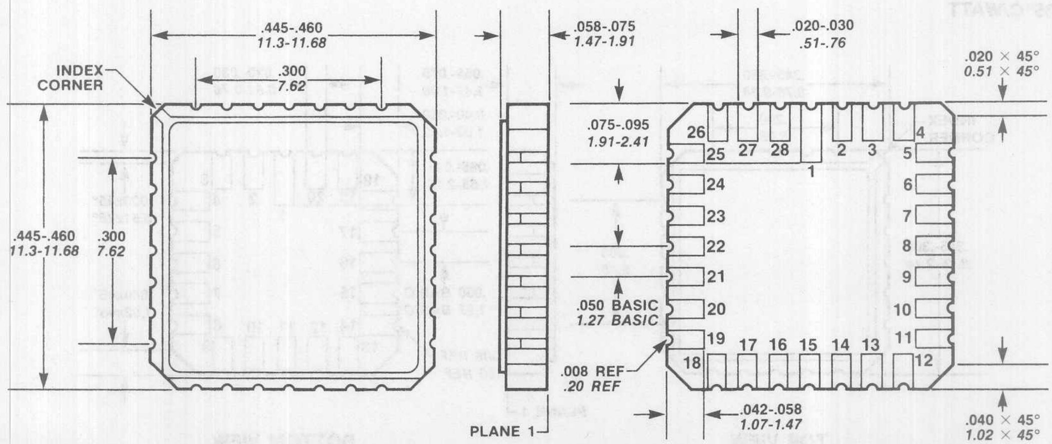


TOP VIEW BOTTOM VIEW

UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
PLANE 1 IS THE PRIMARY HEAT RADIATING SURFACE

L28 Leadless Chip Carrier

θ_{JA} - 63° C/WATT
θ_{JC} - 35° C/WATT

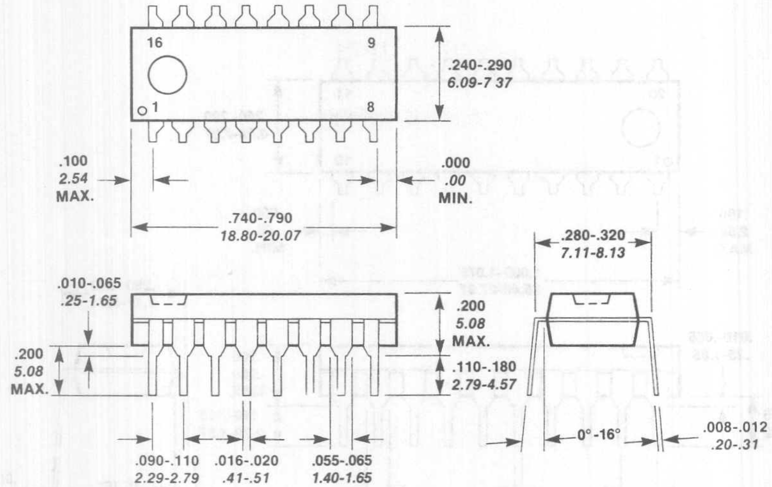


TOP VIEW BOTTOM VIEW

UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
PLANE 1 IS THE PRIMARY HEAT RADIATING SURFACE

N16 Plastic Kool DIP™

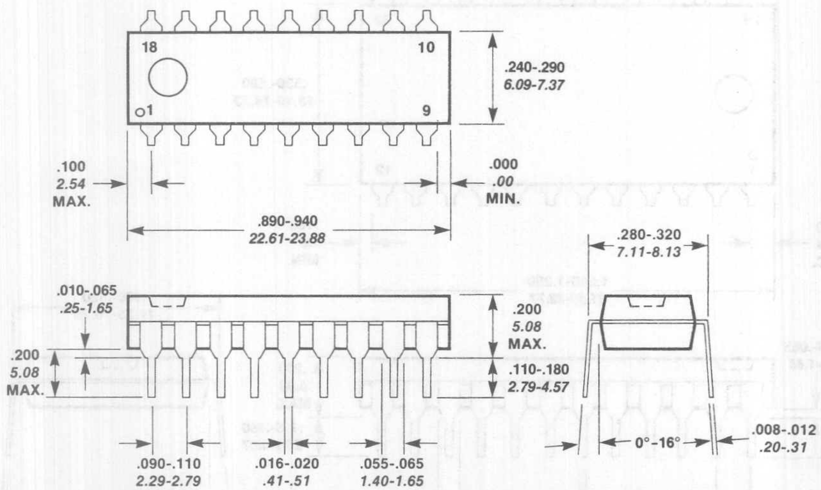
θ_{JA} = 75° C/WATT
θ_{JC} = 35° C/WATT



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

N18 Plastic Kool DIP™ N20 Plastic Kool DIP™

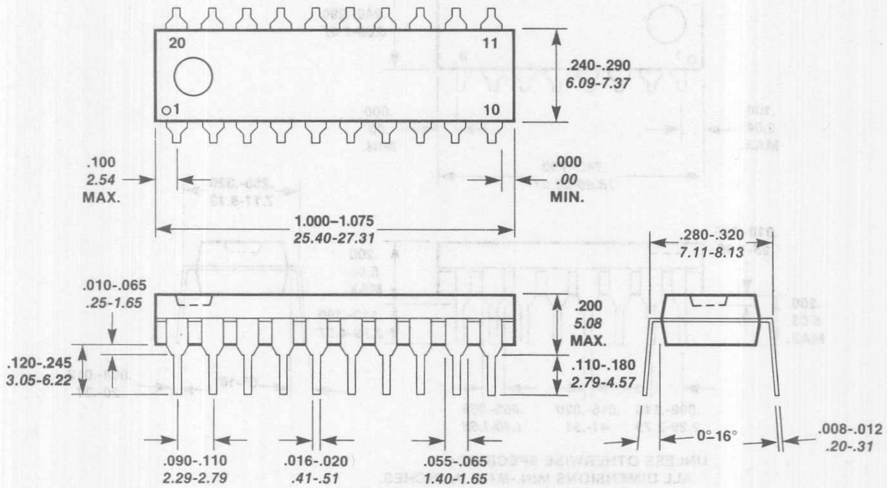
θ_{JA} = 75° C/WATT
θ_{JC} = 35° C/WATT



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

N20 Plastic Kool DIP

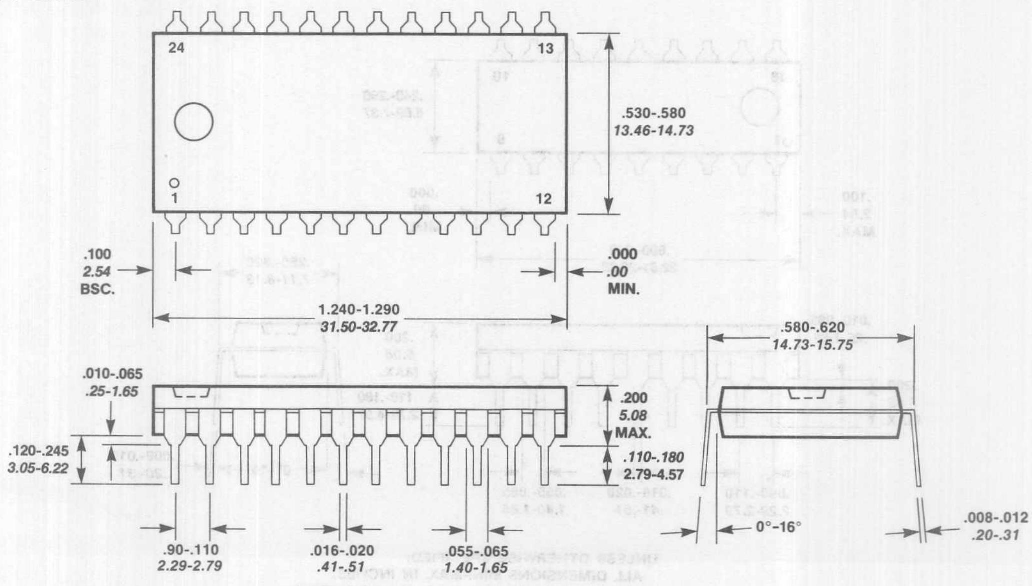
θ_{JA} = 75° C/WATT
θ_{JC} = 35° C/WATT



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

N24 Plastic Kool DIP™

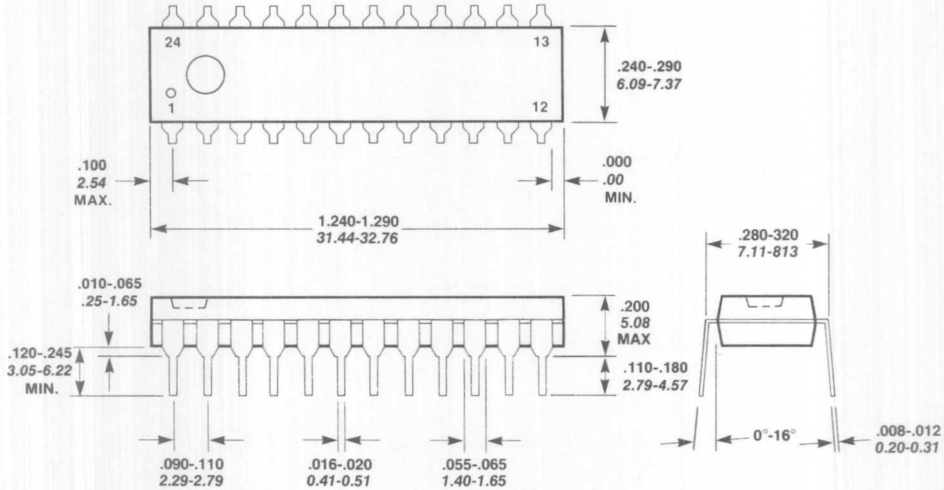
θ_{JA} = 65° C/WATT
θ_{JC} = 30° C/WATT



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

N24S Plastic Kool SKINNYDIP™

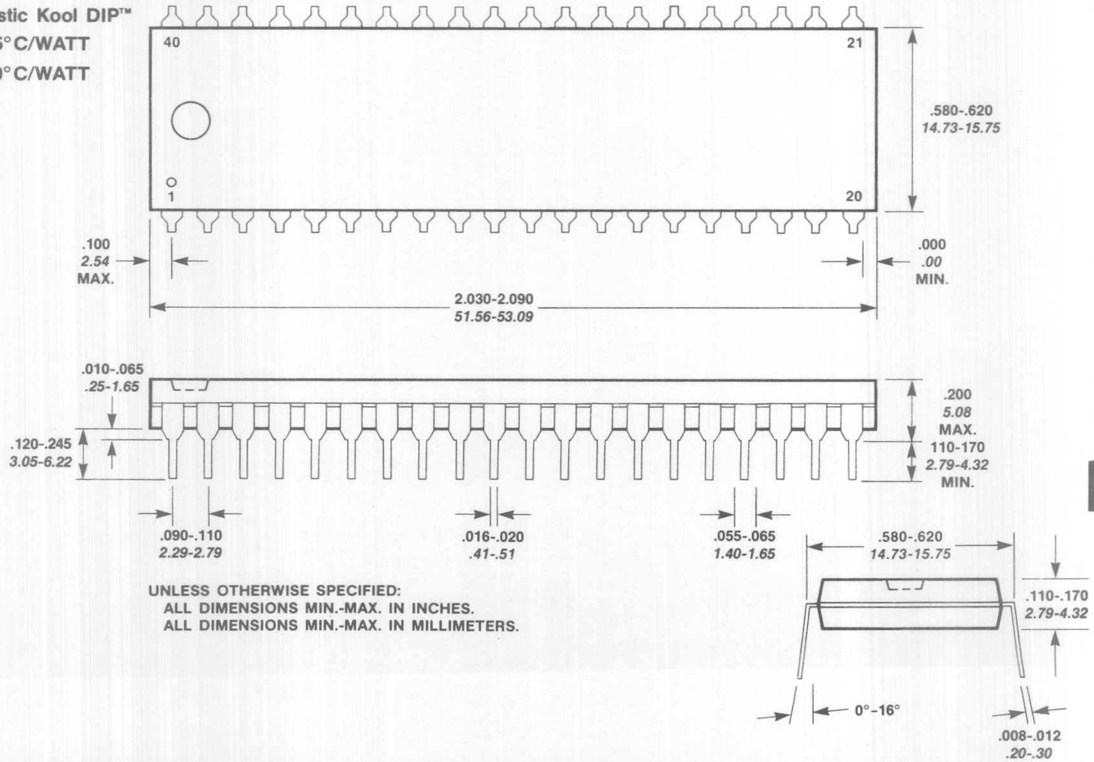
θ_{JA} = 75°C/WATT
θ_{JC} = 35°C/WATT



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

N40 Plastic Kool DIP™

θ_{JA} = 65°C/WATT
θ_{JC} = 30°C/WATT



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.