

AccessionIndex: TCD-SCSS-T.20250922.001

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Object name: Intel C3000 bit-slice chipset and associated chips

Vintage: 1974

Synopsis: Intel's bipolar microprogrammed bit-slice processor.

Description:

Intel's C3000 [1][2][3][4][5] was a Schottky bipolar bit-slice chipset introduced in September, 1974. It consisted of the C3001 microprogram control unit and the C3002 central processing element, both intended for use in microprogrammed computer architectures.

Microprogramming was invented by Maurice Wilkes at Cambridge University, U.K. in 1951 [6]. Even by then a computer was understood to consist of a central processing unit (CPU), memory and input/output. Wilkes proposed that the CPU hardware would be simpler if a very basic CPU could be *microprogrammed* to emulate a higher-level instruction set of the user-level CPU and thereby execute programs in the user-level memory (Fig.1). This simple CPU would be composed of a microprogram control unit, microprogram memory and a central processing element.

This concept was of great value while hardware (both logic and memory) was expensive, as it was for the vacuum-tube era of the early 1950s and the transistor era of the late 1950s and early 1960s, as well as for the early microprocessor era of the 1970s and 1980s. Since then the ability to fabricate billions of inexpensive transistors on a chip has rendered this a niche value concept.

Intel designed the C3000 chipset in the early 1970s to implement this concept. The microprogrammed CPU would comprise a C3001 microprogram control unit (MCU), microprogram memory and multiple C3002 central processing elements (CPEs), see Figs.2-3. The MCU would address its own microprogram memory, with some of its contents being used to control the program sequence. But other of the contents would be distributed to the CPEs to control their operations. Fig.4 shows a C3001 MCU and 16-bit C3002 array (non-pipelined) configuration. Adding a pipeline register as in Fig.5 would speed up execution. Vectored interrupts could be added using the C3214 interrupt control unit, see Fig.6.

The C3001 included the microprogram address register, selected the next microinstruction as needed. Its architecture is shown in Fig.7. It could address 512 microinstructions using a 9-bit microprogram address register, with provision for selection of the next microinstruction based on the contents of the microprogram address register, or a jump function, or decoded and tested data from several busses, or microprogram interrupts, with 11 address control functions selected by the next address logic, including 3 jump & test latch functions, and a 16-way jump & test instruction bus function. It had 2 flag registers, with 8 flag control functions. The sequencer was difficult to write code for due to the variety of row and column jumps to get from point A to point B in the address map.

The C3002 central processing element (CPE) was a 2-bit arithmetic logic unit (ALU) plus a register file. Its architecture is shown in Fig.8. Multiple of these could be

connected to build a wider word-length ALU. It had 3 input data busses and 2 tristate output data busses, 11 general purpose registers, an accumulator, and an independent memory address register. It was able to execute any of over 40 functions in 8 function groups, e.g. 2's complement arithmetic, logical AND, OR, NOT and exclusive-OR, increment/decrement, shift left/right, bit test and zero detection, with internal carry look-ahead generation. Faster external carry/borrow propagation could be added using the C3003 carry look-ahead adder, see Fig.9. Its main drawback was that it was only a 2-bit slice, whereas competitors were mostly 4-bits, and eventually 8-bits and even later 16-bits.

In addition Intel provided the following support chips, see [7]:

Part	Function
3003	Carry-lookahead adder
3205	1 of 8 binary decoder
3207	Quad Bipolar-to-MDS Level Shifter and Driver
3208	Hex Sense Amplifier for MOS Memories
3210	TTL-to-MOS Level Shifter and High Voltage Clock Driver
3211	ECL-to-MOS Level Shifter and High Voltage Clock Driver
3212	Multimode latch buffer
3214	Priority interrupt unit
3216	Noninverting bidirectional bus driver
3222	Refresh Controller for 4K NMOS DRAMs
3226	Inverting bidirectional bus driver
3232	Address Multiplexer and Refresh Counter for 4K DRAMs
3235	Quad Bipolar-to-MOS Level Shifter and Drive
3242	Address Multiplexer and Refresh Counter for 16K DRAMs
3245	Quad Bipolar TTL-to-MOS Level Shifter and Driver for 4K
3246	Quad Bipolar ECL-to-MOS Level Shifter and Driver for 4K
3404	High-performance 6-bit Latch
3408	Hex Sense Amp and Latch for MOS Memories
3601	256x4-bit programable read-only memory
3604	512x8-bit programable read-only memory
3301A	256x4-bit read-only memory
3304A	512x8-bit read-only memory

The chipset was DTL and TTL compatible with a $5V \pm 5\%$ power supply, dissipated 0.85-1.26W, had a 0°C - 70°C operating temperature range, could be clocked at up to 10MHz, and had a minimum cycle time of 85ns. The C3000 was second sourced by Signetics and Intersil. Notably, Signetics then designed and manufactured an 8080 emulator based on the C3000 chipset [8].

Many thanks to Brian Coghlan for donating these items.

The homepage for this catalog is at: <https://www.scss.tcd.ie/SCSSTreasuresCatalog/>
 Click 'Accession Index' (1st column listed) for related folder, or 'About' for further guidance.
 Some of the items below may be more properly part of other categories of this catalog,
 but are listed here for convenience.

Accession Index	Object with Identification
TCD-SCSS-T.20250922.001	Intel C3000 bit-slice chipset and associated chips. Intel's bipolar microcoded bit-slice processor. 1974.
TCD-SCSS-T.20250922.001.01	1 x Intel C3001 microprogram control unit.
TCD-SCSS-T.20250922.001.02	13 x Signetics N3002 central processing element.
TCD-SCSS-T.20250922.001.03	1 x Intel C3003 carry look-ahead adder.
TCD-SCSS-T.20250922.001.04	1 x Intel C3214 priority interrupt unit.
TCD-SCSS-T.20250922.001.05	1 x Intel B3222 DRAM controller.
TCD-SCSS-T.20250922.001.06	1 x Intel D3242 address multiplexer and refresh controller.
TCD-SCSS-X.20250916.001	Dr. Brian Coghlan's Collection of Early Microprocessors. An extensive and nearly complete set of unused 1970s microprocessor chips, most accompanied with documentation, some with demonstration boards. 1971.

References:

1. Intel, *Intel 3001 Microprogram Control Unit*, see:
<https://www.scss.tcd.ie/SCSSTreasuresCatalog/hardware/TCD-SCSS-T.20250922.001/Intel-3001-datasheet.pdf>
 Last browsed to on 22-Sep-2025.
2. Intel, *Intel 3002 Central Processing Element*, see:
<https://www.scss.tcd.ie/SCSSTreasuresCatalog/hardware/TCD-SCSS-T.20250922.001/Intel-3002-datasheet.pdf>
 Last browsed to on 22-Sep-2025.
3. Intel, *Intel 3003 Look-ahead Carry Generator*, see:
<https://www.scss.tcd.ie/SCSSTreasuresCatalog/hardware/TCD-SCSS-T.20250922.001/Intel-3003-datasheet.pdf>
 Last browsed to on 22-Sep-2025.
4. Intel, *Intel 3014 Interrupt Control Unit*, see:
<https://www.scss.tcd.ie/SCSSTreasuresCatalog/hardware/TCD-SCSS-T.20250922.001/Intel-3014-datasheet.pdf>
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5. CPUshack, *The Collector's Guide to Vintage Intel Microchips*, see:
<https://www.cpushack.com/wp-content/uploads/2018/06/VintageIntelMicrochipsRev4.pdf>
 Last browsed to on 22-Sep-2025.
6. Maurice Wilkes, *The Best Way to Design an Automatic Calculating Machine*,
 In: *Manchester University Computer, Inaugural Conference*, July 1951, pp.16-18;
 reprinted in *Annals of the History of Computing*, pp.118-121, Vol.8, 1986,

and in *The Early British Computer Conferences*, M.R. Williams and M. Campbell-Kelly, eds., Charles Babbage Institute Reprint Series for the History of Computing, pp.182-184, Vol.14, MIT Press, Cambridge, Mass., and Tomash Publishers, Los Angeles, 1989.

7. Intel, *Intel C3000 Datasheets*, see:
<https://www.scss.tcd.ie/SCSSTreasuresCatalog/hardware/TCD-SCSS-T.20250922.001/Intel-C3000-datasheets/>
Last browsed to on 22-Sep-2025.
8. Signetics, *Signetics 8080 Emulator Manual*, March 1977, see:
https://bitsavers.org/components/signetics/Signetics_8080_Emulator_Manual_Mar77.pdf
Also: <https://www.scss.tcd.ie/SCSSTreasuresCatalog/hardware/TCD-SCSS-T.20250922.001/Signetics-8080EmulatorManual-Mar1977.pdf>
Last browsed to on 22-Sep-2025.

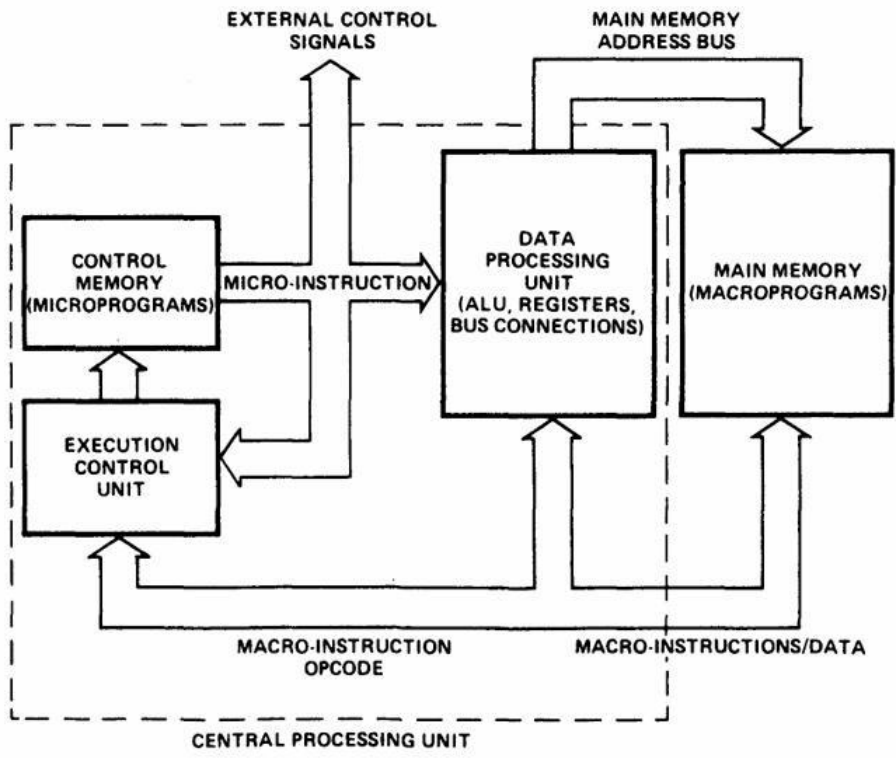


Figure 1: Microprogrammed central processing unit and user-level memory.

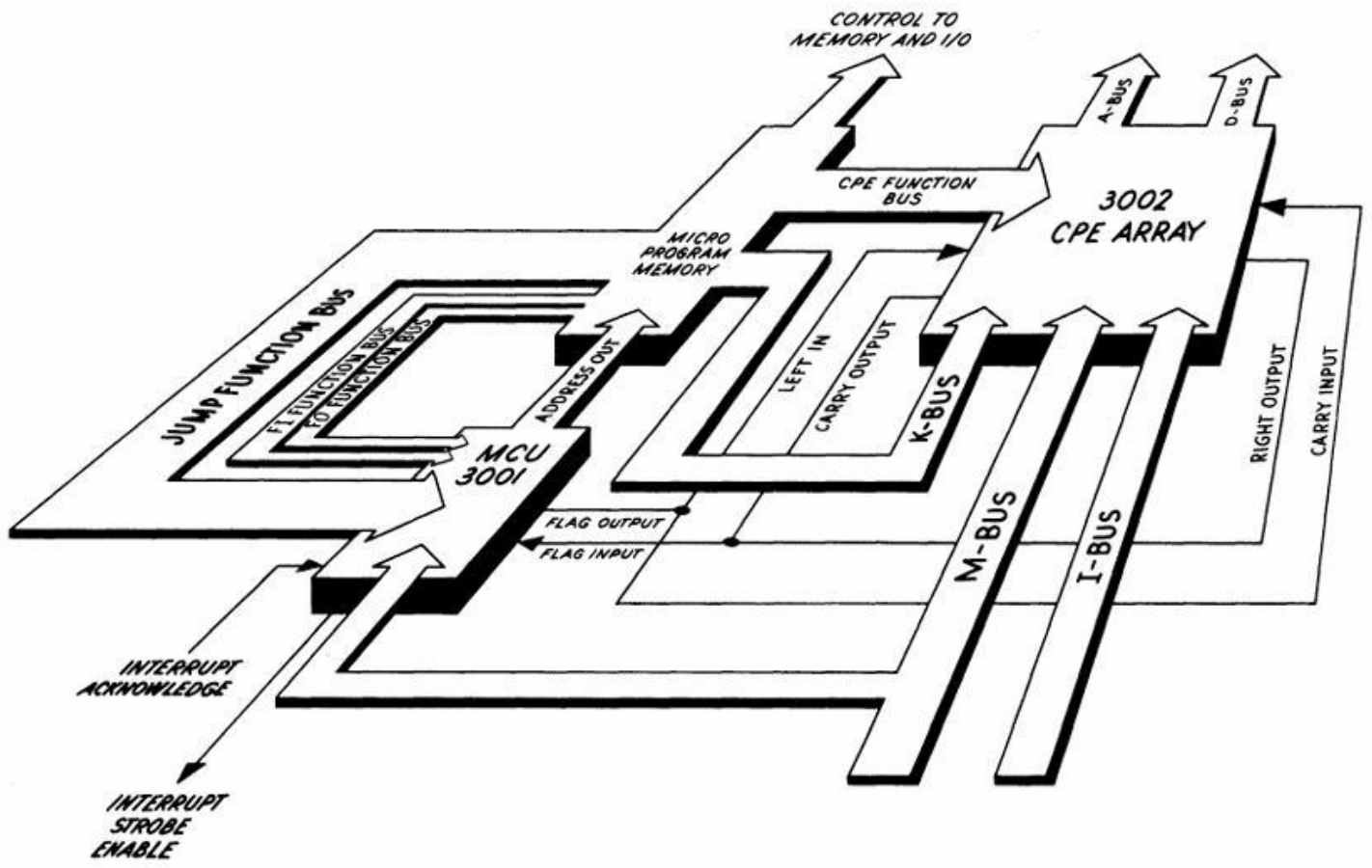


Figure 2: Intel marketing graphic of C3000 central processing unit.

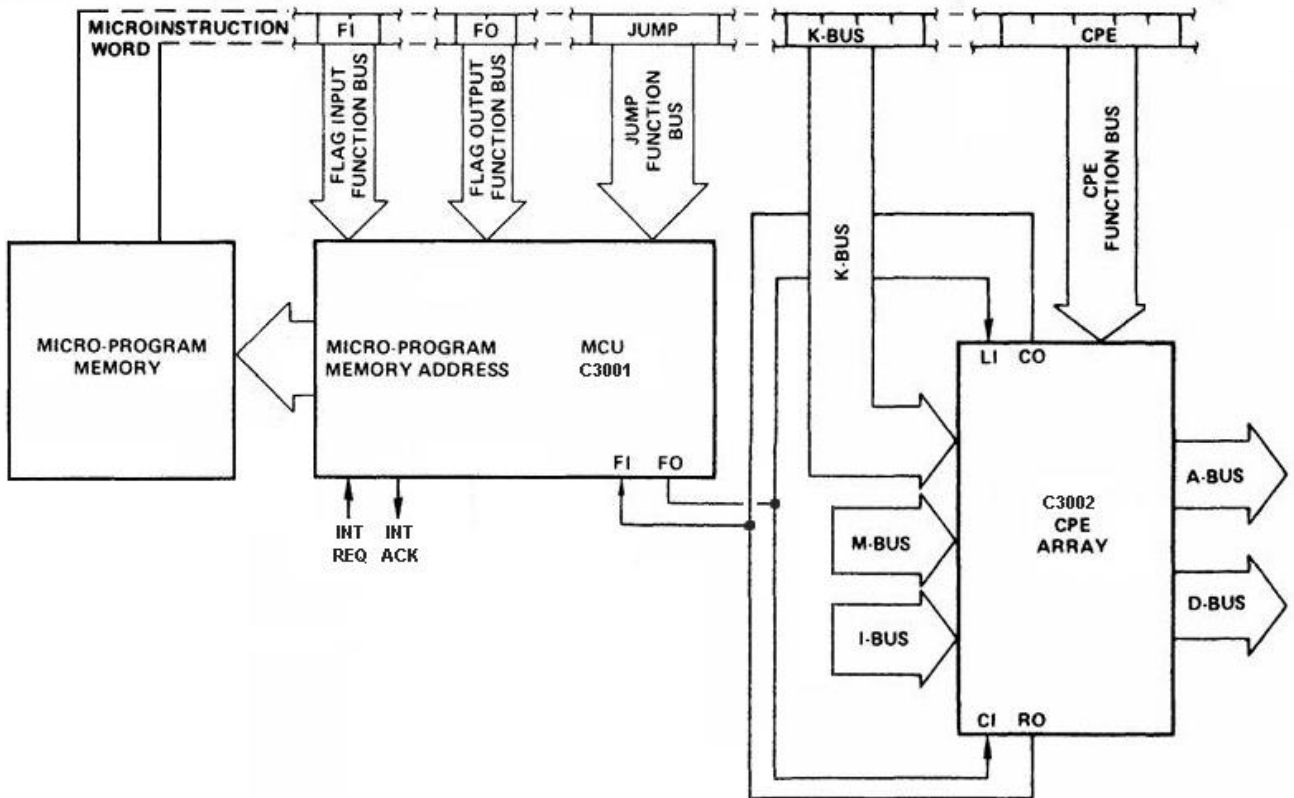


Figure 3: Intel C3000 central processing unit (non-pipelined).

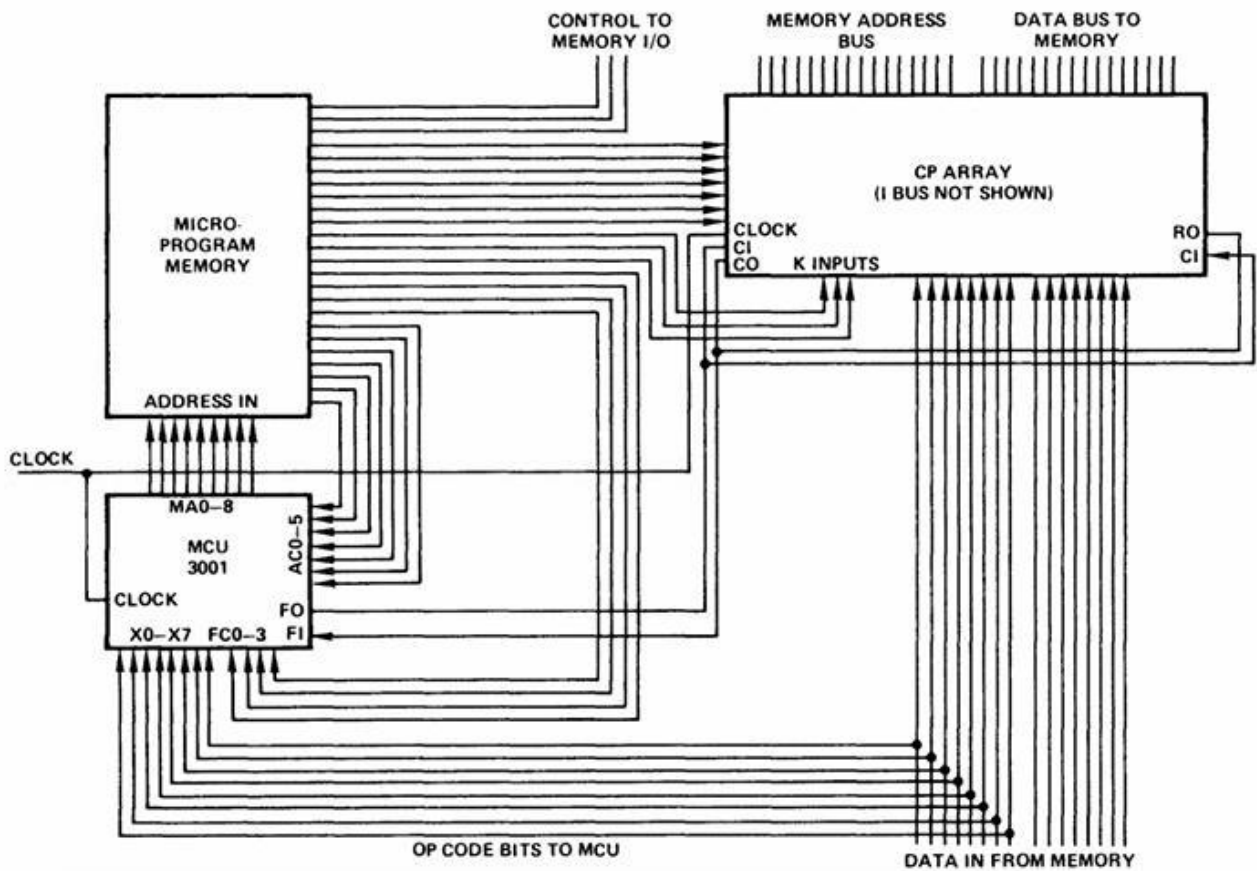


Figure 4: Intel C3001 and 16-bit C3002 array (non-pipelined).

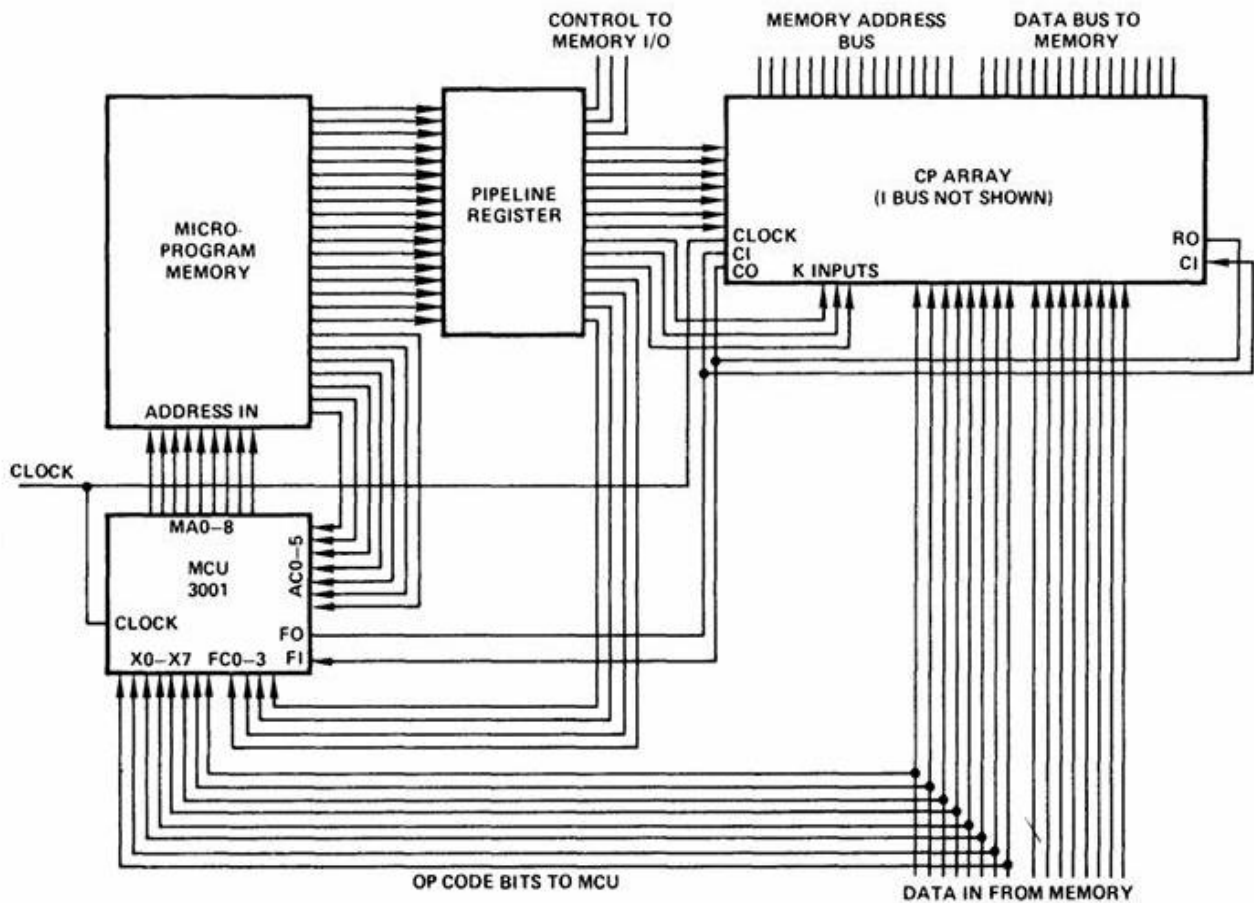


Figure 5: Pipelined Intel C3001 and 16-bit C3002 array.

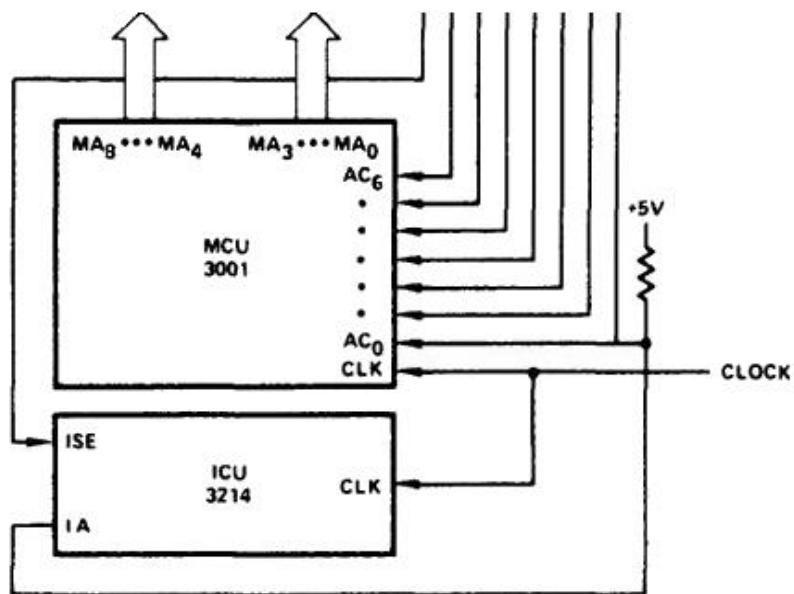


Figure 6: Adding the C3214 interrupt control unit to the Intel C3001 microprogram control unit. The C3214 provides vectored interrupts.

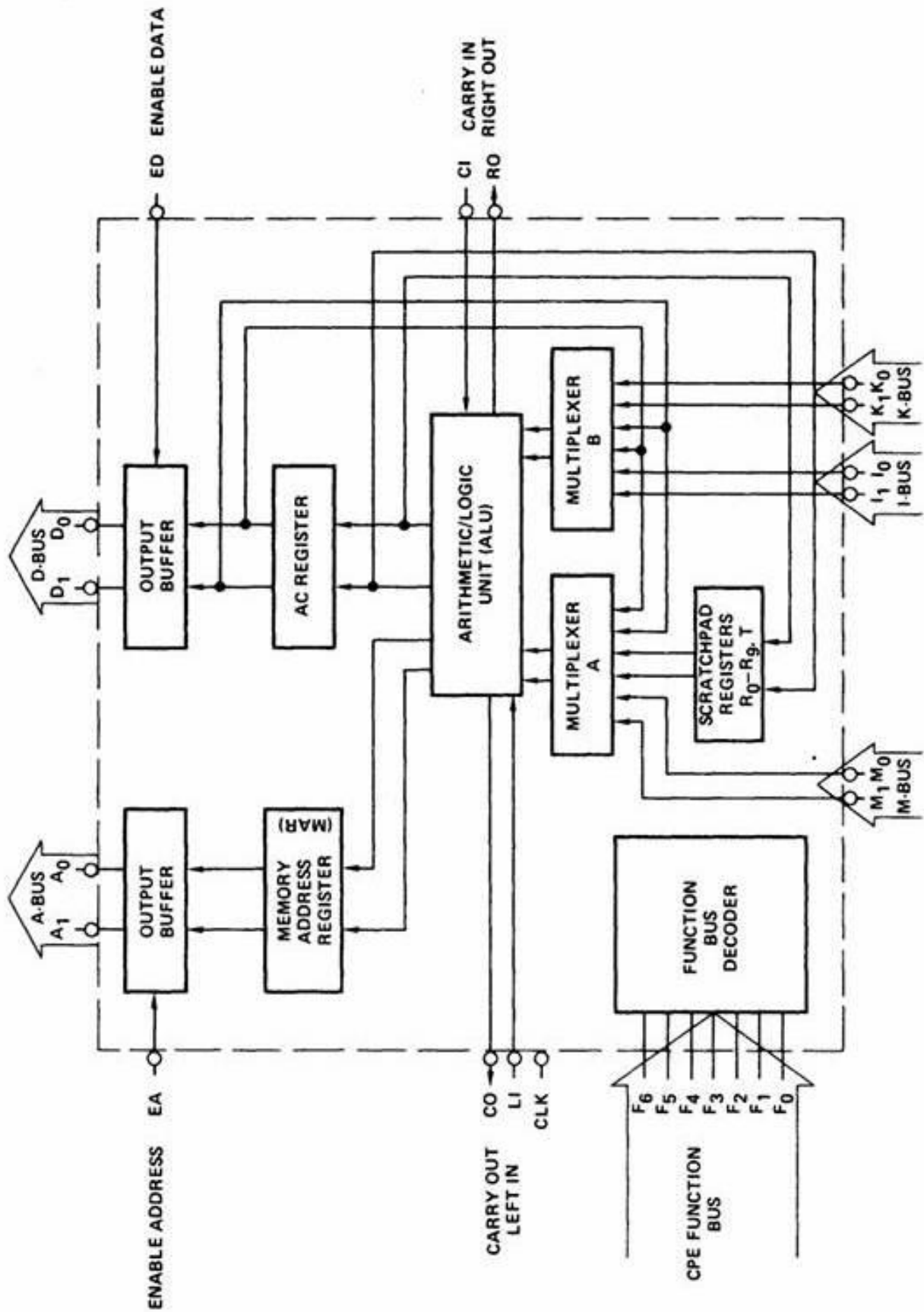


Figure 8: Intel C3002 central processing element (CPE) architecture.

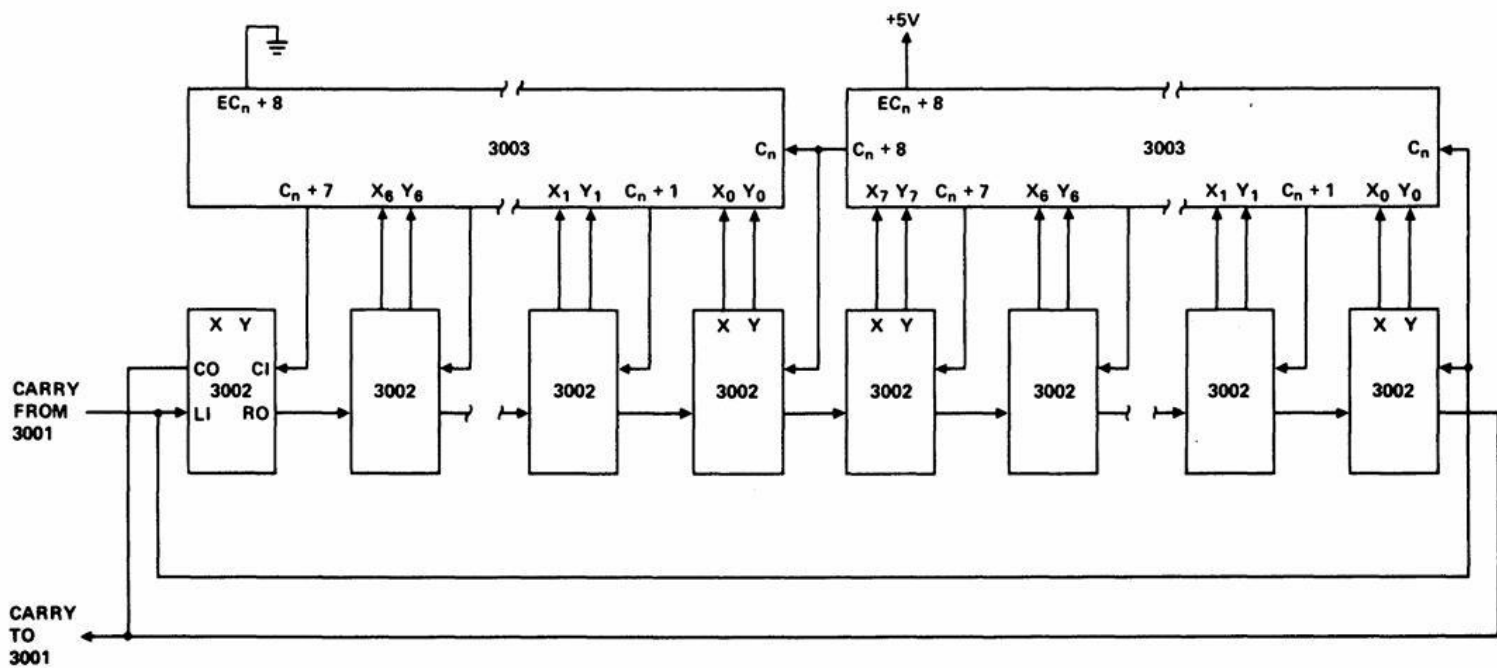


Figure 9: Adding the C3003 carry-lookahead adder to the Intel C3002 central processing element.