QUAD ECL-TO-MOS DRIVER

For 4K N-Channel MOS RAMs

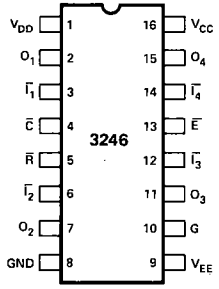
- **Fully Compatible With 4K RAMs Without Requiring Extra Supply Or External Devices.**
- **High Speed, 30 nsec Max. — Delay + Rise Time**
- **10K ECL Compatible Inputs**
- **High Density — Four Drivers In One Package**
- **CerDIP Package — 16 Pin DIP**

The Intel® 3246 is a Quad Bipolar-to-MOS driver which accepts ECL input signals. It provides high output current and voltage suitable for driving the clock inputs of N-channel MOS memories such as the 2107 or 2105. The circuit operates from three power supplies which are 5, -5.2, and 12 volts. Input and output clamp diodes minimize line reflections.

The device features a common enable input, a refresh select input, and a clock control input for simplified system designs. The internal gating structure of the 3246 eliminates gating delays and minimizes package count.

The 3246 is fabricated by means of Intel's Schottky Bipolar technology to assure high performance over the 0°C to +75°C ambient temperature range.

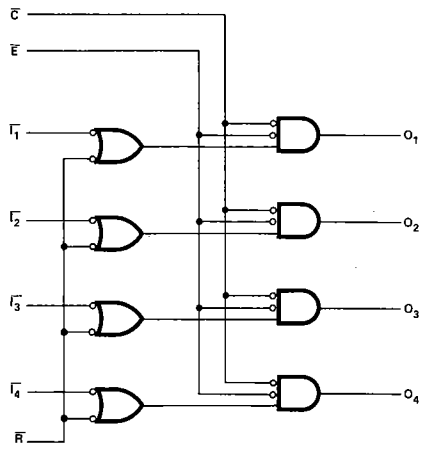
PIN CONFIGURATION



PIN NAMES

$\overline{I_1}$-$\overline{I_4}$	SELECT INPUTS	O_1-O_4	DRIVER OUTPUTS
$\overline{E}$	ENABLE INPUT	V_{CC}	+5V POWER SUPPLY
$\overline{R}$	REFRESH SELECT INPUT	V_{DD}	+12V POWER SUPPLY
$\overline{C}$	CLOCK CONTROL INPUT	V_{EE}	-5.2V POWER SUPPLY
		G	GROUND REFERENCE

LOGIC DIAGRAM



Final Data Sheet Information Will Be Available In Second Quarter 1976.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to 85°C
Storage Temperature . . . . . -65°C to +150°C
Supply Voltage, V_{CC} . . . . . -0.5 to +7V
Supply Voltage, V_{DD} . . . . . -0.5 to +14V
Supply Voltage, V_{EE} . . . . . -7.0 to +0.5V
All Input Voltages . . . . . V_{EE} to +0.5V
Outputs for Clock Driver . . . . . -1.0 to V_{DD} +1V
Power Dissipation at 25°C 2W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

T_A = 0°C to 75°C, V_{CC} = 5.0V ±5%, V_{DD} = 12V ±5%, V_{EE} = -5.2V ±5%

Symbol	Parameter	Min.	Typ[1]	Max.	Unit	Test Conditions
I_{FD}	Input Load Current, $\overline{I_1}$, $\overline{I_2}$, $\overline{I_3}$, $\overline{I_4}$		0.3	0.5	mA	V_F = -0.8V
I_{FE}	Input Load Current, $\overline{R}$,$\overline{C}$,$\overline{E}$		1.0	2.0	mA	V_F = -0.8V
V_{OL}	Output Low Voltage		0.2	0.45	V	I_{OL}=5mA, V_{IH}=-1.025V
		-0.5			V	I_{OL} = -1mA
V_{OH}	Output High Voltage	V_{DD}-0.5	V_{DD}-0.2		V	I_{OH}=-1mA, V_{IL}=-1.520V
			V_{DD}	V_{DD}+0.5	V	I_{OH} = 5mA
V_{IL}	Input Low Voltage, All Inputs			-1.520	V	
V_{IH}	Input High Voltage, All Inputs	-1.025			V	

POWER SUPPLY CURRENT DRAIN AND POWER DISSIPATION

Symbol	Parameter	Typ.[1]	Max.	Unit	Test Conditions — Input states to ensure the following output states:	Additional Test Conditions
I_{CC}	Current from V_{CC}	20	27	mA	High	V_{CC} = 5.25V V_{DD} = 12.6V V_{EE} = -5.46V
I_{DD}	Current from V_{DD}	23	31	mA		
I_{EE}	Current from V_{EE}	-35	-42	mA		
P_{D1}	Power Dissipation	586	762	mW		
	Power Per Channel	146	190	mW		
I_{CC}	Current from V_{CC}	17	24	mA	Low	
I_{DD}	Current from V_{DD}	14	22	mA		
I_{EE}	Current from V_{EE}	-29	-36	mA		
P_{D2}	Power Dissipation	424	600	mW		
	Power Per Channel	106	150	mW		

Note: 1. Typical values are for T_A = 25°C and nominal power supply voltages.

A.C. Characteristics $T_A = 0°$ to $75°C$, $V_{CC} = 5.0V \pm 5\%$, $V_{DD} = 12V \pm 5\%$, $V_{EE} = -5.2V \pm 5\%$

Symbol	Parameter	Min.[1]	Typ.[2,4]	Max.[3]	Unit	Test Conditions
t_{-+}	Input to Output Delay	8	12		ns	$R_{SERIES} = 0$
t_{DR}	Delay Plus Rise Time		18	30	ns	$R_{SERIES} = 0$
t_{+-}	Input to Output Delay	8	13		ns	$R_{SERIES} = 0$
t_{DF}	Delay Plus Fall Time		25	35	ns	$R_{SERIES} = 0$
t_T	Output Rise Time	10	13	23	ns	$R_{SERIES} = 20\Omega$
t_{DR}	Delay Plus Rise Time		23	34	ns	$R_{SERIES} = 20\Omega$
t_{DF}	Delay Plus Fall Time		30	40	ns	$R_{SERIES} = 20\Omega$

NOTES: 1. $C_L = 150pF$
2. $C_L = 200pF$
3. $C_L = 250pF$

These values represent a range of total stray plus clock capacitance for nine 4K RAMs.

4. Typical values are measured at 25°C.

MEMORY SUPPORT

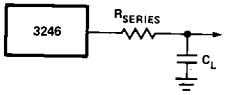
Capacitance* $T_A = 25°C$

Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance, $\overline{I_1}, \overline{I_2}, \overline{I_3}, \overline{I_4}, \overline{R}$	4	7	pF
C_{IN}	Input Capacitance, $\overline{C}, \overline{E}$	8	12	pF

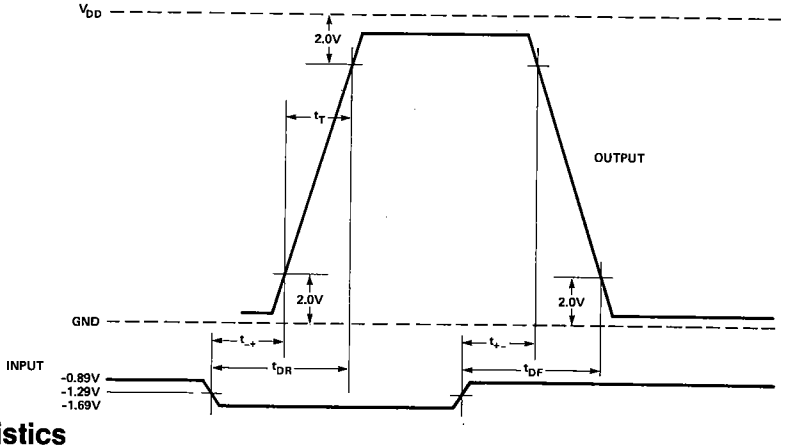
*This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, $V_{bias} = -1V$, $V_{CC} = 0V$, and $T_A = 25°C$.

A.C. CONDITIONS OF TEST

Input Pulse Amplitudes: 0.8V
Input Pulse Rise and Fall Times: 5 ns (between 10% and 90% Points)
Measurement Points: See Waveforms

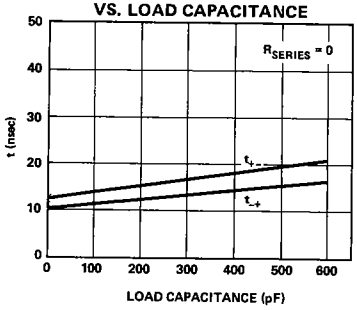


Waveforms

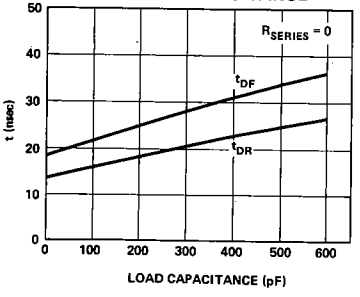


Typical Characteristics

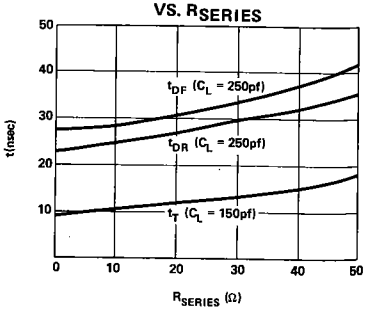
INPUT TO OUTPUT DELAY VS. LOAD CAPACITANCE



DELAY PLUS TRANSITION TIME VS. LOAD CAPACITANCE

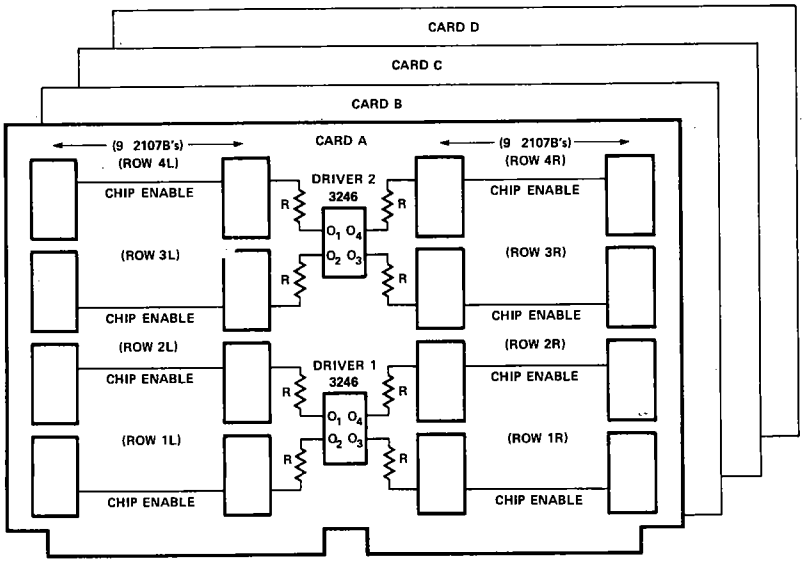


DELAY PLUS TRANSITION TIME VS. R_{SERIES}



Typical System

Below is an example of a 64K x 18 bit memory system (each card is 16K x 18) employing the 3246 quad high voltage driver for the chip enable inputs. A single 3246 package drives 16K x 9 bits. A_0 through A_{11} are 2107B addresses.



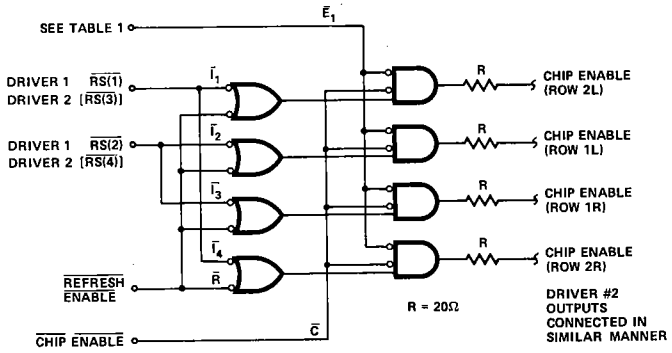


TABLE 1.

CARD	INPUTS E_1
A	$\overline{\text{ENABLE M}}$
B	$\overline{\text{ENABLE N}}$
C	$\overline{\text{ENABLE P}}$
D	$\overline{\text{ENABLE Q}}$