QUAD TTL-TO-MOS DRIVER

For 4K N-Channel MOS RAMs

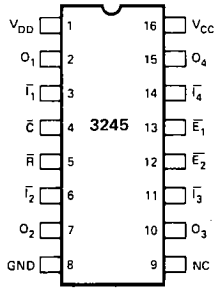
- **Fully Compatible With 4K RAMs Without Requiring Extra Supply Or External Devices**
- **High Speed, 32 nsec Max. — Delay + Transition Time**
- **Low Power — 75mW Typical Per Channel**
- **High Density — Four Drivers in One Package**
- **TTL & DTL Compatible Inputs**
- **CerDIP Package — 16 Pin DIP**
- **Only +5 and +12 Volt Supplies Required**

The Intel® 3245 is a Quad Bipolar-to-MOS driver which accepts TTL and DTL input signals. It provides high output current and voltage suitable for driving the clock inputs of N-channel MOS memories such as the 2107B. The circuit operates from two power supplies which are 5 and 12 volts. Input and output clamp diodes minimize line reflections.

The device features two common enable inputs, a refresh select input, and a clock control input for simplified system designs. The internal gating structure of the 3245 eliminates gating delays and minimizes package count.

The 3245 is fabricated by means of Intel's highly reliable Schottky bipolar process and is specified for operation over a 0 to +75°C ambient temperature range.

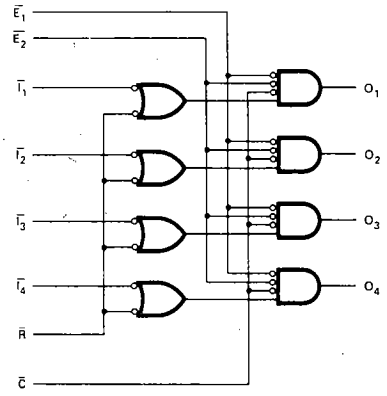
PIN CONFIGURATION



PIN NAMES

$\overline{I}_1$-$\overline{I}_4$	SELECT INPUTS	O_1-O_4	DRIVER OUTPUTS
$\overline{E}_1$,$\overline{E}_2$	ENABLE INPUTS	V_{CC}	+5V POWER SUPPLY
$\overline{R}$	REFRESH SELECT INPUT	V_{DD}	+12V POWER SUPPLY
$\overline{C}$	CLOCK CONTROL INPUT	NC	NOT CONNECTED

LOGIC DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to 85°C
Storage Temperature. . . . . -65°C to +150°C
Supply Voltage, V_{CC} . . . . . -0.5 to +7V
Supply Voltage, V_{DD} . . . . . -0.5 to +14V
All Input Voltages . . . . . -1.0 to V_{DD}
Outputs for Clock Driver . . . . . -1.0 to V_{DD} +1V
Power Dissipation at 25°C 2W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

T_A = 0°C to 75°C, V_{CC} = 5.0V ±5%, V_{DD} = 12V ±5%

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
I_{FD}	Input Load Current, $\overline{I}_1, \overline{I}_2, \overline{I}_3, \overline{I}_4$		-0.25	mA	V_F = 0.45V
I_{FE}	Input Load Current, $\overline{R}, \overline{C}, \overline{E}_1, \overline{E}_2$		-1.0	mA	V_F = 0.45V
I_{RD}	Data Input Leakage Current		10	μA	V_R = 5.0V
I_{RE}	Enable Input Leakage Current		40	μA	V_R = 5.0V
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 5mA, V_{IH} = 2V
		-1.0		V	I_{OL} = -5mA
V_{OH}	Output High Voltage	V_{DD}-0.50		V	I_{OH} = -1mA, V_{IL} = 0.8V
			V_{DD}+1.0	V	I_{OH} = 5mA
V_{IL}	Input Low Voltage, All Inputs		0.8	V	
V_{IH}	Input High Voltage, All Inputs	2		V	

POWER SUPPLY CURRENT DRAIN AND POWER DISSIPATION

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions — Input states to ensure the following output states:	Additional Test Conditions
I_{CC}	Current from V_{CC}	23	30	mA	High	
I_{DD}	Current from V_{DD}	19	26	mA		
P_{D1}	Power Dissipation	365	485	mW		
	Power Per Channel	91	121	mW		V_{CC} = 5.25V
I_{CC}	Current from V_{CC}	29	39	mA	Low	V_{DD} = 12.6V
I_{DD}	Current from V_{DD}	12	15	mA		
P_{D2}	Power Dissipation	300	388	mW		
	Power Per Channel	75	97	mW		

A.C. Characteristics $T_A = 0°$ to $75°C$, $V_{CC} = 5.0V \pm 5\%$, $V_{DD} = 12V \pm 5\%$

Symbol	Parameter	Min.[1]	Typ.[2,4]	Max.[3]	Unit	Test Conditions
t_{-+}	Input to Output Delay	5	11		ns	$R_{SERIES} = 0$
t_{DR}	Delay Plus Rise Time		20	32	ns	$R_{SERIES} = 0$
t_{+-}	Input to Output Delay	3	7		ns	$R_{SERIES} = 0$
t_{DF}	Delay Plus Fall Time		18	32	ns	$R_{SERIES} = 0$
t_T	Output Transition Time	10	17	25	ns	$R_{SERIES} = 20\Omega$
t_{DR}	Delay Plus Rise Time		27	38	ns	$R_{SERIES} = 20\Omega$
t_{DF}	Delay Plus Fall Time		25	38	ns	$R_{SERIES} = 20\Omega$

NOTES: 1. $C_L = 150pF$
2. $C_L = 200pF$
3. $C_L = 250pF$

These values represent a range of total stray plus clock capacitance for nine 4K RAMs.

4. Typical values are measured at 25°C.

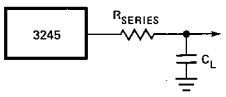
Capacitance* $T_A = 25°C$

Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance, $\overline{I}_1, \overline{I}_2, \overline{I}_3, \overline{I}_4$	5	8	pF
C_{IN}	Input Capacitance, $\overline{R}, \overline{C}, \overline{E}_1, \overline{E}_2$	8	12	pF

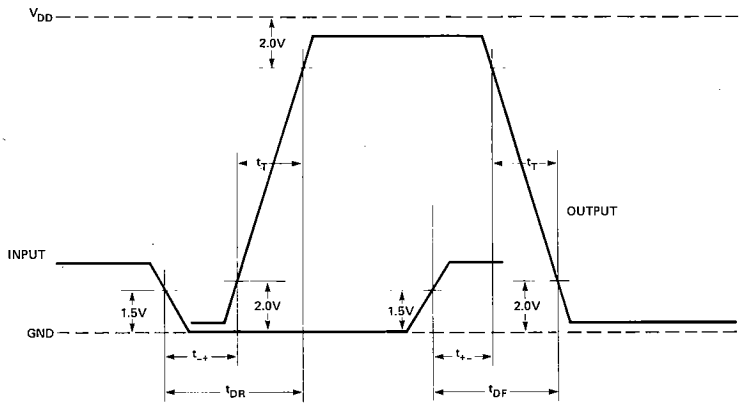
*This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, $V_{bias} = 2V$, $V_{CC} = 0V$, and $T_A = 25°C$.

A.C. CONDITIONS OF TEST

Input Pulse Amplitudes: 3.0V
Input Pulse Rise and Fall Times: 5 ns between 1 volt and 2 volts
Measurement Points: See Waveforms

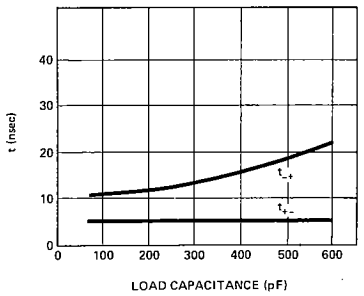


Waveforms

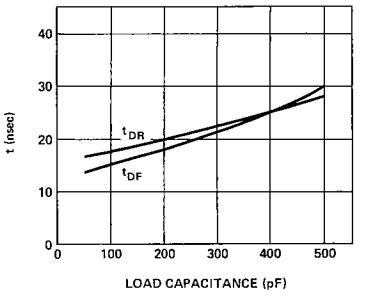


Typical Characteristics

INPUT TO OUTPUT DELAY VS. LOAD CAPACITANCE

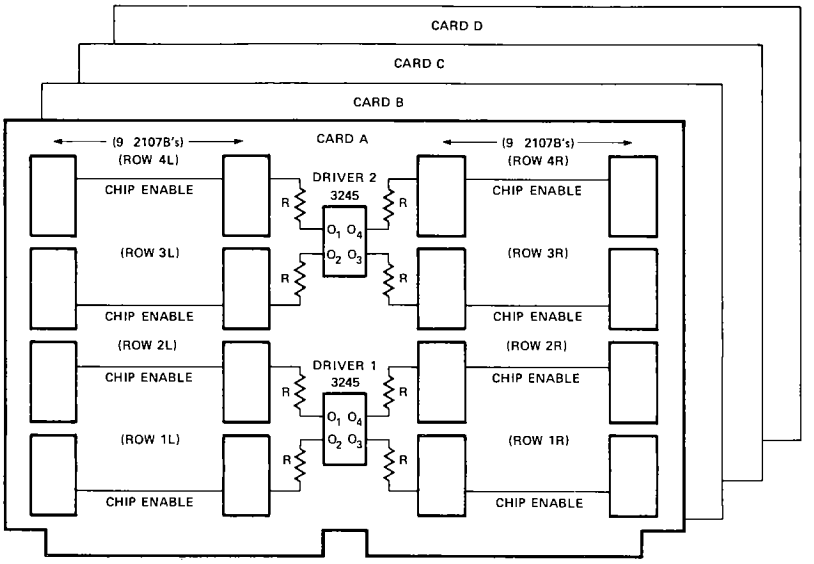


DELAY PLUS TRANSITION TIME VS. LOAD CAPACITANCE



Typical System

Below is an example of a 64K x 18 bit memory system (each card is 16K x 18) employing the 3245 quad high voltage driver for the chip enable inputs. A single 3245 package drives 16K x 9 bits. A_0 through A_{11} are 2107B addresses.



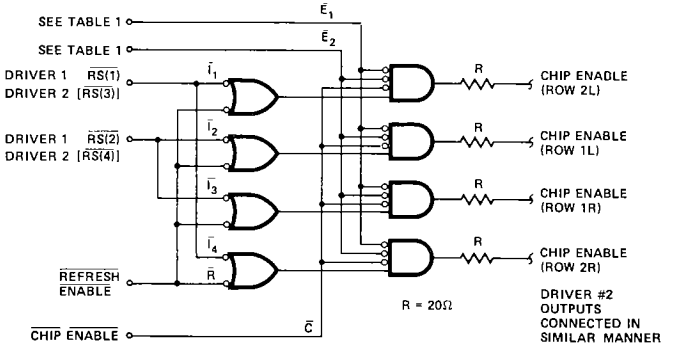


TABLE 1.

CARD	INPUTS $\bar{E}_1$	INPUTS $\bar{E}_2$
A	ENABLE M	ENABLE P
B	ENABLE M	ENABLE Q
C	ENABLE N	ENABLE P
D	ENABLE N	ENABLE Q