QUAD BIPOLAR-TO-MOS DRIVER

For 4K N-Channel MOS RAMs

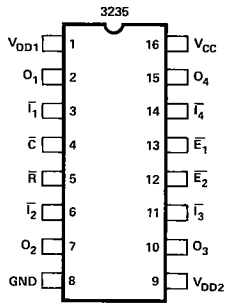
- **High Speed, 32 nsec Max.— Delay + Transition Time Over Temperature with 250 pF load**
- **High Density -- Four Drivers in One Package**
- **Internal Gating Structure Minimizes Package Count and Eliminates Gating Delays**
- **TTL & DTL Compatible Inputs**
- **Minimum Line Reflection--Input and Output Clamp Diodes**
- **Safety Feature Protects 4 K RAMs if +5 V System Supply is Lost**
- **CerDIP Package--16 Pin DIP**

The Intel 3235 is a Quad Bipolar-to-MOS driver which accepts TTL and DTL input signals. It provides high output current and voltage suitable for driving the clock inputs of N-channel MOS memories such as the 2107 or 2105. The circuit operates from three power supplies which are 5, 12, and 15 volts.

The device features two common enable inputs, a refresh select input, and a clock control input for simplified system designs.

A safety feature forces all outputs low if the V_{CC} power supply is lost. This protects 4K RAM's by putting them in the standby mode.

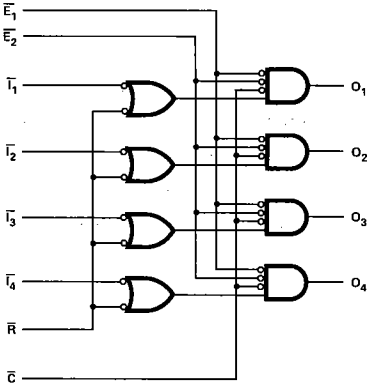
PIN CONFIGURATION



PIN NAMES

$\overline{I_1}$–$\overline{I_4}$	DATA INPUTS	O_1–O_4	DRIVER OUTPUTS
$\overline{E_1}$, $\overline{E_2}$	ENABLE INPUTS	V_{CC}	+5V POWER SUPPLY
$\overline{R}$	REFRESH SELECT INPUT	V_{DD1}	+12V POWER SUPPLY
$\overline{C}$	CLOCK CONTROL INPUT	V_{DD2}	+15V POWER SUPPLY

LOGIC DIAGRAM



The 3245 is a pin-for-pin replacement for the 3235 and has the additional advantage of not requiring a +15V supply. See Data Catalog Supplement for complete specifications on the 3245.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . 0°C to 75°C
Storage Temperature . . . . . -65°C to +150°C
Supply Voltage, V_{CC} . . . . . -0.5 to +7V
Supply Voltage, V_{DD1} . . . . . -0.5 to +13V
Supply Voltage, V_{DD2} . . . . . -0.5 to +16V
All Input Voltages . . . . . -1.0 to V_{DD1}
Outputs for Clock Driver . . . . . -1.0 to V_{DD1}+1V
Power Dissipation at 25°C 2W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

T_A=0°C to 75°C, V_{CC}=5.0V ±5%, V_{DD1}=12V ±5%, V_{DD2}=V_{DD1}+(3V ±5%)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
I_{FD}	Input Load Current, $\overline{I}_1, \overline{I}_2, \overline{I}_3, \overline{I}_4$		-0.25	mA	V_F = 0.45V
I_{FE}	Input Load Current, $\overline{R}, \overline{C}, \overline{E}_1, \overline{E}_2$		-1.0	mA	V_F = 0.45V
I_{RD}	Data Input Leakage Current		10	μA	V_R = 5.0V
I_{RE}	Enable Input Leakage Current		40	μA	V_R = 5.0V
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 5mA, V_{IH} = 2V
V_{OH}	Output High Voltage	V_{DD1}-0.50		V	I_{OH} = -1mA, V_{IL} = 0.8V
V_{IL}	Input Low Voltage, All Inputs		0.8	V	
V_{IH}	Input High Voltage, All Inputs	2		V	

POWER SUPPLY CURRENT DRAIN AND POWER DISSIPATION

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions — Input states to ensure the following output states:	Additional Test Conditions
I_{CC}	Current from V_{CC}	21	32.0	mA	High	V_{CC} = 5.25V V_{DD1} = 12.6V V_{DD2} = 15.75V
I_{DD1}	Current from V_{DD1}	.2	2.0	mA		
I_{DD2}	Current from V_{DD2}	12.5	18.0	mA		
P_{D1}	Power Dissipation	310	477	mW		
	Power Per Driver	77	119	mW		
I_{CC}	Current from V_{CC}	36	46.0	mA	Low	
I_{DD1}	Current from V_{DD1}	2.1	3.0	mA		
I_{DD2}	Current from V_{DD2}	20	26.0	mA		
P_{D2}	Power Dissipation	530	689	mW		
	Power Per Driver	132	172	mW		

A.C. Characteristics $T_A = 0°$ to $75°C$, $V_{CC} = 5.0V \pm 5\%$, $V_{DD1} = 12V \pm 5\%$, $V_{DD2} = V_{DD1} + (3V \pm 5\%)$

Symbol	Parameter	Min.[1]	Typ.[2]	Max.[3]	Unit	Test Conditions
t_{-+}	Input to Output Delay	5	11		ns	
t_{DR}	Delay Plus Rise Time		20	32	ns	
t_{+-}	Input to Output Delay	3	8		ns	
t_{DF}	Delay Plus Fall Time		19	32	ns	

NOTES: 1. $C_L = 150pF$ (minimum C_L for 9 4K RAMs).
2. $C_L = 200pF$ (typical C_L for 9 4K RAMs). Typical values measured at $T_A = 25°C$.
3. $C_L = 250pF$ (maximum C_L for 9 4K RAMs).

Capacitance* $T_A = 25°C$

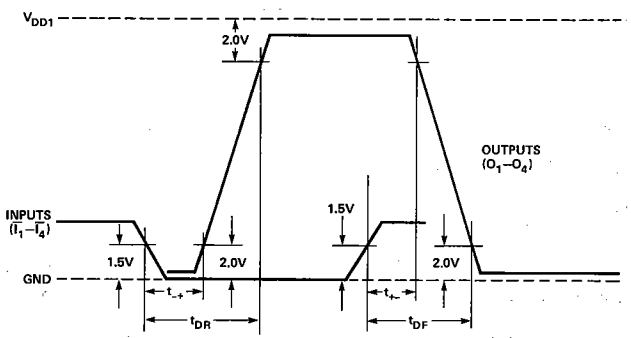
Symbol	Test	Typ.	Max.
C_{IN}	Input Capacitance, $\overline{I}_1, \overline{I}_2, \overline{I}_3, \overline{I}_4$	4.5pF	7
C_{IN}	Input Capacitance, $\overline{R}, \overline{C}, \overline{E}_1, \overline{E}_2$	8pF	12

*This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, $V_{bias} = 2V$, $V_{CC} = 0V$, and $T_A = 25°C$.

A.C. CONDITIONS OF TEST

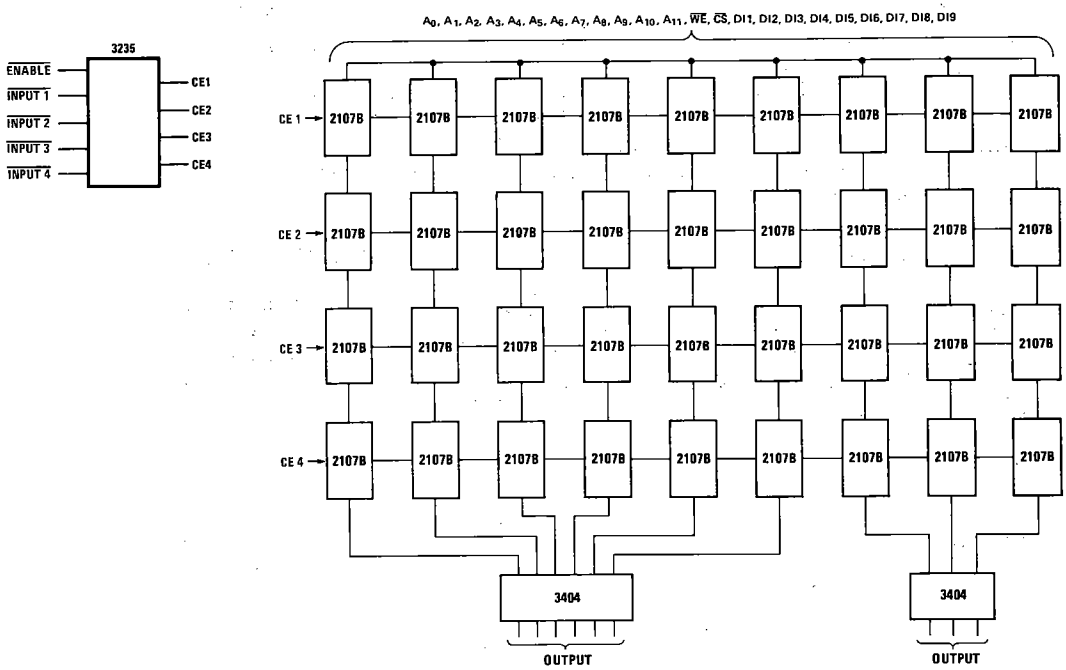
Input Pulse Amplitudes: 3.0V
Input Pulse Rise and Fall Times: 5 ns between 1 volt and 2 volts
Measurement Points: See Waveforms

Waveforms



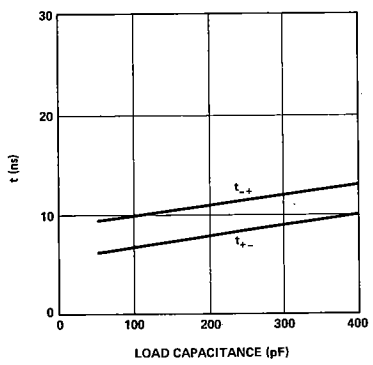
Typical System

Below is an example of a 16K x 9 bit memory circuit employing the 3235 quad high voltage driver for the chip enable inputs. A single 3235 package will drive this 16K x 9 bit memory array.



Typical Characteristics

INPUT TO OUTPUT DELAY
VS. LOAD CAPACITANCE



DELAY PLUS TRANSITION TIME
VS. LOAD CAPACITANCE