4 BIT PARALLEL BI-DIRECTIONAL BUS DRIVER

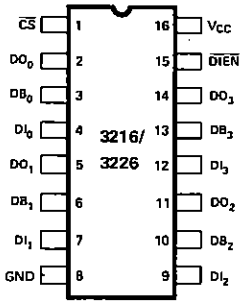
- **Data Bus Buffer Driver**
- **Low Input Load Current: .25mA Maximum**
- **High Output Drive Capability for Driving System Data Bus**
- **3.65V Output High Voltage**
- **Three-State Outputs**
- **Reduces System Package Count**

The 3216/3226 is a 4-bit bi-directional bus driver/receiver.

All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.65V V_{OH}, and for high capacitance terminated bus structures, the DB outputs provide a high 50mA I_{OL} capability.

A non-inverting (3216) and an inverting (3226) are available to meet a wide variety of applications for buffering in microcomputer systems.

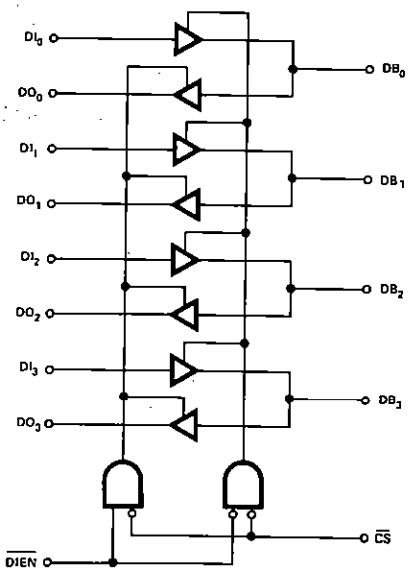
PIN CONFIGURATION



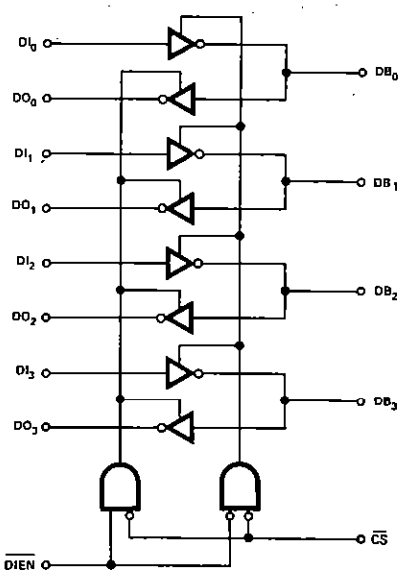
PIN NAMES

DB_0-DB_3	DATA BUS BI-DIRECTIONAL
DI_0-DI_3	DATA INPUT
DO_0-DO_3	DATA OUTPUT
$\overline{DIEN}$	DATA IN ENABLE DIRECTION CONTROL
$\overline{CS}$	CHIP SELECT

LOGIC DIAGRAM
3216



LOGIC DIAGRAM
3226



Functional Description

The 3216/3226 is a four bit bi-directional bus driver specifically designed to buffer microcomputer system components.

Bi-Directional Driver

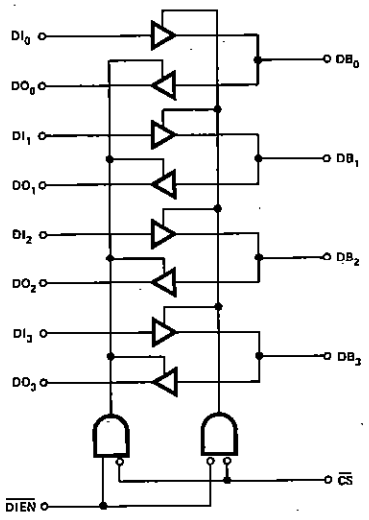
Each buffered line of the four bit driver consists of two separate buffers that are tri-state in nature to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this side is used to interface to the system side components such as memories, I/O, etc., because its interface is direct TTL compatible and it has high drive (50mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bi-directional bus.

Control Gating $\overline{DIEN}$, $\overline{CS}$

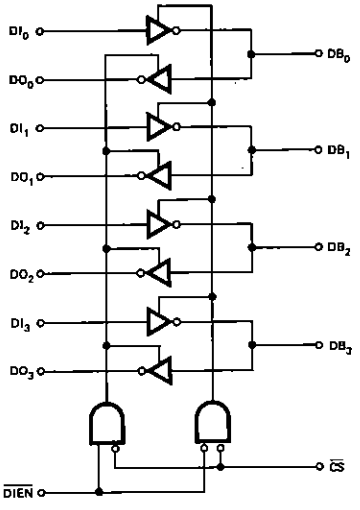
The $\overline{CS}$ input is actually a device select. When it is "high" the output drivers are all forced to their high-impedance state. When it is at "zero" the device is selected (enabled) and the direction of the data flow is determined by the $\overline{DIEN}$ input.

The $\overline{DIEN}$ input controls the direction of data flow (see Figure 1 for complete truth table). This direction control is accomplished by forcing one of the pair of buffers into its high impedance state and allowing the other to transmit its data. A simple two gate circuit is used for this function.

The 3216/3226 is a device that will reduce component count in microcomputer systems and at the same time enhance noise immunity to assure reliable, high performance operation.



(a) 3216



(b) 3226

$\overline{DIEN}$	$\overline{CS}$	
0	0	DI → DB
1	0	DB → DO
0	1	HIGH IMPEDANCE
1	1	

Figure 1. 3216/3226 Logic Diagrams

Absolute Maximum Ratings*

Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
All Output and Supply Voltages . . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V
Output Currents . . . . . 125 mA

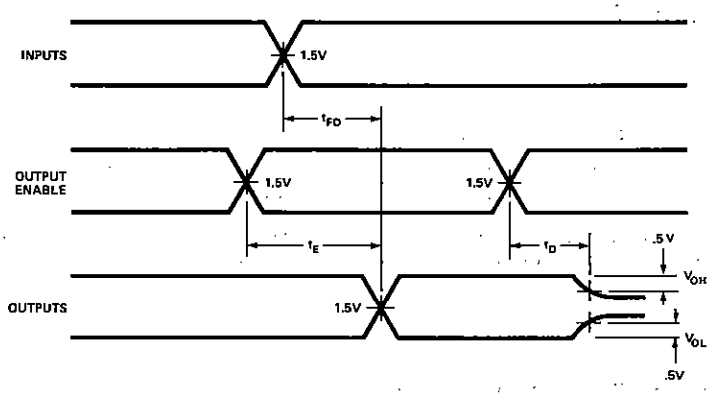
*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics $T_A = 0°C$ to $+70°C, V_{CC}=+5V \pm 5\%$

Symbol	Parameter	Limits Min.	Typ.	Max.	Unit	Conditions
I_{F1}	Input Load Current $\overline{DIEN}$, $\overline{CS}$		-0.15	-.5	mA	$V_F = 0.45$
I_{F2}	Input Load Current All Other Inputs		-0.08	-.25	mA	$V_F = 0.45$
I_{R1}	Input Leakage Current $\overline{DIEN}$, $\overline{CS}$			20	μA	$V_R = 5.25V$
I_{R2}	Input Leakage Current DI Inputs			10	μA	$V_R = 5.25V$
V_C	Input Forward Voltage Clamp			-1	V	$I_C = -5mA$
V_{IL}	Input "Low" Voltage			.95	V	
V_{IH}	Input "High" Voltage	2.0			V	
$\|I_O\|$	Output Leakage Current (3-State) DO DB			20 100	μA	$V_O = 0.45V/5.25V$
I_{CC}	Power Supply Current 3216		95	130	mA	
	3226		85	120	mA	
V_{OL1}	Output "Low" Voltage		0.3	.45	V	DO Outputs $I_{OL}=15mA$ DB Outputs $I_{OL}=25mA$
V_{OL2}	Output "Low" Voltage 3216		0.5	.6	V	DB Outputs $I_{OL}=55mA$
	3226		0.5	.6	V	DB Outputs $I_{OL}=50mA$
V_{OH1}	Output "High" Voltage	3.65	4.0		V	DO Outputs $I_{OH} = -1mA$
V_{OH2}	Output "High" Voltage	2.4	3.0		V	DB Outputs $I_{OH} = -10mA$
I_{OS}	Output Short Circuit Current	-15 -30	-35 -75	-65 -120	mA mA	DO Outputs $V_O \cong 0V$, DB Outputs $V_{CC}=5.0V$

NOTE: Typical values are for $T_A = 25°C$, $V_{CC} = 5.0V$.

Waveforms



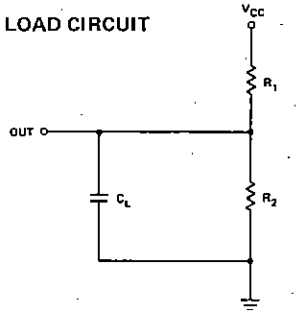
A.C. Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Conditions
T_{PD1}	Input to Output Delay DO Outputs		15	25	ns	C_L=30pF, R_1=300Ω, R_2=600Ω
T_{PD2}	Input to Output Delay DB Outputs					
	3216		20	30	ns	C_L=300pF, R_1=90Ω
	3226		16	25	ns	R_2 = 180Ω
T_E	Output Enable Time					
	3216		45	65	ns	(Note 2)
	3226		35	54	ns	(Note 3)
T_D	Output Disable Time		20	35	ns	(Note 4)

TEST CONDITIONS:

Input pulse amplitude of 2.5V.
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 5 mA and 10 pF.
Speed measurements are made at 1.5 volt levels.

TEST LOAD CIRCUIT



Capacitance[5]

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit
C_{IN}	Input Capacitance		4	8	pF
C_{OUT1}	Output Capacitance		6	10	pF
C_{OUT2}	Output Capacitance		13	18	pF

TEST CONDITIONS: $V_{BIAS} = 2.5V$, $V_{CC} = 5.0V$, $T_A = 25°C$, f = 1 MHz.

NOTES:
1. Typical values are for $T_A = 25°C$, $V_{CC} = 5.0V$.
2. DO Outputs, C_L = 30pF, R_1 = 300/10 KΩ, R_2 = 180/1KΩ; DB Outputs, C_L = 300pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.
3. DO Outputs, C_L = 30pF, R_1 = 300/10 KΩ, R_2 = 600/1K; DB Outputs, C_L = 300pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.
4. DO Outputs, C_L = 5pF, R_1 = 300/10 KΩ, R_2 = 600/1 KΩ; DB Outputs, C_L = 5pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.
5. This parameter is periodically sampled and not 100% tested.