



# 3212

## MULTI-MODE LATCH BUFFER

The INTEL® 3212 Multi-Mode Latch Buffer is a versatile 8-bit latch with three-state output buffers and built-in device select logic. It also contains an independent service request flip-flop for the generation of central processor interrupts. Because of its multi-mode capabilities, one or more 3212's can be used to implement many types of interface and support systems for Series 3000 computing elements including:

- Simple data latches
- Gated data buffers
- Multiplexers
- Bi-directional bus drivers
- Interrupting input/output ports

High Performance – 50 ns Write Cycle Time

Low Input Load Current – 250  $\mu$ A Maximum

Three-State Fully Buffered Outputs

High Output Drive Capability

Independent Service Request Flip-Flop

Asynchronous Data Latch Clear

24 Pin DIP

### PACKAGE CONFIGURATION

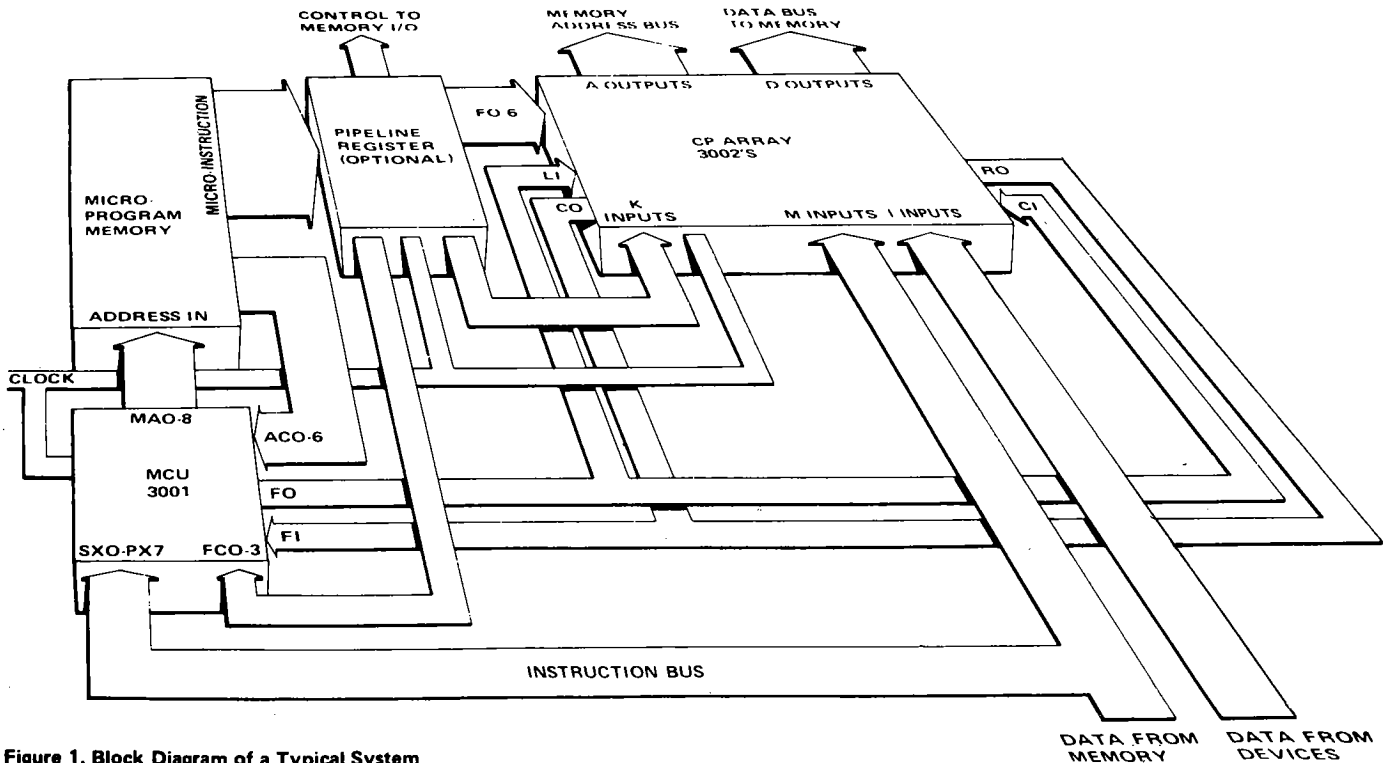
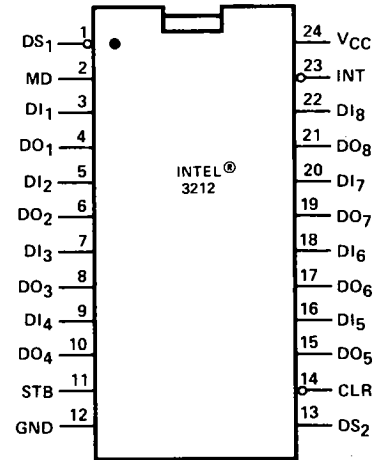


Figure 1. Block Diagram of a Typical System

## PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE <sup>(1)</sup>
1	DS <sub>1</sub>	Device Select Input 1	active LOW
2	MD	Mode Input When MD is high (output mode) the output buffers are enabled and the write signal to the data latches is obtained from the device select logic. When MD is low (input mode) the output buffer state is determined by the device select logic and the write signal is obtained from the strobe (STB) input.	
3, 5, 7, 9, 16, 18, 20, 22	DI <sub>1</sub> –DI <sub>8</sub>	Data Inputs The data inputs are connected to the D-inputs of the data latches.	
4, 6, 8, 10, 15, 17, 19, 21	DO <sub>1</sub> –DO <sub>8</sub>	Data Outputs The data outputs are the buffered outputs of the eight data latches.	three-state
11	STB	Strobe Input When MD is in the LOW state, the STB input provides the clock input to the data latch.	
12	GND	Ground	
13	DS <sub>2</sub>	Device Select Input 2 When DS <sub>1</sub> is low and DS <sub>2</sub> is high, the device is selected.	
14	CLR	Clear	active LOW
23	INT	Interrupt Output The interrupt output will be active LOW (interrupting state) when either the service request flip-flop is low or the device is selected.	active LOW

## NOTE:

(1) Active HIGH, unless otherwise specified.

## FUNCTIONAL DESCRIPTION

The 3212 contains eight D-type data latches, eight three-state output buffers, a separate D-type service request flip-flop, and a flexible device select/mode control section.

### DATA LATCHES

The Q-output of each data latch will follow the data on its corresponding data input line ( $DI_1$ – $DI_8$ ) while its clock input is high. Data will be latched when the internal write line WR is brought low. The output of each data latch is connected to a three-state, non-inverting output buffer. The internal enable line EN is bussed to each buffer. When the EN is high, the buffers are enabled and the data in each latch is available on its corresponding data output line ( $DO_0$ – $DO_8$ ).

### DEVICE SELECT LOGIC

Two input lines  $DS_1$  and  $DS_2$  are provided for device selection. When  $DS_1$  is low and  $DS_2$  is high, the 3212 is selected.

### MODE CONTROL SECTION

The 3212 may be operated in two modes. When the mode input line MD is low, the device is in the input mode. In this mode, the output buffers are enabled whenever the 3212 is selected; the internal WR line follows the STB input line.

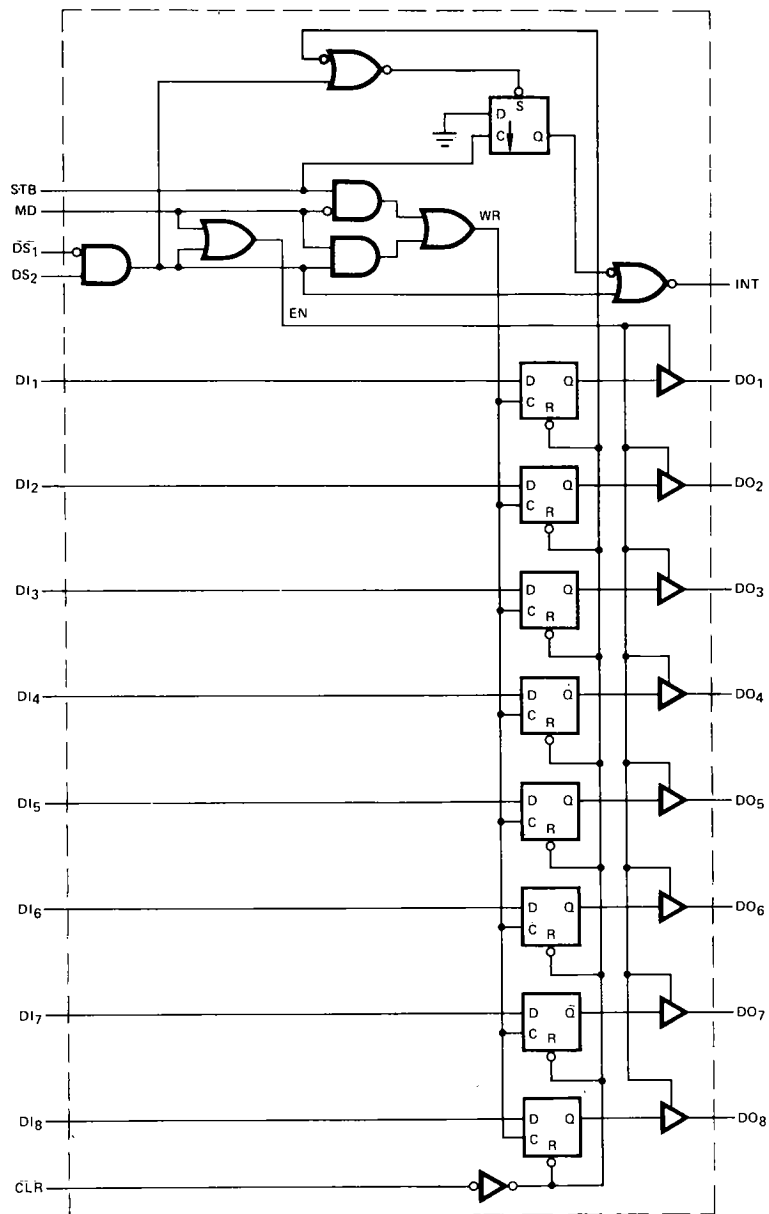
When MD is high, the device is in the output mode and, as a result, the output buffers are enabled. In this mode, the write signal for the data latch is obtained from the device select logic.

### SERVICE REQUEST FLIP-FLOP AND STROBE

The service request flip-flop SR is used to generate and control central processor interrupt signals. For system reset, the SR flip-flop is placed in the non-interrupting state (i.e., SR is set) by bringing the CLR line low. This simultaneously clears (resets) the 8-bit data latch.

The Q output of the SR flip-flop is logically ORed with the output of device select logic and then inverted to provide the interrupt output INT. The 3212 is considered to be in the interrupting state when the INT output is low. This allows direct connection to the active LOW priority request inputs of the INTEL®3214 Interrupt Control Unit.

When operated in the input mode (i.e., MD low) the strobe input STB is used to synchronously write data into the data latch and place the SR flip-flop in the interrupting (reset) state. The interrupt is removed by the central processor when the interrupting 3212 is selected.



M3212 Logic Diagram

## D.C. AND OPERATING CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias . . . . .	0°C to 70°C
Storage Temperature . . . . .	-65°C to +160°C
All Output and Supply Voltages. . . . .	-0.5V to +7V
All Input Voltages. . . . .	-1.0V to +5.5V
Output Currents . . . . .	100 mA

\**COMMENT:* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

$T_A = 0^\circ\text{C to } +75^\circ\text{C}$      $V_{CC} = +5\text{V} \pm 5\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$I_F$	Input Load Current STB, DS <sub>2</sub> , CLR, DI <sub>1</sub> -DI <sub>8</sub> Inputs			-0.25	mA	$V_F = .45\text{V}$
$I_F$	Input Load Current MD Input			-0.75	mA	$V_F = .45\text{V}$
$I_F$	Input Load Current DS <sub>1</sub> Input			-1.0	mA	$V_F = .45\text{V}$
$I_R$	Input Leakage Current STB, DS, CLR, DI <sub>1</sub> -DI <sub>8</sub> Inputs			10	μA	$V_R \leq V_{CC}$
$I_R$	Input Leakage Current MD Input			30	μA	$V_R \leq V_{CC}$
$I_R$	Input Leakage Current DS <sub>1</sub> Input			40	μA	$V_R \leq V_{CC}$
$V_C$	Input Forward Voltage Clamp			-1	V	$I_C = -5\text{ mA}$
$V_{IL}$	Input "Low" Voltage			.85	V	
$V_{IH}$	Input "High" Voltage	2.0			V	
$V_{OL}$	Output "Low" Voltage			.45	V	$I_{OL} = 15\text{ mA}$
$V_{OH}$	Output "High" Voltage	3.65	4.0		V	$I_{OH} = -1\text{ mA}$
$I_{SC}$	Short Circuit Output Current	-15		-75	mA	$V_{CC} = 5.0\text{V}$
$ I_O $	Output Leakage Current High Impedance State			20	μA	$V_O = .45\text{V}/5.25\text{V}$
$I_{CC}$	Power Supply Current		90	130	mA	

**A.C. CHARACTERISTICS**  $T_A = 0^\circ\text{C}$  to  $75^\circ\text{C}$ ,  $V_{CC} = +5.0\text{V} \pm 5\%$ 

Symbol	Parameter	Min.	Typ.	Max.	Unit	
$t_{PW}$	Pulse Width	25			ns	
$t_{PD}$	Data To Output Delay			30	ns	
$t_{WE}$	Write Enable To Output Delay			40	ns	
$t_{SET}$	Data Setup Time	15			ns	
$t_H$	Data Hold Time	20			ns	
$t_R$	Reset To Output Delay			40	ns	
$t_S$	Set To Output Delay			30	ns	
$t_E$	Output Enable Time			45	ns	$C_L = 30\text{ pF}$
$t_C$	Clear To Output Display			45	ns	

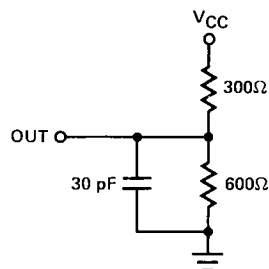
**TEST CONDITIONS:**

Input pulse amplitude of 2.5 volts.

Input rise and fall times of 5 ns between 1 volt and 2 volts.

Output load of 15 mA and 30 pF.

Speed measurements are taken at the 1.5 volt level.

**TEST LOAD CIRCUIT:****CAPACITANCE<sup>(1)</sup>**

Symbol	Test	LIMITS			Units
		Min.	Typ.	Max.	
$C_{IN}$	$DS_1$ , MD Input Capacitance		9	12	pf
$C_{IN}$	$DS_2$ , CLR, STB, $DI_1-DI_8$ Input Capacitance		5	9	pf
$C_{OUT}$	$DO_1-DO_8$ Output Capacitance		8	12	pf

**NOTE:**

(1) This parameter is periodically sampled and is not 100% tested. Condition of measurement is  $f = 1\text{ MHz}$ ,  $V_{BIAS} = 2.5\text{V}$ ,  $V_{CC} = 5\text{V}$  and  $T_A = 25^\circ\text{C}$ .

## D.C. AND OPERATING CHARACTERISTICS

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias . . . . .	-55°C to +125°C
Storage Temperature . . . . .	-65°C to +160°C
All Input and Supply Voltages . . . . .	-0.5V to +7V
All Input Voltages . . . . .	-1.0V to +5.5V
Output Currents . . . . .	100 mA

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

$T_A = -55^\circ\text{C to } +125^\circ\text{C}; V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$I_F$	Input Load Current STB, DS <sub>2</sub> , CLR, DI <sub>1</sub> -DI <sub>8</sub> Inputs			-.25	mA	$V_F = .45\text{V}$
$I_F$	Input Load Current MD Input			-.75	mA	$V_F = .45\text{V}$
$I_F$	Input Load Current DS <sub>1</sub> Input			-1.0	mA	$V_F = .45\text{V}$
$I_R$	Input Leakage Current STB, DS, CLR, DI <sub>1</sub> -DI <sub>8</sub> Inputs			10	$\mu\text{A}$	$V_R \leq V_{CC}$
$I_R$	Input Leakage Current MD Input			30	$\mu\text{A}$	$V_R \leq V_{CC}$
$I_R$	Input Leakage Current DS <sub>1</sub> Input			40	$\mu\text{A}$	$V_R \leq V_{CC}$
$V_C$	Input Forward Voltage Clamp			1.2	V	$I_C = -5\text{ mA}$
$V_{IL}$	Input "Low" Voltage			.80	V	
$V_{IH}$	Input "High" Voltage	2.0			V	
$V_{OL}$	Output "Low" Voltage			.45	V	$I_{OL} = 10\text{ mA}$
$V_{OH}$	Output "High" Voltage	3.5	4.0		V	$I_{OH} = .5\text{ mA}$
$I_{SC}$	Short Circuit Output Current	-15		-75	mA	$V_{CC} = 5.0\text{V}$
$ I_O $	Output Leakage Current High Impedance State			20	$\mu\text{A}$	$V_O = .45\text{V}/5.5\text{V}$
$I_{CC}$	Power Supply Current		90	145	mA	

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$t_{WE}$	Write Enable To Output Delay			50	ns
$t_{SET}$	Data Setup Time	20			ns
$t_H$	Data Hold Time	30			ns
$t_R$	Reset To Output Delay			55	ns
$t_S$	Set To Output Delay			35	ns
$t_E$	Output Enable Time			50	ns
$t_C$	Clear To Output Display			55	ns

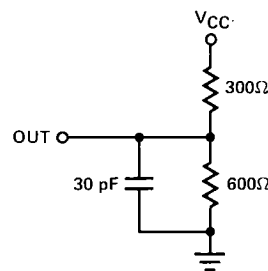
 $C_L = 30\text{ pf}$ **TEST CONDITIONS:**

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$C_{OUT}$	$DO_1$ – $DO_8$ Output Capacitance		8	12	pf

**NOTE:**(1) This parameter is periodically sampled and is not 100% tested. Condition of measurement is  $f = 1\text{ MHz}$ ,  $V_{BIAS} = 2.5\text{V}$ ,  $V_{CC} = 5\text{V}$  and  $T_A = 25^\circ\text{C}$ .

WAVEFORMS

