

SERIES 3000 BIPOLAR MICROPROCESSOR

INTRODUCTION

Since its introduction, the Series 3000 family of computing elements has found acceptance in a wide range of high performance applications from disk controllers to airborne central processors. The Series 3000 offers the flexibility, performance, and system integration necessary for an effective system solution for both high speed controllers and central processors.

The entire 3000 family is available in commercial and military temperature range versions. In addition to the components, Intel has also developed a comprehensive support system to assist the user in writing microprograms, debugging hardware and microcode, and programming PROMs for both prototype and production systems.

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3001

MICROPROGRAM CONTROL UNIT

The INTEL® 3001 Microprogram Control Unit (MCU) controls the sequence in which microinstructions are fetched from the microprogram memory. Its functions include the following:

Maintenance of the microprogram address register.

Selection of the next microinstruction based on the contents of the microprogram address register.

Decoding and testing of data supplied via several input busses to determine the microinstruction execution sequence.

Saving and testing of carry output data from the central processor (CP) array.

Control of carry/shift input data to the CP array.

Control of microprogram interrupts.

High Performance — 85 ns Cycle Time

TTL and DTL Compatible

Fully Buffered Three-State and Open Collector Outputs

Direct Addressing of Standard Bipolar PROM or ROM

512 Microinstruction Addressability

Advanced Organization

9-Bit Microprogram Address Register and Bus

4-Bit Program Latch

Two Flag Registers

Eleven Address Control Functions

Three Jump and Test Latch Functions

16-way Jump and Test Instruction Bus Function

Eight Flag Control Functions

Four Flag Input Functions

Four Flag Output Functions

40 Pin DIP

PACKAGE CONFIGURATION

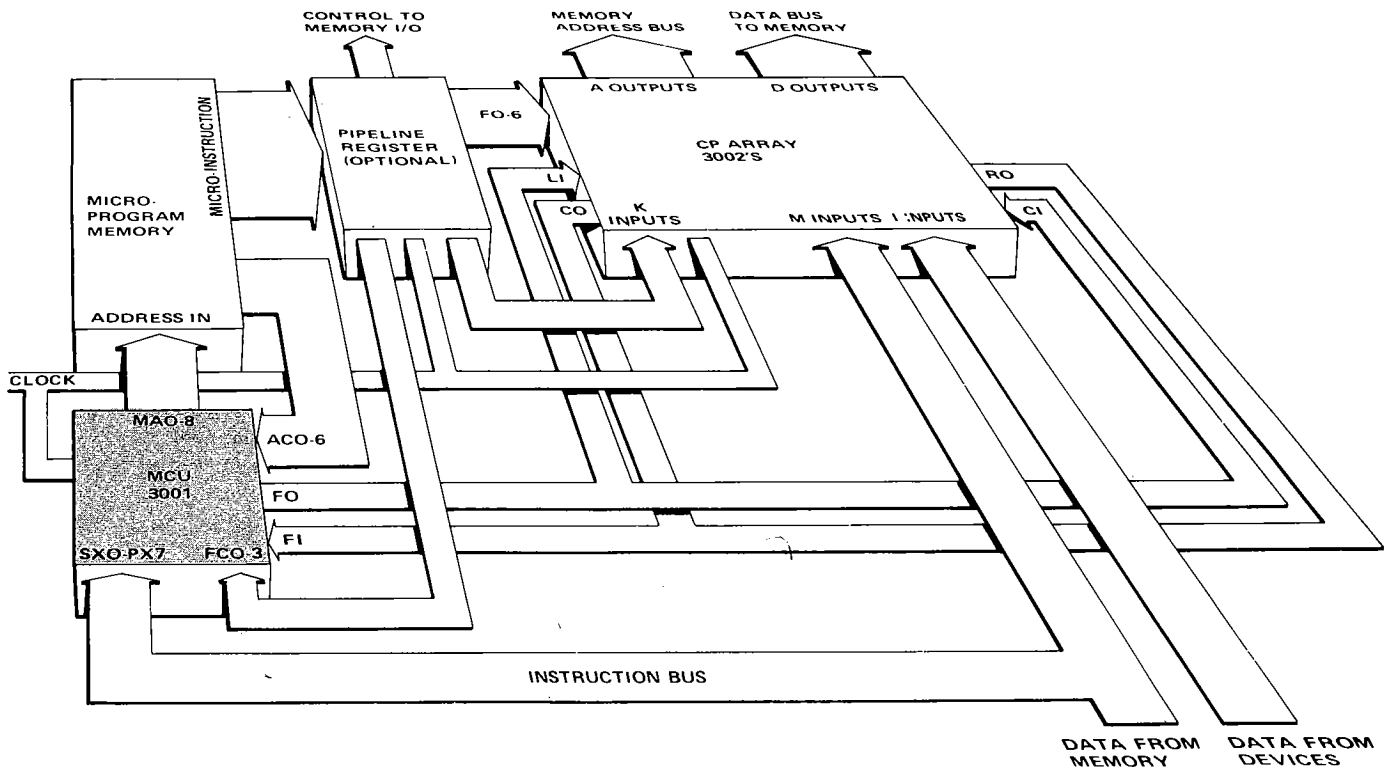
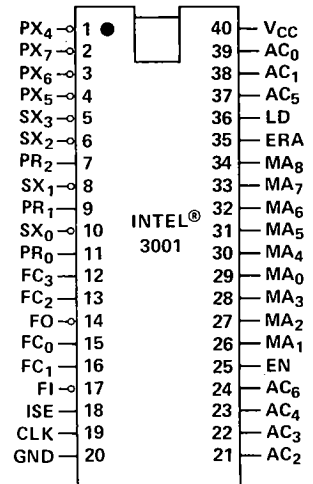


Figure 1. Block Diagram of a Typical System

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE ⁽¹⁾
1-4	PX ₄ -PX ₇	Primary Instruction Bus Inputs Data on the primary instruction bus is tested by the JPX function to determine the next microprogram address.	active LOW
5, 6, 8, 10	SX ₀ -SX ₃	Secondary Instruction Bus Inputs Data on the secondary instruction bus is synchronously loaded into the PR-latch while the data on the PX-bus is being tested (JPX). During a subsequent cycle, the contents of the PR-latch may be tested by the JPR, JLL, or JRL functions to determine the next microprogram address.	active LOW
7, 9, 11	PR ₀ -PR ₂	PR-Latch Outputs The PR-latch outputs are asynchronously enabled by the JCE function. They can be used to modify microinstructions at the outputs of the microprogram memory or to provide additional control lines.	open collector
12, 13, 15, 16	FC ₀ -FC ₃	Flag Logic Control Inputs The flag logic control inputs are used to cross-switch the flags (C and Z) with the flag logic input (FI) and the flag logic output (FO).	
14	FO	Flag Logic Output The outputs of the flags (C and Z) are multiplexed internally to form the common flag logic output. The output may also be forced to a logical 0 or logical 1.	active LOW three-state
17	FI	Flag Logic Input The flag logic input is demultiplexed internally and applied to the inputs of the flags (C and Z). Note: the flag input data is saved in the F-latch when the clock input (CLK) is low.	active LOW
18	ISE	Interrupt Strobe Enable Output The interrupt strobe enable output goes to logical 1 when one of the JZR functions are selected (see Functional Description, page 6). It can be used to provide the strobe signal required by the INTEL 3214 Priority Interrupt Control Unit or other interrupt circuits.	
19	CLK	Clock Input	
20	GND	Ground	
21-24 37-39	AC ₀ -AC ₆	Next Address Control Function Inputs All jump functions are selected by these control lines.	
25	EN	Enable Input When in the HIGH state, the enable input enables the microprogram address, PR-latch and flag outputs.	
26-29	MA ₀ -MA ₃	Microprogram Column Address Outputs	three-state
30-34	MA ₄ -MA ₈	Microprogram Row Address Outputs	three-state
35	ERA	Enable Row Address Input When in the LOW state, the enable row address input independently disables the microprogram row address outputs. It can be used with the INTEL 3214 Priority Interrupt Control Unit or other interrupt circuits to facilitate the implementation of priority interrupt systems.	
36	LD	Microprogram Address Load Input When in the active HIGH state, the microprogram address load input inhibits all jump functions and synchronously loads the data on the instruction busses into the microprogram register. However, it does not inhibit the operation of the PR-latch or the generation of the interrupt strobe enable.	
40	VCC	+5 Volt Supply	

NOTE:

(1) Active HIGH unless otherwise specified.

LOGICAL DESCRIPTION

The MCU performs two major control functions. First, it controls the sequence in which microinstructions are fetched from the microprogram memory. For this purpose, the MCU contains a microprogram address register and the associated logic for selecting the next microinstruction address. The second function of the MCU is the control of the two flag flip-flops that are included for interaction with the carry input and carry output logic of the CP array. The logical organization of the MCU is shown in Figure 2.

NEXT ADDRESS LOGIC

The next address logic of the MCU provides a set of conditional and unconditional address control functions. These address control functions are used to implement a jump or jump/test operation as part of every microinstruction. That is to say, each microinstruction typically contains a jump operation field that specifies the address control function, and hence, the next microprogram address.

In order to minimize the pin count of the MCU, and reduce the complexity of the next address logic, the microprogram address space is organized as a two dimensional array or matrix. Each microprogram address corresponds to a unit of the matrix at a particular row and column location. Thus, the 9-bit microprogram address is treated as specifying not one, but two addresses — the row address in the upper five bits and the column address in the lower four bits. The address matrix can therefore contain, at most, 32 row addresses and 16 column addresses for a total of 512 microinstructions.

The next address logic of the MCU makes extensive use of this two component addressing scheme. For example, from a particular row or column address, it is possible to jump unconditionally in one operation anywhere in that row or column. It is not possible, however, to jump anywhere in the address matrix. In fact, for a given location in the matrix, there is a fixed subset of microprogram addresses that may be selected as the next address. These

possible jump target addresses are referred to as a jump set. Each type of MCU address control (jump) function has a jump set associated with it. Appendix C illustrates the jump set for each function.

FLAG LOGIC

The flag logic of the MCU provides a set of functions for saving the current value of the carry output of the CP array and for controlling the value of the carry input to the CP array. These two distinct flag control functions are called flag input functions and flag output functions.

The flag logic is comprised of two flip-flops, designated the C-flag and the Z-flag, along with a simple latch, called the F-latch, that indicates the current state of the carry output line of the CP array. The flag logic is used in conjunction with the carry and shift logic of the CP array to implement a variety of shift/rotate and arithmetic functions.

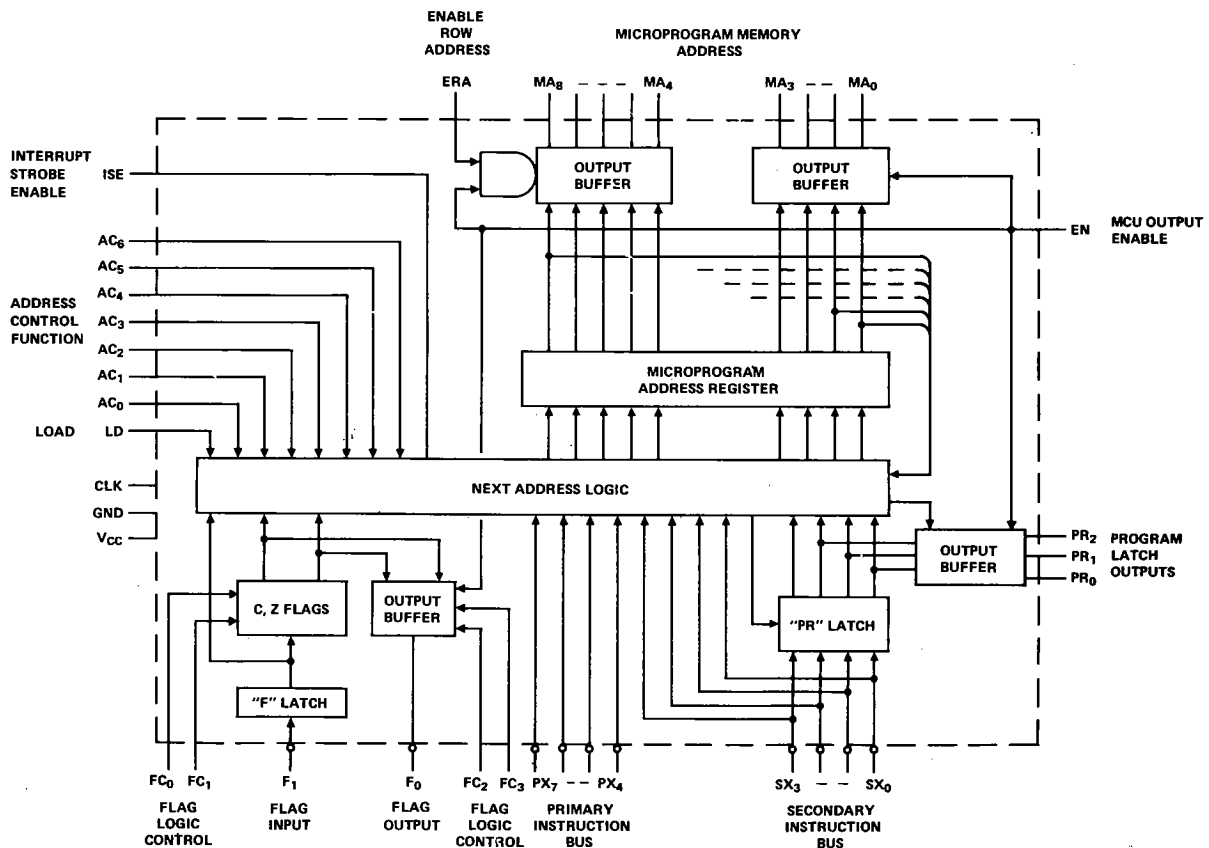


Figure 2. 3001 Block Diagram

FUNCTIONAL DESCRIPTION

ADDRESS CONTROL FUNCTIONS

The address control functions of the MCU are selected by the seven input lines designated AC₀-AC₆. On the rising edge of the clock, the 9-bit microprogram address generated by the next address logic is loaded into the microprogram address register. The next microprogram address is delivered to the microprogram memory via the nine output lines designated MA₀-MA₈. The microprogram address outputs are organized into row and column addresses as:

$$\begin{array}{c} \underline{MA_8 \ MA_7 \ MA_6 \ MA_5 \ MA_4} \\ \text{row address} \\ \\ \underline{MA_3 \ MA_2 \ MA_1 \ MA_0} \\ \text{column address} \end{array}$$

Each address control function is specified by a unique encoding of the data on the function input lines. From three to five bits of the data specify the particular function while the remaining bits are used to select part of either the row or column address desired. Function code formats are given in Appendix A, "Address Control Function Summary."

The following is a detailed description of each of the eleven address control functions. The symbols shown below are used throughout the description to specify row and column addresses.

Symbol	Meaning
row _n	5-bit next row address where n is the decimal row address.
col _n	4-bit next column address where n is the decimal column address.

UNCONDITIONAL ADDRESS CONTROL (JUMP) FUNCTIONS

The jump functions use the current microprogram address (i.e., the contents of the microprogram address register prior to the rising edge of the clock) and several bits from the address control inputs to generate the next microprogram address.

Mnemonic	Function Description
JCC	Jump in current column. AC ₀ -AC ₄ are used to select 1 of 32 row addresses in the current column, specified by

MA₀-MA₃, as the next address

JZR	Jump to zero row. AC ₀ -AC ₃ are used to select 1 of 16 column addresses in row ₀ , as the next address.
JCR	Jump in current row. AC ₀ -AC ₃ are used to select 1 of 16 addresses in the current row, specified by MA ₄ -MA ₈ , as the next address.
JCE	Jump in current column/row group and enable PR-latch outputs. AC ₀ -AC ₂ are used to select 1 of 8 row addresses in the current row group, specified by MA ₇ -MA ₈ , as the next row address. The current column is specified by MA ₀ -MA ₃ . The PR-latch outputs are asynchronously enabled.

FLAG CONDITIONAL ADDRESS CONTROL (JUMP/TEST) FUNCTIONS

The jump/test flag functions use the current microprogram address, the contents of the selected flag or latch, and several bits from the address control function to generate the next microprogram address.

Mnemonic	Function Description
JFL	Jump/test F-Latch. AC ₀ -AC ₃ are used to select 1 of 16 row addresses in the current row group, specified by MA ₈ , as the next row address. If the current column group, specified by MA ₃ , is col ₀ -col ₇ , the F-latch is used to select col ₂ or col ₃ as the next column address. If MA ₃ specifies column group col ₈ -col ₁₅ , the F-latch is used to select col ₁₀ or col ₁₁ as the next column address.
JCF	Jump/test C-flag. AC ₀ -AC ₂ are used to select 1 of 8 row addresses in the current

row group, specified by MA₇ and MA₈, as the next row address. If the current column group specified by MA₃ is col₀-col₇, the C-flag is used to select col₂ or col₃ as the next column address. If MA₃ specifies column group col₈-col₁₅, the C-flag is used to select col₁₀ or col₁₁ as the next column address.

JZF	Jump/test Z-flag. Identical to the JCF function described above, except that the Z-flag, rather than the C-flag, is used to select the next column address.
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PX-BUS AND PR-LATCH CONDITIONAL ADDRESS CONTROL (JUMP/TEST) FUNCTIONS

The PX-bus jump/test function uses the data on the primary instruction bus (PX₄-PX₇), the current microprogram address, and several selection bits from the address control function to generate the next microprogram address. The PR-latch jump/test functions use the data held in the PR-latch, the current microprogram address, and several selection bits from the address control function to generate the next microprogram address.

Mnemonic	Function Description
JPR	Jump/test PR-latch. AC ₀ -AC ₂ are used to select 1 of 8 row addresses in the current row group, specified by MA ₇ and MA ₈ , as the next row address. The four PR-latch bits are used to select 1 of 16 possible column addresses as the next column address.
JLL	Jump/test leftmost PR-latch bits. AC ₀ -AC ₂ are used to select 1 of 8 row addresses in the current row group, specified by MA ₇ and MA ₈ , as the next row address. PR ₂ and PR ₃ are used to

FUNCTIONAL DESCRIPTION (con't)

	select 1 of 4 possible column addresses in col ₄ through col ₇ as the next column address.
JRL	Jump/test rightmost PR-latch bits. AC ₀ and AC ₁ are used to select 1 of 4 high-order row addresses in the current row group, specified by MA ₇ and MA ₈ , as the next row address. PR ₀ and PR ₁ are used to select 1 of 4 possible column addresses in col ₁₂ through col ₁₅ as the next column address.
JPX	Jump/test PX-bus and load PR-latch. AC ₀ and AC ₁ are used to select 1 of 4 row addresses in the current row group, specified by MA ₆ -MA ₈ , as the next row address. PX ₄ -PX ₇ are used to select 1 of 16 possible column addresses as the next column address. SX ₀ -SX ₃ data is locked in the PR-latch at the rising edge of the clock.

FLAG CONTROL FUNCTIONS

The flag control functions of the MCU are selected by the four input lines designated FC₀-FC₃. Function code formats are given in Appendix B, "Flag Control Function Summary."

The following is a detailed description of each of the eight flag control functions.

FLAG INPUT CONTROL FUNCTIONS

The flag input control functions select which flag or flags will be set to the current value of the flag input (FI) line. Data on FI is stored in the F-latch when the clock is low. The content of the F-latch is loaded into the C and/or Z flag on the rising edge of the clock.

Mnemonic	Function Description
SCZ	Set C-flag and Z-flag to FI. The C-flag and the Z-flag are both set to the value of FI.
STZ	Set Z-flag to FI. The Z-flag is set to the value of FI. The C-flag is unaffected.
STC	Set C-flag to FI. The C-flag is set to the value of FI. The Z flag is unaffected.
HCZ	Hold C-flag and Z-flag. The values in the C-flag and Z-flag are unaffected.

FLAG OUTPUT CONTROL FUNCTIONS

The flag output control functions select the value to which the flag output (FO) line will be forced.

Mnemonic	Function Description
FF0	Force FO to 0. FO is forced to the value of logical 0.
FFC	Force FO to C. FO is forced to the value of the C-flag.
FFZ	Force FO to Z. FO is forced to the value of the Z-flag.
FF1	Force FO to 1. FO is forced to the value of logical 1.

LOAD AND INTERRUPT STROBE FUNCTIONS

The load function of the MCU is controlled by the input line designated LD. If the LD line is active HIGH at the rising edge of the clock, the data on the primary and secondary instruction busses, PX₄-PX₇ and SX₀-SX₃, is loaded into the microprogram address register. PX₄-PX₇ are loaded into MA₀-MA₃ and SX₀-SX₃ are loaded into MA₄-MA₇. The high-order bit of the microprogram address register MA₈ is set to a logical 0. The bits from the primary instruction bus select 1 of 16 possible column addresses. Likewise, the bits from the secondary instruction bus select 1 of the first 16 row addresses.

The interrupt strobe enable of the MCU is available on the output line designated ISE. The line is placed in the active high state whenever a JZR to col₁₅ is selected as the address control function. Customarily, the start of a macroinstruction fetch sequence is situated at row₀ and col₁₅ so that the INTEL 3214 Priority Interrupt Control Unit may be enabled at the beginning of the fetch/execute cycle. The priority interrupt control unit may respond to the interrupt by pulling the enable row address (ERA) input line down to override the selected next row address from the MCU. Then by gating an alternative next row address on to the row address lines of the microprogram memory, the microprogram may be forced to enter an interrupt handling routine. The alternative row address placed on the microprogram memory address lines does not alter the contents of the microprogram address register. Therefore, subsequent jump functions will utilize the row address in the register, and not the alternative row address, to determine the next microprogram address.

Note, the load function always overrides the address control function on AC₀-AC₆. It does not, however, override the latch enable or load sub-functions of the JCE or JPX instruction, respectively. In addition, it does not inhibit the interrupt strobe enable or any of the flag control functions.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +160°C
All Output and Supply Voltages	-0.5V to +7V
All Input Voltages	-1.0V to +5.5V
Output Currents	100 mA

**COMMENT:* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

$T_A = 0^\circ\text{C to } 70^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 5\%$

SYMBOL	PARAMETER	MIN	TYP ⁽¹⁾	MAX	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		-0.8	-1.0	V	$I_C = -5\text{ mA}$
I_F	Input Load Current:					
	CLK Input		-0.075	-0.75	mA	$V_F = 0.45\text{V}$
	EN Input		-0.05	-0.50	mA	
	All Other Inputs		-0.025	-0.25	mA	
I_R	Input-Leakage Current:					
	CLK			120	μA	$V_R = 5.25\text{V}$
	EN Input			80	μA	
	All Other Inputs			40	μA	
V_{IL}	Input Low Voltage			0.8	V	$V_{CC} = 5.0\text{V}$
V_{IH}	Input High Voltage	2.0			V	
I_{CC}	Power Supply Current ⁽²⁾		170	240	mA	
V_{OL}	Output Low Voltage (All Output Pins)		0.35	0.45	V	$I_{OL} = 10\text{ mA}$
V_{OH}	Output High Voltage (MA ₀ -MA ₈ , ISE, FO)	2.4	3.0		V	$I_{OH} = -1\text{ mA}$
I_{OS}	Output Short Circuit Current (MA ₀ -MA ₈ , ISE, FO)	-15	-28	-60	mA	$V_{CC} = 5.0\text{V}$
$I_{O(off)}$	Off-State Output Current:					
	MA ₀ -MA ₈ , FO			-100	μA	$V_O = 0.45\text{V}$
	MA ₀ -MA ₈ , FO, PR ₀ -PR ₂			100	μA	$V_O = 5.25\text{V}$

NOTES:

- (1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.
 (2) EN input grounded, all other inputs and outputs open.

A.C. CHARACTERISTICS AND WAVEFORMS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5.0\text{V} \pm 5\%$

SYMBOL	PARAMETER	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{CY}	Cycle Time ⁽²⁾	85	60		ns
t_{WP}	Clock Pulse Width	30	20		ns
	Control and Data Input Set-Up Times:				
t_{SF}	LD, AC ₀ -AC ₆	10	0		ns
t_{SK}	FC ₀ , FC ₁	0			ns
t_{SX}	SX ₀ -SX ₃ , PX ₄ -PX ₇	35	25		ns
t_{SI}	FI	15	5		ns
	Control and Data Input Hold Times:				
t_{HF}	LD, AC ₀ -AC ₆	5	0		ns
t_{HK}	FC ₀ , FC ₁	0			ns
t_{HX}	SX ₀ -SX ₃ , PX ₄ -PX ₇	20	5		ns
t_{HI}	FI	20	8		ns
t_{CO}	Propagation Delay from Clock Input (CLK) to Outputs (MA ₀ -MA ₈ , FO)	10	30	45	ns
t_{KO}	Propagation Delay from Control Inputs FC ₂ and FC ₃ to Flag Out (FO)		16	30	ns
t_{FO}	Propagation Delay from Control Inputs AC ₀ -AC ₆ to Latch Outputs (PR ₀ -PR ₂)		26	40	ns
t_{EO}	Propagation Delay from Enable Inputs EN and ERA to Outputs (MA ₀ -MA ₈ , FO, PR ₀ -PR ₂)		21	32	ns
t_{FI}	Propagation Delay from Control Inputs AC ₀ -AC ₆ to Interrupt Strobe Enable Output (ISE)		24	40	ns

NOTE:

(1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.(2) $t_{CY} = t_{WP} + t_{SF} + t_{CO}$

TEST CONDITIONS:

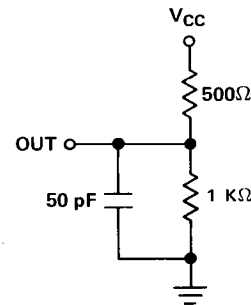
Input pulse amplitude of 2.5 volts.

Input rise and fall times of 5 ns between 1 volt and 2 volts.

Output load of 10 mA and 50 pF.

Speed measurements are taken at the 1.5 volt level.

TEST LOAD CIRCUIT:

CAPACITANCE⁽²⁾ $T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance:				
	CLK, EN		11	16	pF
	All Other Inputs		5	10	pF
C_{OUT}	Output Capacitance		6	12	pF

NOTE:

(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is $f = 1\text{ MHz}$, $V_{BIAS} = 2.5\text{V}$, $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +160°C
All Input and Supply Voltages	-0.5V to +7V
All Input Voltages	-1.0V to +5.5V
Output Currents	100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

SYMBOL	PARAMETER	MIN	TYP ⁽¹⁾	MAX	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		-0.8	-1.2	V	$I_C = -5\text{ mA}$
I_F	Input Load Current:					$V_F = 0.45\text{V}$
	CLK Input		-75	-750	μA	
	EN Input		-50	-500	μA	
	All Other Inputs		-25	-250	μA	
I_R	Input Leakage Current:					$V_R = 5.5\text{V}$
	CLK			120	μA	
	EN Input			80	μA	
	All Other Inputs			40	μA	
V_{IL}	Input Low Voltage			0.8	V	$V_{CC} = 5.0\text{V}$
V_{IH}	Input High Voltage	2.0			V	
I_{CC}	Power Supply Current ⁽²⁾		170	250	mA	
V_{OL}	Output Low Voltage (All Output Pins)		0.35	0.45	V	$I_{OL} = 10\text{ mA}$
V_{OH}	Output High Voltage (MA ₀ -MA ₈ , ISE, FO)	2.4	3.0		V	$I_{OH} = -1\text{ mA}$
I_{OS}	Output Short Circuit Current (MA ₀ -MA ₈ , ISE, FO)	-15	-28	-60	mA	$V_{CC} = 5.0\text{V}$
$I_{O(\text{off})}$	Off-State Output Current:					$V_O = 0.45\text{V}$ $V_O = 5.5\text{V}$
	MA ₀ -MA ₈ , FO			-100	μA	
	MA ₀ -MA ₈ , FO, PR ₀ -PR ₂			100	μA	

NOTES:

(1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

(2) EN input grounded, all other inputs and outputs open.

A.C. CHARACTERISTICS AND WAVEFORMS $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

SYMBOL	PARAMETER	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{CY}	Cycle Time ⁽²⁾	95	60		ns
t_{WP}	Clock Pulse Width	40	20		ns
	Control and Data Input Set-Up Times:				
t_{SF}	LD, AC ₀ -AC ₆	10	0		ns
t_{SK}	FC ₀ , FC ₁	0			ns
t_{SX}	SX ₀ -SX ₃ , PX ₄ -PX ₇	35	25		ns
t_{SI}	FI	15	5		ns
	Control and Data Input Hold Times:				
t_{HF}	LD, AC ₀ -AC ₆	5	0		ns
t_{HK}	FC ₀ , FC ₁	0			ns
t_{HX}	SX ₀ -SX ₃ , PX ₄ -PX ₇	25	5		ns
t_{HI}	FI	22	8		ns
t_{CO}	Propagation Delay from Clock Input (CLK) to Outputs (MA ₀ -MA ₈ , FO)	10	30	45	ns
t_{KO}	Propagation Delay from Control Inputs FC ₂ and FC ₃ to Flag Out (FO)		16	50	ns
t_{FO}	Propagation Delay from Control Inputs AC ₀ -AC ₆ to Latch Outputs (PR ₀ -PR ₂)		26	50	ns
t_{EO}	Propagation Delay from Enable Inputs EN and ERA to Outputs (MA ₀ -MA ₈ , FO, PR ₀ -PR ₂)		21	35	ns
t_{FI}	Propagation Delay from Control Inputs AC ₀ -AC ₆ to Interrupt Strobe Enable Output (ISE)		24	40	ns

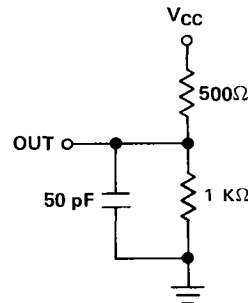
NOTE:

(1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.(2) $t_{CY} = t_{WP} + t_{SF} + t_{CO}$

TEST CONDITIONS:

Input pulse amplitude of 2.5 volts.
 Input rise and fall times of 5 ns between 1 volt and 2 volts.
 Output load of 10 mA and 50 pF.
 Speed measurements are taken at the 1.5 volt level.

TEST LOAD CIRCUIT:

CAPACITANCE⁽²⁾ $T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance:				
	CLK, EN		11	16	pF
	All Other Inputs		5	10	pF
C_{OUT}	Output Capacitance		6	12	pF

NOTE:

(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is $f = 1\text{ MHz}$, $V_{BIAS} = 2.5\text{V}$, $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$.

3001 WAVEFORMS

