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September 29, 1969
Electronics International

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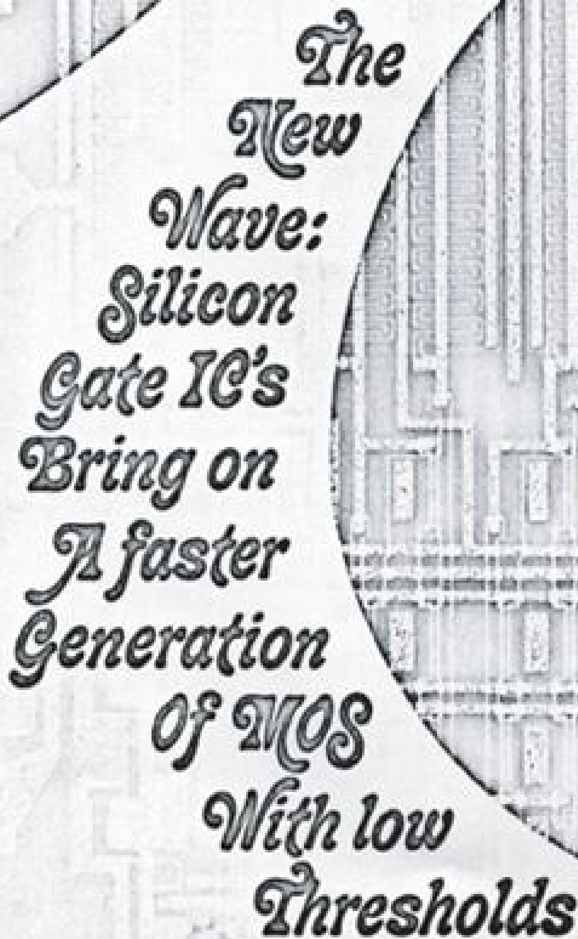


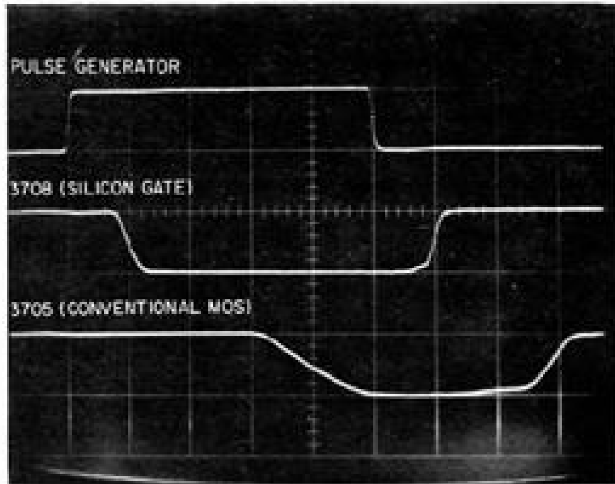
# A faster generation of MOS devices with low thresholds is riding the crest of the new wave, silicon-gate IC's

In what may well be the technology's most startling change, highly doped silicon — not aluminum — is used as the gate electrode; the new technique lends itself to bipolar processing, say Federico Fagginand Thomas Klein, engineers at Fairchild Semiconductor

● Unquestionably, the silicon gate is the new wave in MOS technology. And it's no secret that silicon-gate integrated circuits have lived up to their promise of great speed and low threshold voltages, with the latter making them compatible with bipolar IC's. Just how well this promise has been fulfilled is evidenced by the committment both the Intel Corp. and Fairchild Semiconductor have made to the silicon-gate technique [*Electronics*, Sept. 15, p. 67]. In fact, Fairchild plans to use the technique in just about all of the company's new metal-oxide-semiconductor circuits.

Why is Fairchild so enamored with the silicon-gate technique? The answer, obviously, stems from several factors. But they all add up to this. The technique has already reduced threshold voltages to a mere 0.4 volt, it has tripled speed, and it has cut circuit area by as much as a half—thus more functions can be packed into a given chip area.

Aside from both present and future digital applications, the technique will be useful in making analog circuits for low-level input signals. But the most important application more than likely will be the marriage of MOS and bipolar transistors on the same chip. This marriage will come about because silicon-gate devices, with their protected gate oxide, can be exposed to high diffusion temperatures at almost any step in the process without risk of deterioration.




**Waveforms:** Control signal from the pulse generator causes the eight-channel multiplexer to switch channels. Switching occurs much more rapidly in the silicon-gate version of the multiplexer (3708) than in the conventional version (3705). Here, the IC's are switched from channel 7 to channel 8. Horizontal scale is 200 nsec per division; vertical scale is 5 volts per division. Test circuit is shown below.

In essence, the technique differs from the conventional approach in that the MOS IC is fabricated with polycrystalline silicon, rather than aluminum, as the gate electrode [*Electronics*, May 26, p. 49]. Both techniques are equal in terms of complexity—the number of masking steps are the same. Just why the silicon-gate technique hadn't been thought of earlier can be attributed largely to the fact that aluminum has always been the least troublesome part of MOS structures. Advances in the technology stemmed in large part from work on the dielectric and the semiconductor-dielectric interface, rather than on the aluminum. Moreover, poly silicon can't be wire bonded, and this probably contributed to the delay in considering the material. Researchers reasoned that an aluminum interconnection layer would still be needed.

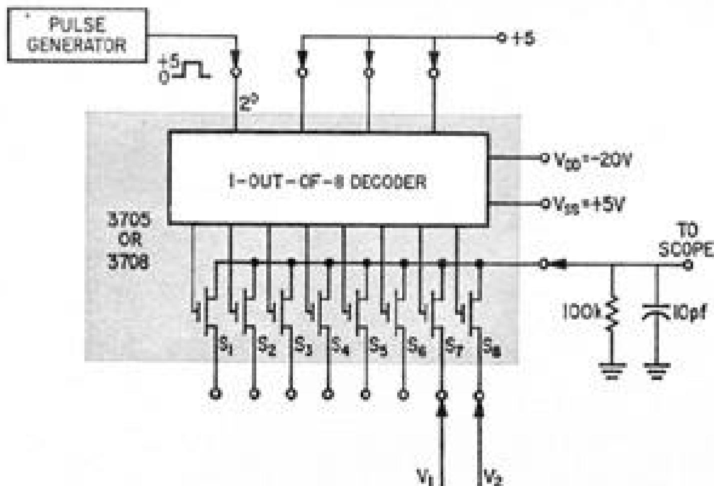
**Even when the first** silicon-gate MOS devices were successfully fabricated, J. C. Sarace and his coworkers at Bell Telephone Laboratories who were doing the research apparently failed to recognize some of the most significant advantages of the structure. This was particularly true of the reduced threshold voltage and the higher component density. Fairchild entered the picture late in 1967, when it launched its silicon-gate research-and-development effort. And now, less than two years later, the company is going all out with the new technique.

## A rose by any other name . . .

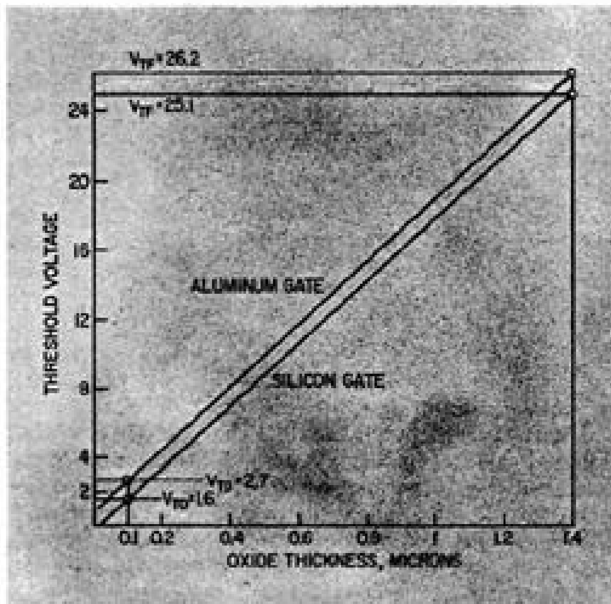
Metal oxide semiconductors they're called, but metal oxide semiconductors they're not—at least, the newer "MOS" devices are not.

When the term first was coined, no one foretold the proliferation of surface-controlled devices and IC's that were to depart from the traditional structure of a semiconductor in which a metallic oxide serves as an insulating layer. These changes have been so radical that MOS no longer is exactly accurate. First, silicon nitride entered the picture as an alternative to silicon dioxide. Now, highly doped silicon has come along as a replacement for the aluminum-gate electrode.

A far more descriptive term would be conductor-insulator-semiconductor, or CIS. Though such a term comes closer to the mark, its chances of being picked up and popularized are so slim as to be almost nonexistent. So entrenched is the term MOS in engineering parlance that it would be virtually impossible for it to be dropped. And as if adding insult to injury, silicon-gate circuits can be described mathematically with the same physical and electrical models as MOS circuits. Little wonder the term MOS will be around for a while.



**. . . Another factor contributing to the small size is that separate masks are used to deposit the gate and the metalization in silicon-gate IC's . . .**




**Improvement.** Silicon gate gives lower threshold voltage for any oxide thickness: Moreover, it gives a higher ratio of parasitic threshold to device threshold ($V_{TF}/V_{TO}$).

Strangely enough, what at first appeared to be major problems—obtaining a thin, smooth film of poly silicon so that contact could be made with the aluminum metalization, and preventing oxygen contamination of the gate during the boron diffusion that would prevent good contact with the aluminum metalization— proved, in the long run, not to be serious at all.

The low threshold voltage is traced to the silicon itself. It has a lower work function than aluminum, and it reduces the fixed surface-state charge, $Q_{ss}$—both of which strongly influence the threshold voltage, $V_{TO} = (Q_{ss} + Q_B)/C_o - \Phi_{MS} - 2\phi_f$, where $Q_B$ is the bulk charge of the silicon, $C_o$ is the dielectric capacitance (which is equal to $k/x_o$, the ratio of dielectric constant to the thickness of the dielectric), $\Phi_{MS}$ is the work-function difference between the metal and semiconductor, and $2\phi_f$ is the difference in Fermi potential between the inverted surface and the bulk of the semiconductor.

All other things being equal, the use of p-doped silicon for the gate will reduce $V_{TO}$ by 1.1 volts from that of an aluminum gate.

The advantage of the silicon gate becomes even more apparent when the equation is simplified to a linear function of oxide thickness alone: $V_{TO} = A_1 + A_2x_o$, where $A_1$ and $A_2$ are constants for any given MOS structure.

With the conventional aluminum-silicon dioxide-silicon

**Shrinkage.** Conventional gate masks must allow for misalignment and therefore produce a transistor that's 50% wider than the self-aligning silicon-gate device.

## Comparison of basic parameters

| | 1-1-1 Si gate | 1-1-1 conventional | 1-0-0 Si gate | 1-0-0 conventional |
|---|---|---|---|---|
| $V_{TO}$, active device threshold voltage | 1.5-2.0 | 3.5-5.0 | 0.4-1.2 | 2.0-3.0 |
| $V_{TF}$, parasitic device threshold voltage | 25-40 | 25-40 | 10-17 | 10-17 |
| $BV_D$, drain breakdown voltage with gate grounded | 29-33 | 35-45 | 29-33 | 35-45 |

structure, $A_1$ is about 0.9 volt. But with the silicon-gate structure (silicon-$SiO_2$-silicon), $A_1$ is 1.1 volts lower or −0.2 volt. This means that with a typical gate-oxide thickness of 0.1 micron, $V_{TO}$ is 2.7 volts for the conventional structure and only 1.6 volts for the silicon-gate structure as shown on opposite page.

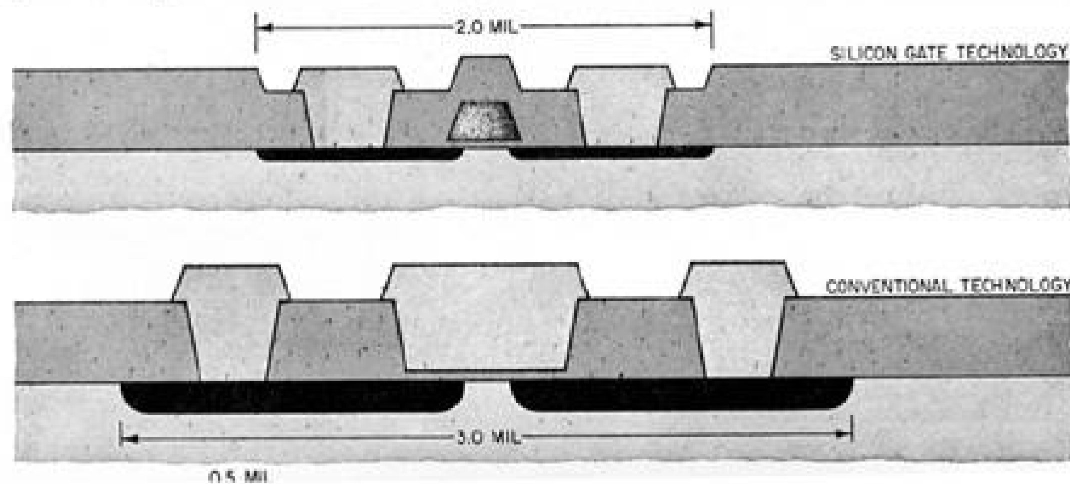
Even more important is the effect of lower $A_1$ on the ratio of thick-oxide to thin-oxide threshold voltages. Over the rest of the MOS chip, the oxide is made many times thicker than the gate oxide to minimize chances for parasitic MOS transistors. Typically, the thickness in this region is about 1.4 microns. With conventional MOS structures, the ratio of parasitic threshold to device threshold is 9.7. For the silicon gate structure, the ratio is 15.2. Thus, silicon-gate structures provide margins for operating voltages that are far more comfortable than what conventional structures provide. The figures given here are for 1-1-1 oriented silicon crystals. For 1-0-0 material, the difference is greater, as shown in the table above. The threshold voltage for resistance can be made as low as 0.4 volt.

How does silicon-gate technology result in more compact circuits and faster switching? Consider, first, the conventional process. Here, allowance has to be made for possible misalignment of the three masks used for the source-drain diffusion, gate dielectric growth, and gate-metal deposition. The cumulative alignment tolerances and sideways diffusion during gate oxidation create large source- and drain-junction areas, and—far more serious—create a large capacitance between gate and drain. This capacitance, caused by the necessary overlapping of the gate metal and the diffused regions, limits switching speed and is particularly evident when a high-dielectric-constant material (silicon nitride) is used as the gate insulator to obtain low threshold voltage.

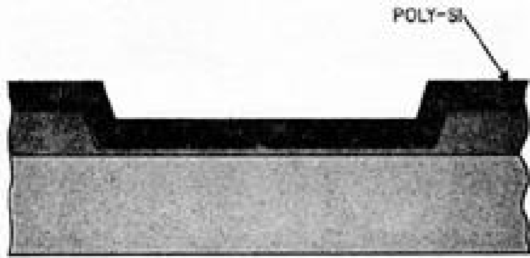
**Unlike the conventional** structure, the silicon-gate structure aligns itself so that there's no need to allow extra area for misalignment. Source and drain regions are diffused after gate oxidation, so there's negligible sideways diffusion. The result is a device whose gate-drain feedback capacitance is negligible. Thus the device can be placed in an area only 2 mils wide, not 3 mils, illustrated below.

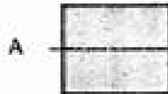
Another factor contributing to the small size is that separate masks are used to deposit the gate and the metalization in silicon-gate circuits, whereas the same mask is used in the conventional MOS process. In conventional circuits, there is a minimum spacing between gate and contact metal lines which is dictated by the resolution of the photolithographic process. This factor does not enter the silicon-gate picture.

The compactness afforded by the silicon-gate technology is clearly illustrated by the two-phase, dynamic

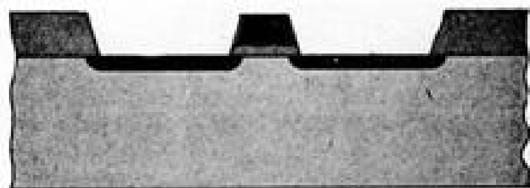


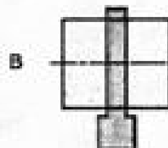
## So similar, yet so different



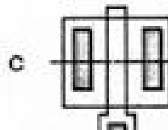



**Oxide is grown and poly silicon is deposited.**

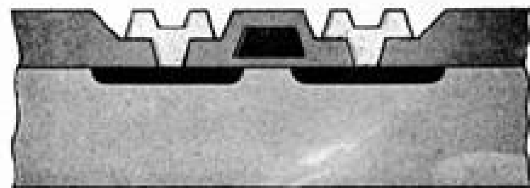


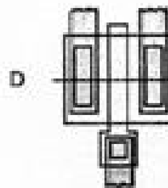



**Boron is diffused, forming source and drain junctions.**



**$SiO_2$ is deposited, windows for contacts are masked and etched.**




**Aluminum is deposited, second interconnection plane is defined.**

The conventional method of making MOS IC's starts with growing an oxide on the silicon wafer, and continues with diffusion of boron into the source, drain, and interconnection regions; removal of the thick oxide from regions where the gates are to be formed; growth of a thin thermal oxide in the gate regions under controlled conditions; opening holes in the contact areas; and metalizing the interconnection pattern.

Using silicon-gate technology, p-channel MOS IC's can be fabricated in four masking steps—the same number required in the conventional technology. The starting material, as shown at left, is an n-type silicon wafer; it is oxidized, and a window is etched for each MOS transistor. After this first masking step, the gate oxide is grown and a layer of polycrystalline silicon is deposited over the wafer (A).

The poly silicon layer is masked and etched to define the gate and the first interconnection plane. The gate oxide over the future source and drain is etched away. This is where the self-aligning feature of the silicon gate comes into play: it acts as a mask, preventing the gate oxide from being etched.

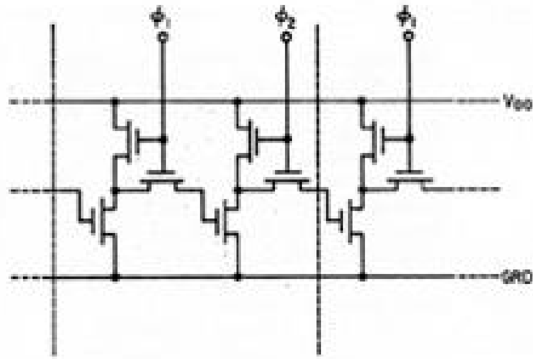
Next boron is diffused to form the source and drain junctions (B). Simultaneously, the silicon gate is doped p-type by the boron to give it low resistivity and provide the correct work-function difference.

Another layer of silicon dioxide is deposited, and windows for the source and drain contacts are masked and etched (C). Aluminum is then deposited over the entire surface, which is masked and etched to define the second interconnection plane (D).

The silicon gate process is much more flexible than the conventional one—because it is protected by the silicon and by more $SiO_2$, the delicate gate oxide can be exposed to high temperatures after it is formed.

This brings out a major advantage of the silicon-gate process: It's more compatible with bipolar processes. Suppose MOS and bipolar transistors are to be fabricated on the same chip with the conventional process. If it's not to be destroyed or seriously deteriorated, the gate oxide must be grown as the last high-temperature step. This requirement severely limits the performance that can be obtained from the bipolar devices.

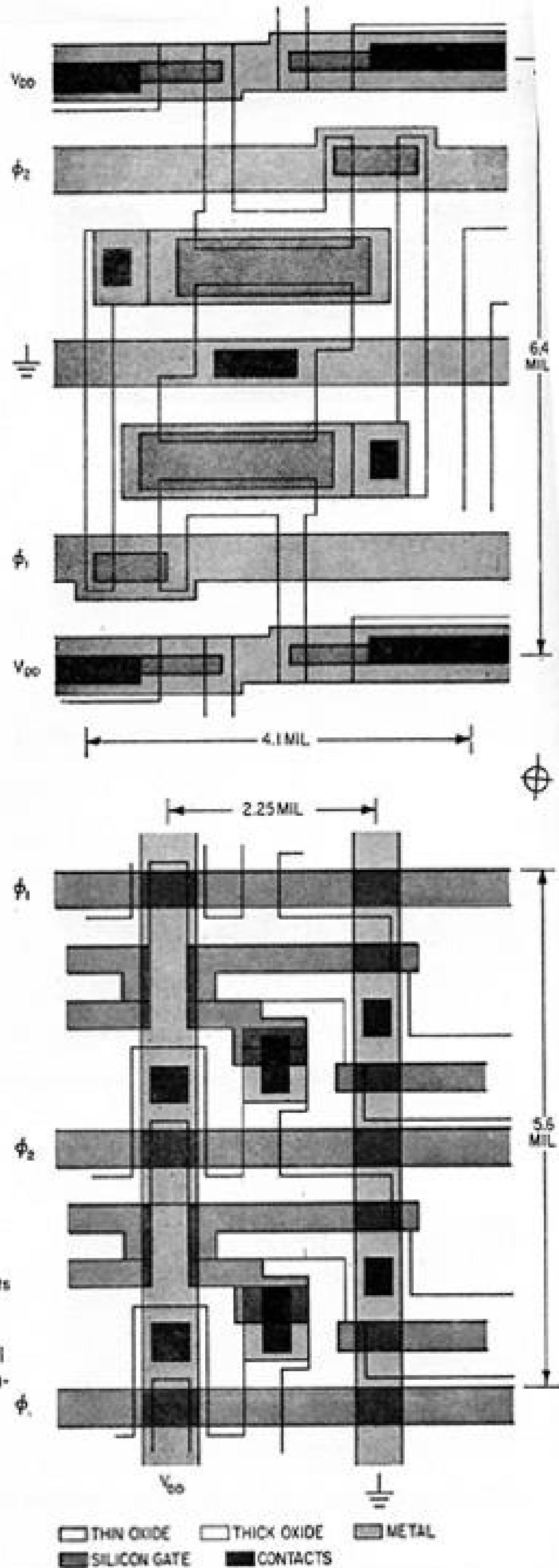
In silicon-gate circuits, however, subsequent processing won't affect the gate oxide. Shallow-diffused structures can be formed, as can bipolar transistors for driving current-sinking logic circuits. LSI will have the packing density of MOS and the speed of bipolar circuits.




shift register circuit at right. With silicon-gate technology, the register requires an area measuring 2.25 by 5.6 mils. With conventional technology, which must take into account the typical 0.2-mil tolerance for misalignment, the circuit requires an area 4.1 by 6.4 mils. Obviously, the conventional layout is severely metal-limited, which isn't true with the new technology. The silicon-gate layout is enhanced by the two available conductive planes.

**From a user's viewpoint,** the silicon-gate circuit's lower-threshold and higher-speed advantages are obvious. But the size advantage isn't quite as clear. In the long run, the small area will mean lower costs. This saving stems from the fact that more circuits can be packed onto a wafer and processed simultaneously, and because for a given number of defects per wafer, proportionately fewer circuits are affected.

Contributing to this higher yield is a significant difference in the process sequence. With the new techniques, the gate oxide is well protected by the silicon gate and by a deposited $SiO_2$ layer, so there is considerable freedom to use subsequent diffusion or other heat-treatment steps. In conventional MOS, on the other hand, the gate oxide is exposed until the final metalization. Because the gate oxide is thin and is critically located, the heat it can tolerate is severely limited and poor bipolar performance has to be accepted.




**Real estate:** Extra conductive plane provided by silicon-gate technique results in space saving over and above that given by the self-aligning feature. Conventional version of shift-register cell (top) occupies more area than the silicon-gate version (bottom) because more surface is needed for aluminum metalization.

## Comparison of multiplexer characteristics

| | 3705 (conventional) | 3708 (Si gate) |
|---|---|---|
| Data channel on resistance, ohms | 190 | 80 |
| Maximum output leakage current, na | 10 | 2 |
| Data input leakage current, na | 2 | 0.2 |
| Output capacitance, pf | 40 | 25.5 |
| Data input capacitance, pf | 7.5 | 4.5 |
| Logic input capacitance, pf | 5.5 | 2.5 |
| Absolute maximum voltage at any pin | —35 | —30 |

Fairchild has observed much higher yields in silicon gate circuits than in conventional MOS circuits whose function is identical, even when no attempt was made to exploit the smaller geometry of the silicon gate.

The circuits used for this comparison were the 3705, an eight-channel multiplexer switch with decoding logic and the 3708, a silicon-gate version of the same circuit with essentially the same geometry. The comparison of electrical characteristics in the table above is revealing; in almost every parameter, the silicon-gate version is superior.

The data-output channel on resistance, for example, is less than half that of the standard-gate IC because lower sheet resistivity in the p-diffused layers can be obtained with silicon-gate technology. This is because the boron-doped layers are not depleted by a subsequent reoxidation. In the interdigitated output buffers (eight are used in the circuit), the source and drain fingers therefore have less series resistance, and the output buffers therefore are more efficient.

The smaller input and output capacitances for the silicon-gate circuit are a direct result of the self-aligning gate.

And when it comes to switching speed, the silicon-gate version really shines. The silicon-gate 3708 responds to an output-enable control signal about three times faster than the standard-gate 3705. And the high level is about 10% greater in the 3708 because of its lower on resistance. In channel-to-channel switching, too, the silicon-gate IC out-performs the 3705, as shown by the waveforms on page 89.

**As for reliability,** silicon-gate IC's present no problem. Breakdown voltage, for example, showed a slight downward trend in some silicon-gate units in a 200-hour life test of 20 units at 150°C at a bias of —25 volts. In no case, however, did breakdown voltage go below the lowest pre-test value (32 volts), and it was always well above the minimum rating of 25 volts. Under accelerated life testing at 300°C for five minutes with —15 volts reverse bias applied at input and output, the silicon-gate circuits have proven to be exceptionally stable with no failure on the six runs tested. On resistance and leakage current showed similar behavior. After the 200-hour operating life test, for example, on resistance exhibited a negligible change in distribution. ●

### Bibliography

J.C. Sarace, R.E. Kerwin, D.L. Klein, and R. Edwards, "Metal-Nitride-Oxide Field-Effect Transistors with Self-Aligned Gates," Solid-State Electronics, Vol. 11, 1968, p. 653.

F. Faggin, T. Klein, and L. Vadasz, "Insulated Gate Field Effect Transistor Circuits with Silicon Gates," presented at International Electron Devices Meeting, Washington, October 1968.

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