AccessionIndex: TCD-SCSS-T.20220825.011
Accession Date: 25-Aug-2022
Accession By: Dr.Brian Coghlan
Object name: Intel Pentium microprocessor
Vintage: 1996
Synopsis: Pentium i166 CPU chip. P/N: FV80502166.

Description:
The Pentium was Intel's 5th generation 32-bit x86 microprocessor, introduced in 1993, instruction-set-compatible with the i80486, but with a new microprocessor architecture that Intel called their *P5* microarchitecture. It was the first superscalar x86 microarchitecture, with separate instruction and data caches, branch prediction, built-in floating-point unit, and a 64-bit external bus.

The Pentium i166 was released by Intel on 4th January, 1996, designated the part number FV80502166 and sSpec number SY037 (cC0). It was the 166MHz selection of Intel's *P54CS* (0.35µm) variant of their *P5* microarchitecture. It had a 166MHz external clock frequency, a 2.5X internal CPU clock-frequency multiplier, 8kB L1 instruction and data caches, a 66M-transactions/sec (MT/s) front-side bus (FSB), ran at 3.135–3.6 V, dissipated 14.5Watts, and had 321 pins to suit Intel's ZIF *Socket 7*.

The i166 in this Collection was removed from a working PC and replaced with an Evergreen *Spectra 333* plugin-upgrade using an AMD AMD K6-2 microprocessor. For convenience, Figures 5-16 show images of Intel's Pentium information brochure, see elsewhere in this catalog.

Many thanks to Brian Coghlan for donating this item.

The homepage for this catalog is at: https://www.scss.tcd.ie/SCSSTreasuresCatalog/
Click *'Accession Index'* (1st column listed) for related folder, or *'About'* for further guidance.
Some of the items below may be more properly part of other categories of this catalog,
but are listed here for convenience.

Accession Index	Object with Identification
TCD-SCSS-T.20220825.011.001	Intel Pentium microprocessor. Pentium i166 CPU chip. P/N: FV80502166. 1996.
TCD-SCSS-T.20220825.011.002	Intel Pentium microprocessor cradle.
TCD-SCSS-T.20220825.011.003	Intel Pentium microprocessor heatsink.
TCD-SCSS-V.20220825.001	Intel Pentium processor. Intel, information brochure about the Pentium microprocessor. 1996.

References:

1. Wikipedia, *Pentium (original)*, see:
   https://en.wikipedia.org/wiki/Pentium_(original)
   Last browsed to on 25-Aug-2022.

Figure 1: Pentium i166 in cradle, top view

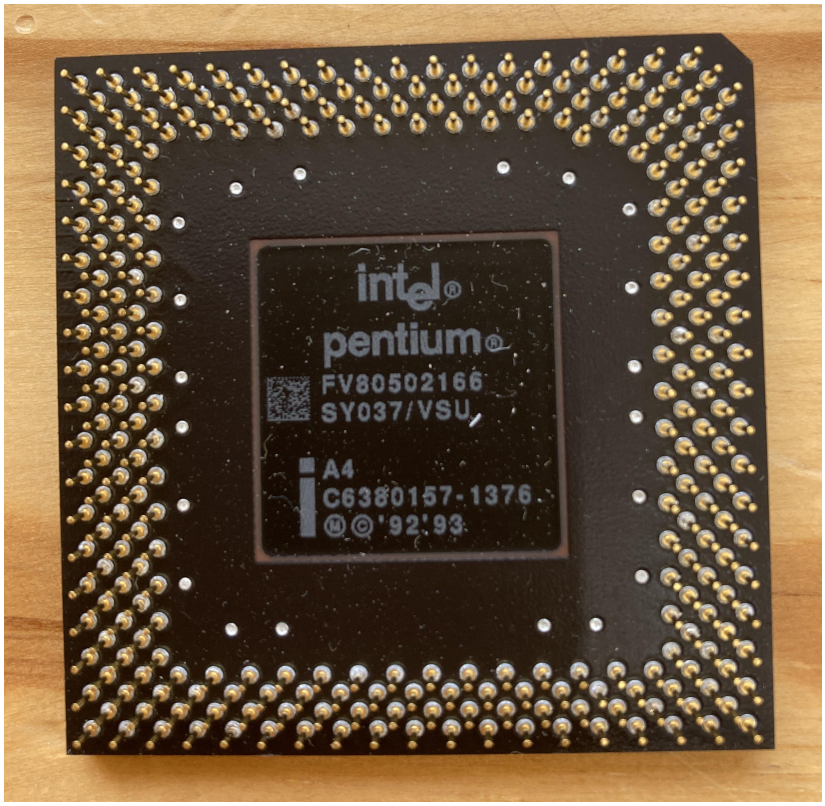


Figure 2: Pentium i166 bottom view

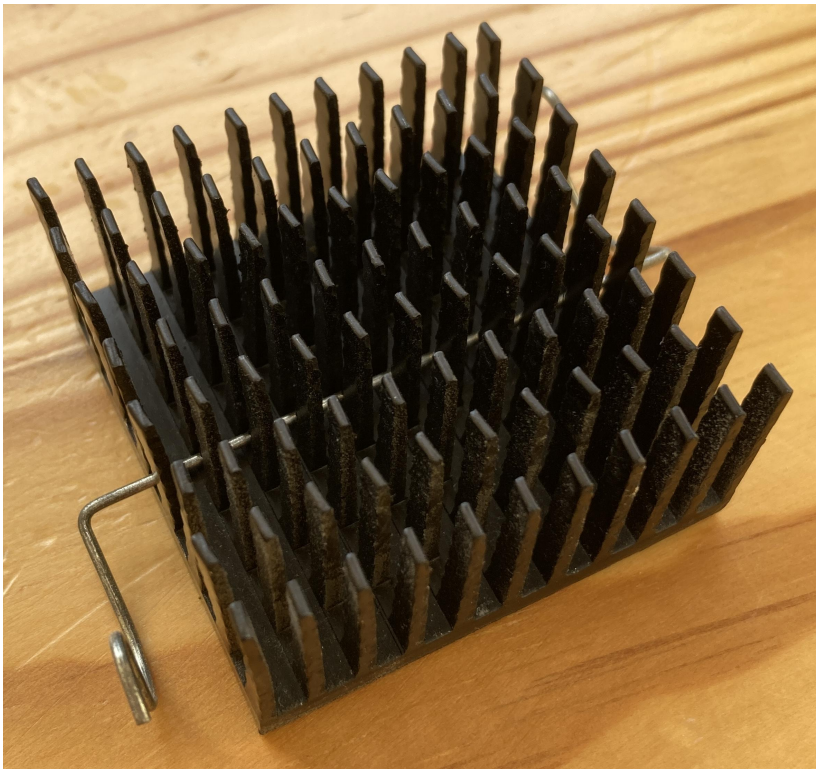


Figure 3: Pentium i166 heatsink

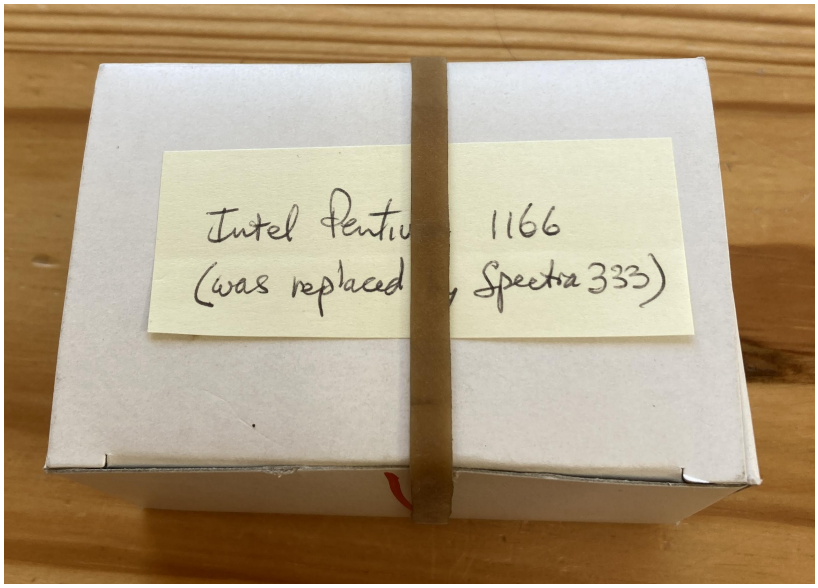


Figure 4: Pentium i166 in packaging

Figure 5: Pentium information brochure page 1

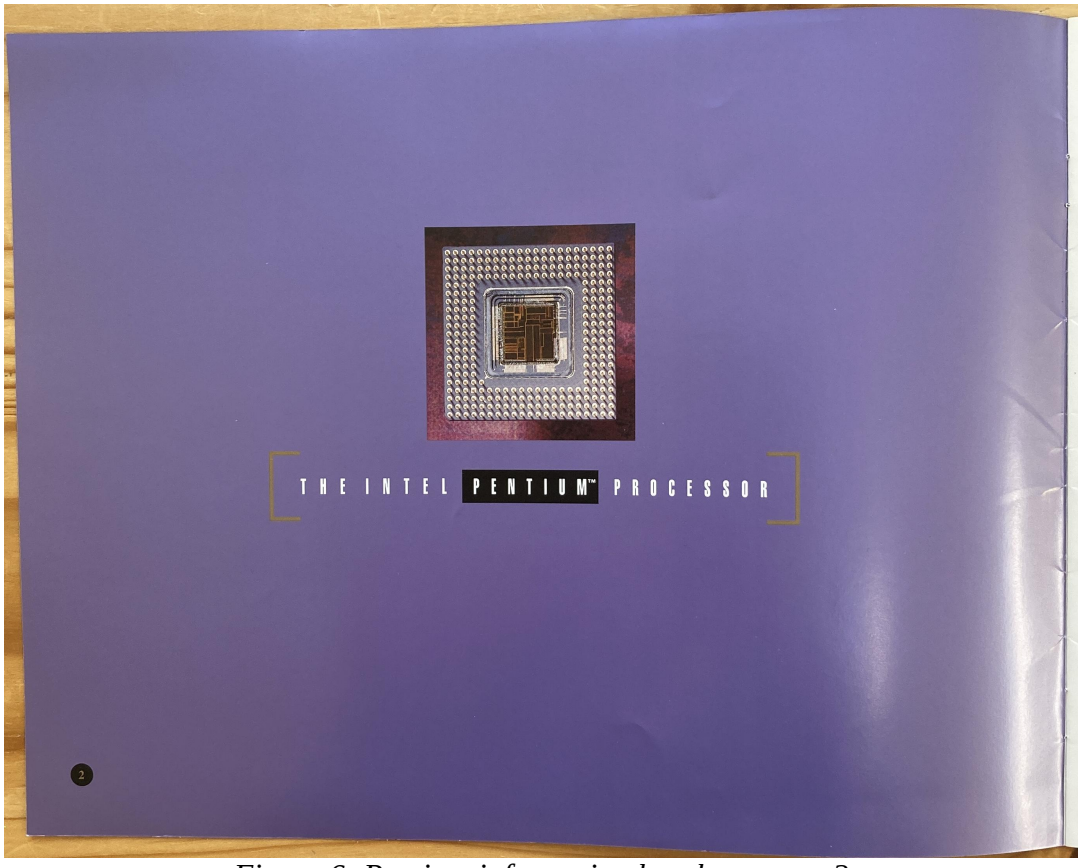


Figure 6: Pentium information brochure page 2

Intel's Pentium™ processor combines the performance traditionally associated with minicomputers and workstations with the flexibility and compatibility that characterize the personal computer platform. Designed to meet the needs of today's and tomorrow's sophisticated software applications, the Pentium processor extends the range of Intel's microprocessor architecture to new heights, blurring previous distinctions between hardware platforms and creating an entirely new realm of possibilities for notebook computers, desktop PCs, and servers.

This paper begins by presenting an overview of the Pentium processor. Afterwards, it details the key technological features that enable this Intel solution to meet the market's evolving requirements for high performance, continued software compatibility, and advanced functionality.

The world's best performance for all PC software

The Pentium processor family includes the highest performing members of Intel's family of microprocessors—the Pentium processor at iCOMP™ index 510\60 MHz, Pentium processor at iCOMP index 567\66 MHz, Pentium processor at iCOMP index 735\90 MHz, and Pentium processor at iCOMP index 815\100 MHz. While incorporating new features and improvements made possible by advances in semiconductor technology, the Pentium processor is fully software compatible with previous members of the Intel microprocessor family—thereby preserving the value of users' software investments which are worth billions of dollars. The Pentium processor meets the demands of computing in a number of areas: advanced operating systems, such as Windows 4.0*, UNIX*, Windows-NT*, OS/2*, Solaris* and NeXTstep*; compute-intensive graphics applications such as 3-D modeling, computer-aided design/engineering (CAD/CAE), large-scale financial analysis, high-throughput client/server, handwriting, and voice recognition; network applications; virtual reality; electronic mail that combines many of the above areas; and new applications yet to be developed.

The Pentium processor family was designed using an advanced process technology and has features that are less than a micron (one-millionth of a meter) in size. The Pentium processor (510\60, 567\66) was developed utilizing 5V, 0.8 micron technology with 3.1 million transistors, while the Pentium processor (735\90, 815\100) was designed using 3.3V, 0.6 micron technology with 3.3 million transistors.

The Pentium processor: technical innovations

There are a number of innovative product features that contribute to the Pentium processor's unique combination of high performance, compatibility, data integrity and upgradability. These include:

- Superscalar architecture
- Separate code and data caches
- Branch prediction
- High-performance floating-point unit
- Enhanced 64-bit data bus
- Data integrity features
- SL technology power management features
- Multiprocessor support
- Performance monitoring
- Memory page size feature
- Upgradability

Figure 7: Pentium information brochure page 3

Superscalar architecture

The Pentium processor's superscalar architecture enables the processor to achieve new levels of performance by executing more than one instruction per clock cycle. The term "superscalar" refers to a microprocessor that contains more than one execution unit. These execution units—or pipelines—are where the chip processes the data and instructions that are fed to it by the rest of the system.

The Pentium processor's superscalar implementation represents a natural progression from previous generations of processors in the 32-bit Intel architecture. The Intel486™ processor, for example, is able to execute many of its instructions in one clock cycle, while previous generations of Intel microprocessors require multiple clock cycles to execute a single instruction.

This ability to execute multiple instructions per clock cycle is due to the fact that the Pentium processor's two pipelines can execute two instructions simultaneously. As with the Intel486 processor's single pipeline, the Pentium processor's dual pipelines execute integer instructions in five stages: prefetch, decode 1, decode 2, execute and write-back. This permits several instructions to be in various stages of execution, thus increasing processing performance.

The Pentium processor also uses hardwired instructions to replace many of the microcoded instructions used in previous microprocessor generations. Hardwired instructions are simple and commonly used, and can be executed by the processor's hardware without requiring microcode. This improves performance without affecting compatibility. In the case of more complex instructions, the Pentium processor's enhanced microcode further boosts performance by employing both dual integer pipelines to execute instructions.

Separate code and data caches

Another significant advancement is the Pentium processor's innovative on-chip cache implementation. On-chip caches increase performance by acting as temporary storage places for commonly-used instructions and data, replacing the need to go off-chip to the system's main memory to fetch information. The Intel486 microprocessor, for example, contains a single 8 Kbyte on-chip cache to handle both code and data caching functions. Intel Pentium processor designers improved on this implementation by creating separate on-chip code and data caches. This increases performance because bus conflicts are reduced (with a single cache, conflicts can occur between instruction prefetches and data accesses) and the caches are available more often when they are needed.

The Pentium processor's code and data caches each contain 8 Kbytes of information, and both are organized as two-way set associative caches—meaning that they save time by searching only pre-specified 32-byte segments rather than the entire cache. This performance-enhancing feature is in turn supplemented by the Pentium processor's 64-bit data bus, which ensures that the dual caches and superscalar execution pipelines are continually supplied with data.

The Pentium processor's data cache uses two other important techniques: "write-back" caching and an algorithm called the MESI (Modified, Exclusive, Shared, Invalid) protocol. The write-back method transfers data to the cache without going out to main memory (data is written to main memory only when it is removed from the cache). In contrast, previous-generation "write-through" cache implementations transfer data to the external

Figure 8: Pentium information brochure page 4

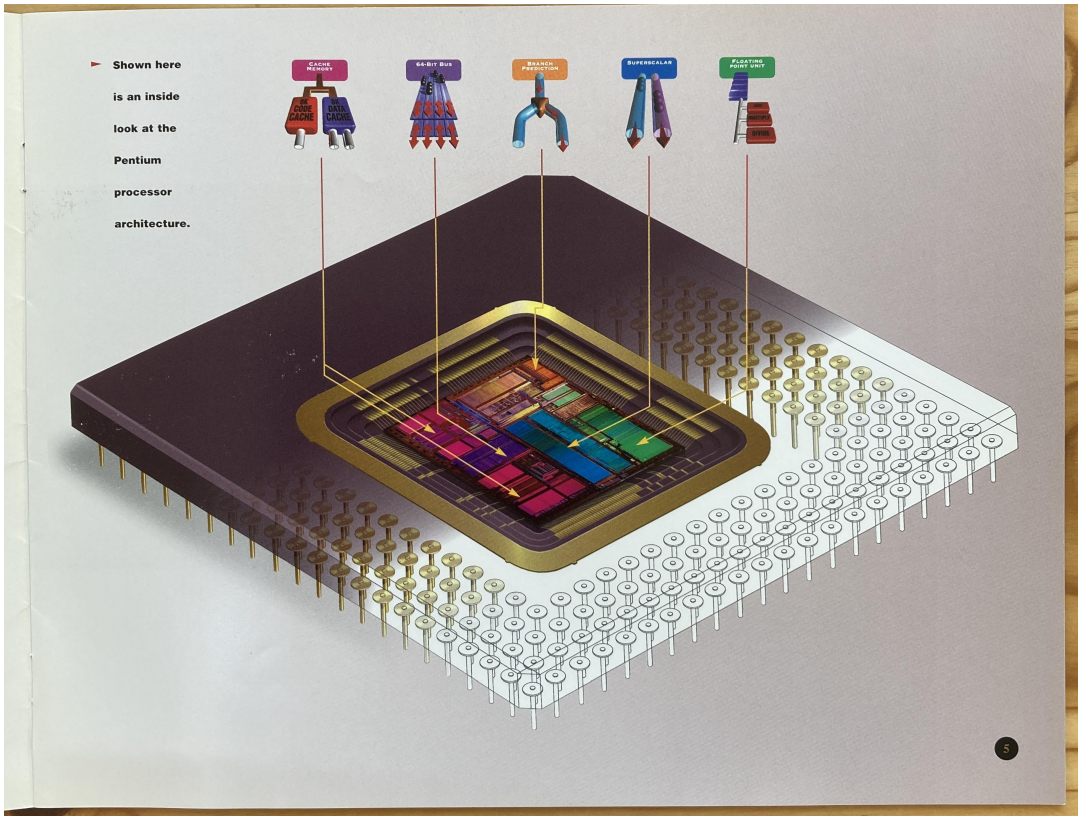


Figure 9: Pentium information brochure page 5

memory each time the processor writes data to the cache. The write-back technique increases performance by reducing bus utilization and preventing needless bottlenecks in the system.

To ensure that data in the cache and in main memory are consistent, the data cache implements the MESI protocol. By obeying the rules of the protocol during reads/writes, the Pentium processor can maintain cache consistency and circumvent problems that might be caused by multiple processors using the same data.

Branch Prediction

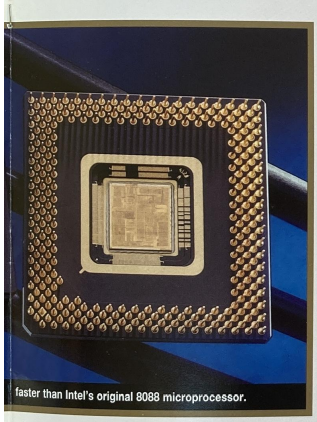
Branch prediction is an advanced computing technique that boosts performance by keeping the execution pipelines full. This is accomplished by predetermining the most likely set of instructions to be executed. The Pentium processor is the first PC-compatible microprocessor to use branch prediction, which until now has traditionally been associated with mainframe computers.

For a better understanding of this concept, consider a typical application program. After each pass through a software loop, the program performs a conditional test to determine whether to return to the beginning of the loop or to exit and continue on to the next execution step. These two choices, or paths, are called branches. Branch prediction forecasts which branch the software will require, based on the assumption that the previous branch that was taken will be used again. The Pentium processor makes branch predictions using a Branch Target Buffer (BTB). This software-transparent innovation eliminates the need for recompiling code, thus increasing overall speed and application software performance.

To efficiently predict branches, the Pentium processor uses two prefetch buffers. One buffer prefetches code in a linear fashion (for the next execution step) while the other prefetches instructions based on addresses in the Branch Target Buffer (to jump to the beginning of the loop). As a result, the needed code is always prefetched before it is required for execution.

The Pentium processor's prediction algorithm not only forecasts simple branch choices, but also supports more complex branch prediction—for example, within nested loops. This is accomplished by storing multiple

Figure 10: Pentium information brochure page 6



branch addresses in the Branch Prediction Buffer. The BTB's design allows 256 addresses to be recorded, and thus the prediction algorithm can forecast up to 256 branches.

High-performance floating-point unit

The emerging wave of 32-bit compute-intensive software applications require a high degree of floating-point processing power to handle mathematical calculations. As the floating-point requirements of personal computer software have steadily increased, advances in microprocessor technology have been introduced to satisfy these needs. The Intel486 DX processor, for example, was the first Intel microprocessor to integrate math coprocessing functions on-chip; previous-generation Intel processors used off-chip math coprocessors when floating-point calculations were required.

The Pentium processor family takes math computational ability to the next performance level by using an enhanced on-chip floating-point unit that incorporates sophisticated eight-stage pipelining and hardwired functions. A three-stage floating-point instruction pipeline is appended to the integer pipelines. Most floating-point instructions begin execution in one of the integer pipelines, then move on to the floating-point pipeline. In addition, common floating-point functions—such as add, multiply and divide—are hardwired for faster execution.

As a result of these innovations, the Pentium processor (815\100) executes floating-point instructions five to ten times faster than the 33-MHz Intel486 DX processor, optimizing it for the high-speed numeric calculations inherent in advanced visual applications such as CAD and 3D graphics.

Enhanced 64-bit data bus

The data bus is the highway that carries information between the processor and the memory subsystem. Because of its external 64-bit data bus, the Pentium processor can transfer data to and from memory at rates up to 528 Mbytes/second, a more than five-fold increase over the peak transfer rate of the 66-MHz IntelDX2™ microprocessor (105 Mbytes/second). This wider data bus facilitates high-speed processing by maintaining the flow of instructions and data to the processor's superscalar execution unit. As a result, the Pentium processor's (815\100) overall performance is

Figure 11: Pentium information brochure page 7

over two and one-half times that of the 66-MHz IntelDX2 microprocessor.

In addition to having a wider data bus, the Pentium processor implements bus cycle pipelining to increase bus bandwidth. Bus cycle pipelining allows a second cycle to start before the first one is completed. This gives the memory subsystem more time to decode the address, which allows slower and less-expensive memory components to be used—resulting in a lower overall system cost. Furthermore, burst reads and writes, parity on address and data, and a simple cycle identification all contribute to providing better bandwidth and improved system reliability.

The Pentium processor also has two write buffers, one corresponding to each pipeline, to enhance the performance of consecutive writes to memory. Write buffers improve performance by allowing the processor to proceed with the next set of instructions, even though one of the current instructions needs to write to memory while the bus is busy.

Data integrity features

Protecting important data and ensuring its integrity has become increasingly important as mission-critical applications continue to proliferate. To ensure the Pentium processor's reliability, Intel performed millions of simulations and tests. In addition, designers integrated two advanced features traditionally associated with mainframe-class designs—internal error detection and functional redundancy testing—to help preserve data integrity in today's evolving PC-based networks.

Internal error detection places parity bits on the internal code and data caches, translation look aside buffers, microcode, and branch target buffer. This feature helps detect errors in a manner that remains transparent to both the user and the system.

For situations where data integrity is especially crucial, the Pentium processor supports Functional Redundancy Checking (FRC). FRC requires the use of two Pentium chips, one acting as the master and the other as the "checker." The two chips run in tandem, and the checker compares its output with that of the master Pentium processor to assure that errors have not occurred. If a discrepancy is discovered, the system is notified.

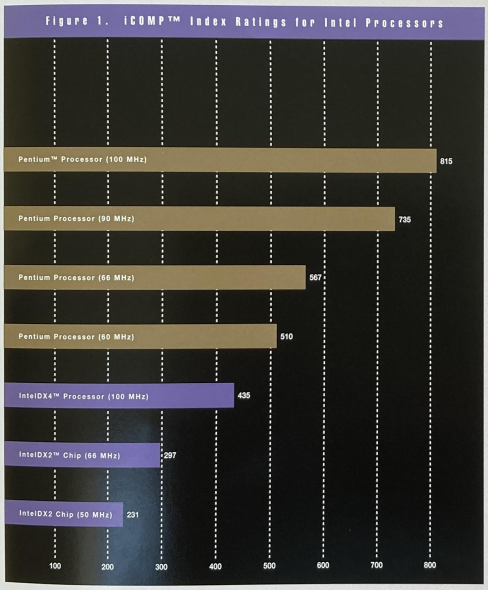
SL technology power management features

The Pentium processors (735\90, 815\100) incorporate new SL technology features for superior power-management capabilities. These features operate at two levels: the microprocessor and the system. Power management at the processor level involves putting the processor into low power state during non-processor intensive tasks (such as word processing), or into a very low-power state when the computer is not in use ("sleep" mode). At the system level, Intel's SL technology uses system management mode (SMM) to control the way power is used by the computer (including peripherals). This mode provides intelligent system management that allow the microprocessor to slow down, suspend, or completely shut down various system components so as to maximize energy savings. All members of the Pentium processor family include SMM.

Multiprocessor support

The Pentium processor is ideal for the increasing wave of multiprocessing systems. Multiprocessing applications that combine two or more Pentium processors are well

Figure 12: Pentium information brochure page 8



served by the chip's advanced architecture, separate on-chip code and data caches, chip sets for controlling external caches, and sophisticated data integrity features.

As previously discussed, the Pentium processor family uses the MESI protocol to maintain cache consistency among several processors. The Pentium processor also ensures that instructions are seen by the system in the order that they were programmed. This strong ordering helps software designed to run on a single-processor system to work correctly in a multiprocessing environment.

The Pentium processors (735\90, 815\100) also include two new multiprocessor (MP) features: a multiprocessor interrupt controller on-chip and the dual processor mode. The processor's on-chip MP interrupt controller can support up to 60 processors. The dual processor mode enables two processors to share a single second-level cache, allowing the development of low-cost shared-cache multiprocessor systems for workstations and low-end servers.

Source: iComp™: A simplified measure of relative Intel microprocessor performance, Intel Corp., 1992.

Figure 13: Pentium information brochure page 9

Performance Monitoring

Performance monitoring is a feature of the Pentium processor that enables system designers and application developers to optimize their hardware and software products by identifying potential code bottlenecks. Designers can observe and count clocks for internal processor events that affect the performance of data reads and writes, cache hits and misses, interrupts, and bus utilization. This allows them to measure the effect that their code has on both the Pentium processor architecture and their product, and to fine-tune their application or system for optimal performance. The benefit to end users is better value and higher performance, due to the greater synergy between the Pentium processor, its host system, and application software.

Memory Page Size Feature

The Pentium processor offers the option of supporting either the traditional memory page size of 4 Kbytes, or a larger 4 Mbyte page. This feature—which is transparent to the application software—was provided to reduce the frequency of page swapping in complex graphics applications, frame buffers, and operating system kernels, where the increased page size allows users to map large, previously unwieldy objects. The larger page enables an increased page hit rate, which results in higher performance.

Upgradability

As with all new implementations of the Intel 32-bit microprocessor architecture, the Pentium processor has been designed for easy upgradability using Intel's upgrade technology. This innovation protects user investments by adding performance that helps to maintain the productivity levels of Intel processor-based systems over their entire lifespans.

Upgrade technology makes it possible for users to take advantage of more advanced processor technology in their existing systems with an easy-to-install, single-chip performance upgrade. For example, Intel's first upgrade options, the OverDrive™ processors developed for Intel486 SX and Intel486 DX processors, apply the same speed-doubling technology used in the development of the IntelDX2 microprocessor.

Intel's upgrade processors will also be available for systems based on the Pentium processor family, ensuring an easy future upgrade path based on even more advanced processor technology. In addition, Pentium processor technology will be the basis of the upgrade processors now being developed for Intel486 processor-based systems.

Increased Performance: By the Numbers

The Pentium processor stands alone on the performance ladder when compared to all other PC-compatible microprocessors. While there are many ways to measure performance, three different examples are offered here to demonstrate the Pentium processor's speed and processing power: Intel's iCOMP™ index, the SPECint92 UNIX benchmark, and the SPECfp92 UNIX benchmark.

One indication of the Pentium processor's high performance is provided by Intel's iCOMP (Intel COmparative Microprocessor Performance) index. The iCOMP index, which measures the performance of the members of the Intel 32-bit architecture, was created so that computer users can more easily identify relative performance differences among Intel's microprocessors. The index is based on four distinct aspects of processor performance: integer, floating-point, graphics and video performance. Each of the four

Figure 14: Pentium information brochure page 10

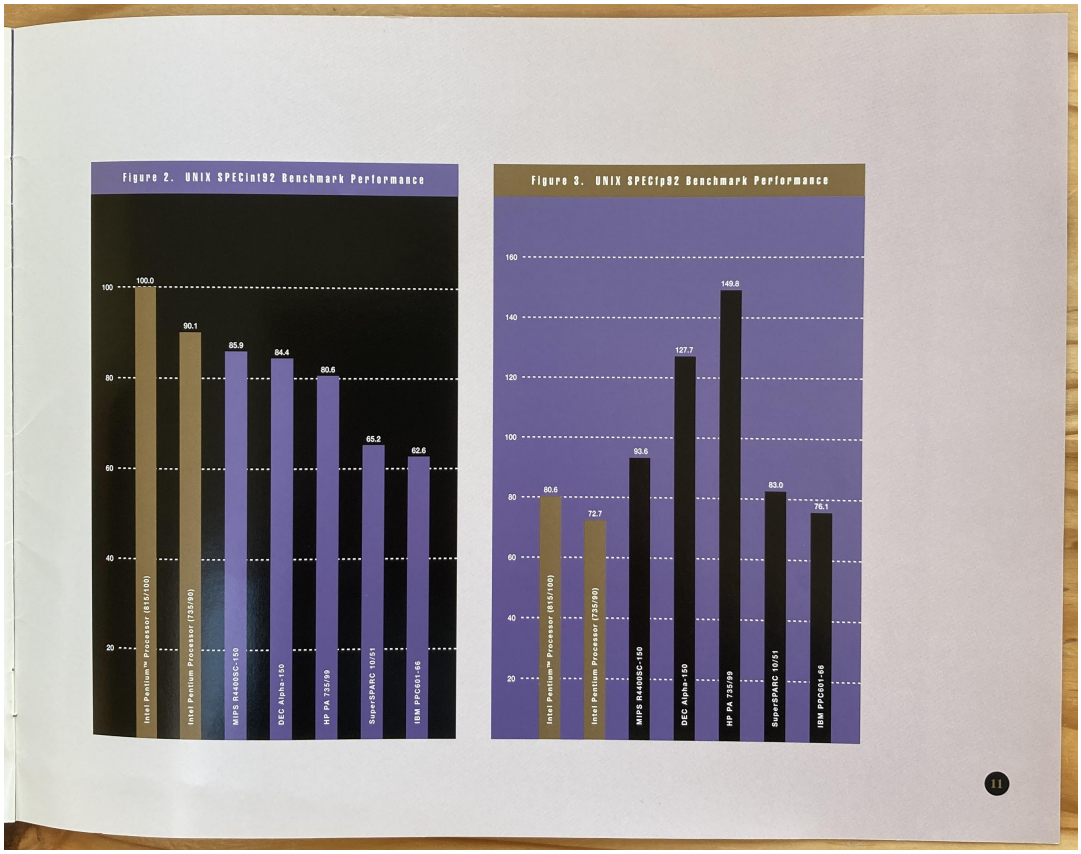


Figure 15: Pentium information brochure page 11

elements is considered for both 16- and 32-bit software, and is weighted relative to the estimated percentage of time it occupies the processor's attention (based on a mix of today's commonly used application software). As shown in Figure 1, the Pentium processor at iCOMP index 815\100 MHz has more than 2.7 times the relative performance of the 66-MHz IntelDX2 microprocessor, which has an iCOMP rating of 297.

SPECint92 is a processor-intensive UNIX benchmark (Figure 2) that evaluates desktop performance using a representative mix of application instructions. With a SPECint92 rating of 100.0, the Pentium processor at iCOMP index 815\100 MHz outperforms many workstation-class, RISC-based processors, including members of the IBM, MIPS and Sun SPARC processor families.

The SPECfp92 UNIX benchmark (Figure 3) is a useful measure of floating-point performance. The SPECfp92 rating for the Pentium processor at iCOMP index 815\100 MHz is 80.6. This is comparable to that of today's RISC architectures, and is more than 4.3 times that of the 66-MHz IntelDX2 processor.

High performance while maintaining compatibility

The Pentium processor family provides extremely high-performance because it incorporates the latest state-of-the-art design principles. With its superscalar architecture, separate code and data caches, branch prediction, and enhanced floating-point unit, the Pentium processor can meet the performance needs of today's—and tomorrow's—applications software. Meanwhile, it maintains complete compatibility with the large installed base of software currently running on Intel architecture processors.

The Pentium processor's combination of performance and compatibility uniquely positions it to meet the needs of the emerging wave of notebook, desktop, and server applications. Not only will users experience dramatic performance improvements while running their current software, but they can also anticipate that new applications will take even further advantage of the Pentium processor's high-performance features.

Figure 16: Pentium information brochure page 12