UNIBUS

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The **UNIBUS** (or **Unibus** - the capitalization style changed over time) was the earliest of two bus technologies used with PDP-11s manufactured by DEC; it was first seen in the PDP-11/20, in 1970. Later, early VAX systems from that company used the UNIBUS as an I/O bus; it was also used in the small mainframe KS10-based model of the DECSYSTEM-20, to furnish it with inexpensive peripherals.

It was the only bus in most PDP-11 systems, and thus supported several capabilities: the ability of the CPU to read and write main memory, and device registers; and the ability for devices to do DMA transfers to memory, and to interrupt the CPU.

It could exist on a cable (the original physical form of implementation), and later, within a backplane (in 'Small Peripheral Controller (SPC)' or 'Modified UNIBUS Device (MUD)' slots). Up to 20 nodes (devices) could be connected to a single UNIBUS segment; additional segments could be connected via a bus repeater.

The UNIBUS contained 16 data lines, and 18 address lines, as well as a number of control lines. The 18 address lines allowed the addressing of a maximum of 256 KBytes. Typically, the top 8 KBytes of address space was reserved for the registers of the memory mapped I/O devices used in the PDP-11 architecture; this block is often referred to as the **I/O page**. The limit of 18 address lines was to prove a severe handicap in the later phases of the UNIBUS' operational life.

The bus was completely asynchronous, allowing a mixture of fast and slow devices. It also allowed arbitration (selection of the next *bus master*) while the current bus master was still performing data transfers, overlapping the two functions.

The design deliberately minimized the amount of redundant logic required in the system. For example, a system always contained more slave devices than master devices, so most of the complex logic required to implement asynchronous data transfers was forced into the relatively few master devices. For interrupts, only the *interrupt-fielding processor* needed to contain the complicated timing logic.

The end result was that most I/O controllers could be implemented with very simple logic; most of the critical logic was later implemented as a custom MSI IC.

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Operation

Two control lines (C0 and C1) allowed the selection of four different data transfer cycle types in normal master/slave cycles:

- DATI (Data In, a read)
- DATIP (Data In/Pause, the first portion of a Read-Modify-Write operation. A DATO or DATOB operation completes this.)
- DATO (Data Out, a word write)
- DATOB (Data Out/Byte, a byte write)

During these operations, several signals (MSYN - Master Sync; SSYN - Slave Sync; and BBSY - Bus Busy) are used to synchronize between the master and slave, to indicate when the data is ready to be read (during a DATI/DATIP), or has been written (during a DATO/DATOB).

During an interrupt cycle, a fifth style of transfer was used to convey an *interrupt vector* from the interrupting device to the *interrupt-fielding processor*.

DMA and Interrupts

Both DMA (in which a device must request control of the bus, so that it can peform a normal master/slave cycle, only with itself as the master), and interrupts, use the same mechanism for the device to communicate with the CPU to request something, and for the CPU to communicate with the device that it has granted the device's request.

There are bus request lines (NPR for DMA, and BR4-BR7 for interrupts), and bus grant lines (NPG for DMA, and BG4-7 for interrupts). The request lines are normal 'wired-OR' broadcast bus lines, but the grant lines are special; they are wired in series - one device's 'grant out' line is connected to the next device's 'grant in' line, starting the the CPU's 'grant out' line.

When a device receives a grant, it uses another bus line (SACK) to indicate that it received its grant; if the CPU sends a grant, and does not see a SACK in response, it know there was some sort of error.

Documentation

Details of the operation of the UNIBUS may be found in the DEC publications "pdp11 peripherals handbook" (various editions from 1972 to 1977), and the "pdp11 bus handbook" (1979).

NOTE: There is a serious editing error in the latter volume, in the description of UNIBUS arbitration. On page 38, immediately after step 13 of the NPR Arbitration Sequence ("13. .... SACK must be negated before BBSY may be negated."), it says "A bus master may issue an interrupt command to the interrupt fielding processor."

Despite its location in the text, this does ***not*** apply to the "NPR arbitration sequence" being discussed above. There is an editing error - this text is (or *should be*) separate from the "NPR Arbitration Sequence" section just before it; it belongs with "BR Interrupt Arbitration Sequence" - that header (on pg. 39) was put in the wrong place.

The 1975 "peripherals handbook" has very similar text, but it *does* have a section header after the NPR details (line 13 is identical), and before the start of the (very similar) BR text ("A bus master that has gained control ... through a BRn/BGn arbitration transaction may issue an interrupt command to the processor.").

Lines

The UNIBUS is usually described as containing 56 lines. In its initial BC11A cable instantiation, the UNIBUS was composed of 72 wires (2 standard DEC board edge connectors, with 36 lines per connector); when not

counting the power and ground lines, this was reduced to the canonical 56.

Among the UNIBUS signals are:

- BR4-BR7 - Bus (Interrupt) Requests at priorities 4 (lowest) through 7 (highest)
- BG4-BG7 - Bus (Interrupt) Grants at priorities 4 (lowest) through 7 (highest)
- NPR - Non Processor (DMA) Request
- NPG - Non Processor (DMA) Grant
- MSYNC - Master Sync
- SSYNC - Slave Sync
- BBSY - Bus Busy
- SACK - Selection Acknowledge
- PA, PB - Parity control
- C0, C1 - Cycle Control

Cables

For many years, the cable used to carry the UNIBUS from one backplane to another was the BC11A cable, a pair of wide (3-3/4 inch) white flexible printed circuit flat cables, separated by a thin foam layer, with small printed circuit boards with edge connector fingers on each end of the cable. The latter plugged into 'UNIBUS In' and 'UNIBUS out' slots in backplanes. The flat cables actually contained 64 connectors each; every other trace was grounded, to prevent cross-talk between the signal lines.

DEC later developed a series of cards (the M9014, an extended height dual card, and the M9042 short dual card) which plug into the same slots, and contain three 2x20 headers for 40-conductor flat cables (known as H854 cables in DEC parlance); a pair of these, and three cables, perform the same role as a BC11A cable. Both of these cards use the same header pinout, so they may be used interchangeably.

Pinout

The following table gives the pinout for the flat cable form and SPC slot form. Pins are identified in the standard DEC manner; there are two connectors, A and B; pins on the component side are 1, those on the solder side are 2. Pins are identified by the 'DEC alphabet', A-V, with G, I, O and Q dropped.

Signal	Assertion	Termination	Cable Pin	SPC Pin
Initialization and Shutdown				
DC LO	L	Slow	BF2	CN1
AC LO	L	Slow	BF1	CV1
INIT	L	Fast	AA1	DL1
Arbitration				
NPR	L	Fast	AS2	FJ1
BR7	L	Fast	AT2	DD2
BR6	L	Fast	AU2	DE2
BR5	L	Fast	BC1	DF2
BR4	L	Fast	BD2	DH2
NPG	H	Grant	AU1	In-CA1; Out-CB1
BG7	H	Grant	AV1	In-DK2; Out-DL2
BG6	H	Grant	BA1	In-DM2; Out-DN2
BG5	H	Grant	BB1	In-DP2; Out-DR2
BG4	H	Grant	BE2	In-DS2; Out-DT2
SACK	L	Fast	AR2	FT2
Addressing				
A00	L	Fast	BH2	EH2
A01	L	Fast	BH1	EH1
A02	L	Fast	BJ2	EF1
A03	L	Fast	BJ1	EV2
A04	L	Fast	BK2	EU2
A05	L	Fast	BK1	EV1
A06	L	Fast	BL2	EU1
A07	L	Fast	BL1	EP2
A08	L	Fast	BM2	EN2
A09	L	Fast	BM1	ER1
A10	L	Fast	BN2	EP1
A11	L	Fast	BN1	EL1
A12	L	Fast	BP2	EC1
A13	L	Fast	BP1	EK2
A14	L	Fast	BR2	EK1
A15	L	Fast	BR1	ED2
A16	L	Fast	BS2	EE2
A17	L	Fast	BS1	ED1
Data				
D00	L	Fast	AC1	CS2

D01	L	Fast	AD2	CR2
D02	L	Fast	AD1	CU2, FE2%
D03	L	Fast	AE2	CT2, FL1%
D04	L	Fast	AE1	CN2, FN2%
D05	L	Fast	AF2	CP2, FF1%
D06	L	Fast	AF1	CV2, FF2%
D07	L	Fast	AH2	CM2, FH1%
D08	L	Fast	AH1	CL2, FK1%
D09	L	Fast	AJ2	CK2
D10	L	Fast	AJ1	CJ2
D11	L	Fast	AK2	CH1
D12	L	Fast	AK1	CH2
D13	L	Fast	AL2	CF2
D14	L	Fast	AL1	CE2
D15	L	Fast	AM2	CD2
Control				
C0	L	Fast	BU2	EJ2
C1	L	Fast	BT2	EF2
PA	L	Fast	AM1	CC1
PB	L	Fast	AN2	CS1
BBSY	L	Fast	AP2	FD1
MSYN	L	Fast	BV1	EE1
INTR	L	Fast	AB1	FM1
SSYN	L	Fast	BU1	EJ1, FC1%
Power				
Ground	N/A	N/A	AB2	
Ground	N/A	N/A	AC2	xC2
Ground	N/A	N/A	AN1	
Ground	N/A	N/A	AP1	
Ground	N/A	N/A	AR1	
Ground	N/A	N/A	AS1	
Ground	N/A	N/A	AT1	xT1
Ground	N/A	N/A	AV2	
Ground	N/A	N/A	BB2	
Ground	N/A	N/A	BC2	
Ground	N/A	N/A	BD1	
Ground	N/A	N/A	BE1	
Ground	N/A	N/A	BT1	

Ground	N/A	N/A	BV2	
+5	N/A	N/A	AA2	xA2
+5	N/A	N/A	BA2	
-15	N/A	N/A	N/A	xB2 (except 1A, 1B, 4A, 4B)

Entries of the form 'xYN' mean that that is available on all 4 connectors (A, B, C and D) in each slot.

% For forward compatibility, use the first pin rather than the second

See also

- Extended UNIBUS
- Small Peripheral Controller
- Modified UNIBUS Device
- UNIBUS memories
- QBUS