# UNIBUS

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The UNIBUS (or Unibus - the capitalization style changed over time) was the earliest of two bus technologies used with PDP-11s manufactured by DEC; it was first seen in the PDP-11/20, in 1970. Later, early VAX systems from that company used the UNIBUS as an I/O bus; it was also used in the small mainframe KS10-based model of the DECSYSTEM-20, to furnish it with inexpensive peripherals.

It was the only bus in most PDP-11 systems, and thus supported several capabilities: the ability of the CPU to read and write main memory, and device registers; and the ability for devices to do DMA transfers to memory, and to interrupt the CPU.

It could exist on a cable (the original physical form of implementation), and later, within a backplane (in 'Small Peripheral Controller (SPC)' or 'Modified UNIBUS Device (MUD)' slots). Up to 20 nodes (devices) could be connected to a single UNIBUS segment; additional segments could be connected via a bus repeater.

The UNIBUS contained 16 data lines, and 18 address lines, as well as a number of control lines. The 18 address lines allowed the addressing of a maximum of 256 KBytes. Typically, the top 8 KBytes of address space was reserved for the registers of the memory mapped I/O devices used in the PDP-11 architecture; this block is often referred to as the **I/O page**. The limit of 18 address lines was to prove a severe handicap in the later phases of the UNIBUS' operational life.

The bus was completely asynchronous, allowing a mixture of fast and slow devices. It also allowed arbitration (selection of the next *bus master*) while the current bus master was still performing data transfers, overlapping the two functions.

The design deliberately minimized the amount of redundant logic required in the system. For example, a system always contained more slave devices than master devices, so most of the complex logic required to implement asynchronous data transfers was forced into the relatively few master devices. For interrupts, only the *interrupt-fielding processor* needed to contain the complicated timing logic.

The end result was that most I/O controllers could be implemented with very simple logic; most of the critical logic was later implemented as a custom MSI IC.

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# Operation

Two control lines (C0 and C1) allowed the selection of four different data transfer cycle types in normal master/slave cycles:

- DATI (Data In, a read)
- DATIP (Data In/Pause, the first portion of a Read-Modify-Write operation. A DATO or DATOB operation completes this.)
- DATO (Data Out, a word write)
- DATOB (Data Out/Byte, a byte write)

During these operations, several signals (MSYN - Master Sync; SSYN - Slave Sync; and BBSY - Bus Busy) are used to synchronize between the master and slave, to indicate when the data is ready to be read (during a DATI/DATIP), or has been written (during a DATO/DATOB).

During an interrupt cycle, a fifth style of transfer was used to convey an *interrupt vector* from the interrupting device to the *interrupt-fielding processor*.

## **DMA and Interrupts**

Both DMA (in which a device must request control of the bus, so that it can peform a normal master/slave cycle, only with itself as the master), and interrupts, use the same mechanism for the device to communicate with the CPU to request something, and for the CPU to communicate with the device that it has granted the device's request.

There are bus request lines (NPR for DMA, and BR4-BR7 for interrupts), and bus grant lines (NPG for DMA, and BG4-7 for interrupts). The request lines are normal 'wired-OR' broadcast bus lines, but the grant lines are special; they are wired in series - one device's 'grant out' line is connected to the next device's 'grant in' line, starting the the CPU's 'grant out' line.

When a device receives a grant, it uses another bus line (SACK) to indicate that it received its grant; if the CPU sends a grant, and does not see a SACK in response, it know there was some sort of error.

### Documentation

Details of the operation of the UNIBUS may be found in the DEC publications "pdp11 peripherals handbook" (various editions from 1972 to 1977), and the "pdp11 bus handbook" (1979).

*NOTE:* There is a serious editing error in the latter volume, in the description of UNIBUS arbitration. On page 38, immediately after step 13 of the NPR Arbitration Sequence ("13. .... SACK must be negated before BBSY may be negated."), it says "A bus master may issue an interrupt command to the interrupt fielding processor."

Despite its location in the text, this does *not* apply to the "NPR arbitration sequence" being discussed above. There is an editing error - this text is (or *should be*) separate from the "NPR Arbitration Sequence" section just before it; it belongs with "BR Interrupt Arbitration Sequence" - that header (on pg. 39) was put in the wrong place.

The 1975 "peripherals handbook" has very similar text, but it *does* have a section header after the NPR details (line 13 is identical), and before the start of the (very similar) BR text ("A bus master that has gained control ... through a BRn/BGn arbitration transaction may issue an interrupt command to the processor.").

## Lines

The UNIBUS is usually described as containing 56 lines. In its initial BC11A cable instantiation, the UNIBUS was composed of 72 wires (2 standard DEC board edge connectors, with 36 lines per connector); when not

counting the power and ground lines, this was reduced to the canonical 56.

Among the UNIBUS signals are:

- BR4-BR7 Bus (Interrupt) Requests at priorities 4 (lowest) through 7 (highest)
- BG4-BG7 Bus (Interrupt) Grants at priorities 4 (lowest) through 7 (highest)
- NPR Non Processor (DMA) Request
- NPG Non Processor (DMA) Grant
- MSYNC Master Sync
- SSYNC Slave Sync
- BBSY Bus Busy
- SACK Selection Acknowledge
- PA, PB Parity control
- C0, C1 Cycle Control

#### Cables

For many years, the cable used to carry the UNIBUS from one backplane to another was the BC11A cable, a pair of wide (3-3/4 inch) white flexible printed circuit flat cables, separated by a thin foam layer, with small printed circuit boards with edge connector fingers on each end of the cable. The latter plugged into 'UNIBUS In' and 'UNIBUS out' slots in backplanes. The flat cables actually contained 64 connectors each; every other trace was grounded, to prevent cross-talk between the signal lines.

DEC later developed a series of cards (the M9014, an extended height dual card, and the M9042 short dual card) which plug into the same slots, and contain three 2x20 headers for 40-conductor flat cables (known as H854 cables in DEC parlance); a pair of these, and three cables, perform the same role as a BC11A cable. Both of these cards use the same header pinout, so they may be used interchangeably.

#### Pinout

The following table gives the pinout for the flat cable form and SPC slot form. Pins are identified in the standard DEC manner; there are two connectors, A and B; pins on the component side are 1, those on the solder side are 2. Pins are identified by the 'DEC alphabet', A-V, with G, I, O and Q dropped.

Signal	Assertion	Termination	Cable Pin	SPC Pin				
Initialization and Shutdown								
DC LO	L	Slow	BF2	CN1				
AC LO	L	Slow	BF1	CV1				
INIT	L	Fast	AA1	DL1				
Arbitration								
NPR	L	Fast	AS2	FJ1				
BR7	L	Fast	AT2	DD2				
BR6	L	Fast	AU2	DE2				
BR5	L	Fast	BC1	DF2				
BR4	L	Fast	BD2	DH2				
NPG	Н	Grant	AU1	In-CA1; Out-CB1				
BG7	Н	Grant	AV1	In-DK2; Out-DL2				
BG6	Н	Grant	BA1	In-DM2; Out-DN2				
BG5	Н	Grant	BB1	In-DP2; Out-DR2				
BG4	Н	Grant	BE2	In-DS2; Out-DT2				
SACK	L	Fast	AR2	FT2				
Addressing								
A00	L	Fast	BH2	EH2				
A01	L	Fast	BH1	EH1				
A02	L	Fast	BJ2	EF1				
A03	L	Fast	BJ1	EV2				
A04	L	Fast	BK2	EU2				
A05	L	Fast	BK1	EV1				
A06	L	Fast	BL2	EU1				
A07	L	Fast	BL1	EP2				
A08	L	Fast	BM2	EN2				
A09	L	Fast	BM1	ER1				
A10	L	Fast	BN2	EP1				
A11	L	Fast	BN1	EL1				
A12	L	Fast	BP2	EC1				
A13	L	Fast	BP1	EK2				
A14	L	Fast	BR2	EK1				
A15	L	Fast	BR1	ED2				
A16	L	Fast	BS2	EE2				
A17	L	Fast	BS1	ED1				
			Data					
D00	L	Fast	AC1	CS2				

D02LFastAD1CU2, FE2%D03LFastAE2CT2, FL1%D04LFastAE1CN2, FN2%D05LFastAF1CV2, FE2%D06LFastAF1CV2, FE2%D07LFastAH2CM2, FH1%D08LFastAH2CV2, FE2%D09LFastAH2CM2, FH1%D09LFastAH2CV2, FE2%D09LFastAH2CV2, FE2%D10LFastAH2CV2, FE2%D11LFastAH2CV2, FE2%D12JFastAH2CV2, FE2%D14FastAK2CH1D15LFastAK2CP2D14LFastAK2CP2D15LFastAL2CP2D14FastAU2CP2D15LFastBU2EP2C14FastBU2EP2C14FastAM2CP1D15LFastAM2CP1C14FastAM2CP1D15LFastAM2CP1C14FastAM2CP1C15FastAM2CP1D16LFastAM2C15FastAM2CP1C16KAKAAP2C17FastAM2CP1C18KAKA </th <th>D01</th> <th>L</th> <th>Fast</th> <th>AD2</th> <th>CR2</th>	D01	L	Fast	AD2	CR2			
D03LFastAE2CT2, FL1%D04LFastAE1CN2, FN2%D05LFastAF1CV2, FF3%D06LFastAF1CV2, FF3%D07LFastAH2CM2, FH1%D08LFastAH2CM2, FH1%D09LFastAI2CK2D09LFastAI2CK2D10LFastAK1CI2D11LFastAK1CH2D12LFastAL1CE2D13LFastAL2CF2D14FastAL2CC2D15LFastAL1CE2D14FastAM2CD2D15LFastAM2CD2D16LFastBU2CD2D17LFastSU2CD2D18LFastAM2CD2C19LFastAM2CD2C10LFastAM2CD1C11FastAM2CD1C11FastAM2CD1C11FastAM2CD1C11FastAM2CD1C11FastAM2CD1C11FastAM2CD1C12FastAM2CD1C13FastAM2CD1C14FastAM2CD1C15FastAM2CD1C16 <td>D02</td> <td>L</td> <td>Fast</td> <td>AD1</td> <td>CU2, FE2%</td>	D02	L	Fast	AD1	CU2, FE2%			
D04LFastAE1CN2, FN2%D05LFastAF2CP2, FF1%D06LFastAF1CV2, FP2%D07LFastAH2CM2, FH1%D08LFastAH2CL2, FK1%D09LFastAI1CI2D10LFastAI2CK2D11LFastAI2CH1D12LFastAI2CH2D13LFastAI2CP2D14LFastAI2CP2D15LFastAI2CP2D14LFastAI2CP2D15LFastAI2CP2D16LFastAI2CP2D17LFastAI2CP2D18LFastAI2CP2D19LFastBU2EP2C1SaFastSM1CI1C1FastAI2CP2PALFastAI2CP2PALFastAI2CP2SaLFastBU1EP1SaLFastAI2CP3SaLFastAI2CP3SaLFastBU1EP1SaLFastAI2CP3SaLFastAI2CP3SaLFastAI2CP3SaSaAI2CP3<	D03	L	Fast	AE2	CT2, FL1%			
D05LFastAF2CP2, FF1%D06LFastAF1CV2, FF2%D07LFastAH2CM2, FH1%D08LFastAH2CM2, FH1%D08LFastAH2CL2, FK1%D09LFastAI2CK2D10LFastAI2CM2D11LFastAK2CH1D12LFastAL2CP2D14LFastAL2CP2D15LFastAL2CP2D14LFastAL2CP2D15LFastAL2CP2C14FastAM2CD2C15LFastAM2CP2C16LFastAM2CP2C17FastAM2CP2PMLFastAM2CP2PMLFastAM2CP2PMLFastAM2CP2PMLFastAM2CP2StYNLFastAP2FD1StYNLFastAB2FM1StYNLFastAP2FD1GroudN/AAP3FAGroudN/AAP3FAGroudN/AAP3FAGroudN/AAP3FAGroudN/AAP3FAGroudN/AAP3FAGroudN/AAP3FA<	D04	L	Fast	AE1	CN2, FN2%			
D06LFastAF1CV2, FF2%D07LFastAH2CM2, FH1%D08LFastAH2CL2, FK1%D09LFastAJ2CK2D10LFastAJ2CM2D11LFastAK2CH1D12LFastAL2CF2D13LFastAL2CF2D14LFastAL2CF2D15LFastAL2CP2D14LFastAL2CP2D15LFastAL2CP2D14LFastAL2CP2D15LFastAL2CP2C1LFastAL2CP2C1StaFastBU2EP2C1StaFastBU2CS1PMLFastAP2FD1StaFastAP3CS1StaLFastAP3CS1StaLFastBU1EI1StaNAAB1CI1StaNAAS1GroundNANAAS1GroundNAAN4AS1GroundNASS1GroundNAAS1GroundNAAS1GroundNASS1GroundNASS1GroundNASS1GroundNASS1GroundNASS1G	D05	L	Fast	AF2	CP2, FF1%			
D07LFastAH2CM2, FH1%D08LFastAH1C12, FK1%D09LFastAJ2CK2D10LFastAJ1C12D11LFastAK2CH1D12LFastAL2CP2D13LFastAL2CP2D14LFastAL1CE2D15LFastAU2CD2C0LFastBU2C1C1FastBU2E2C1SFastBU2C1C1SFastAM1C1C1SFastAM1C1C1FastAM2CS1C1FastAM2CS1PMLFastAM2CS1SMSLFastAM2CS1SMSYLFastAM1C1SYNLFastBU1E1SYNLFastAB2FM1GroundN/AAG2SC2GroundN/AAG2SC2GroundN/AAG1GroundN/AAG1GroundN/AAG1GroundN/AAG2GroundN/ASC3GroundN/ASC3GroundN/ASC4GroundN/ASC4GroundN/ASC4GroundN/ASC4GroundN/ASC4 <td>D06</td> <td>L</td> <td>Fast</td> <td>AF1</td> <td>CV2, FF2%</td>	D06	L	Fast	AF1	CV2, FF2%			
D08LFastAH1CL2, FK1%D09LFastAJ2CK2D10LFastAJ1CJ2D11LFastAK2CH1D12LFastAL2CF2D13LFastAL2CF2D14LFastAL1CE2D15LFastAL2CF2D14LFastAL1CE2D15LFastBU2EJ2C0LFastBU2E12C1LFastBU2E12C1LFastAN2CS1PMLFastAN2CS1PMLFastAB1E11SYNLFastBV1E11SYNLFastAB2CGroundN/AAS2SC2SC2GroundN/AAS1SC3GroundN/AAS1SC3GroundN/AAS1SC4GroundN/AAS1GroundN/AAS1GroundN/ASC3GroundN/ASC3GroundN/ASC4GroundN/ASC4GroundN/ASC4GroundN/ASC4GroundN/ASC4GroundN/ASC4GroundN/ASC4GroundN/ASC4GroundN/ASC4 <td< td=""><td>D07</td><td>L</td><td>Fast</td><td>AH2</td><td>CM2, FH1%</td></td<>	D07	L	Fast	AH2	CM2, FH1%			
D09I. and FastAJ2CK2D10I. and FastAJ1CJ2D11I. and FastAK2CH1D12I. and FastAL2CF2D13I. and FastAL1CE2D14I. and FastAM2CD2D15I. and FastAM2CD2C0I. and FastBU2FJ2C1I. and FastBU2FJ2C1I. and FastBU2FJ2C1I. and FastAM1CC1PMI. and FastAM2CS1PMI. and FastAP2FD1BSYI. and FastBU1EE1SYNI. fastBU1EI1SYNI. fastAB1FM1GroundN/AAC2XC2GroundN/AAC1AC2GroundN/AAN1GroundN/AAN1GroundN/AAN1GroundN/AAN1GroundN/AAN1GroundN/AAN1GroundN/AAN1GroundN/AAN2GroundN/AAN2GroundN/AAN2GroundN/AAN2GroundN/AAN2GroundN/AM/AGroundN/AAN2GroundN/AAN2GroundN/AAN2GroundN/AAN2Ground<	D08	L	Fast	AH1	CL2, FK1%			
D10LFastAJ1CJ2D11LFastAK2CH1D12LFastAK1CH2D13LFastAL2CF2D14LFastAL1CE2D15LFastAM2CD2CFastBU2FJ2C1LFastBT2C1LFastAM1C1FastAM1CC1C1LFastAM1C1FastAM2CS1P8LFastAP2FBSYLFastBU1SYNLFastBU1SYNLFastBU1SYNLFastBU1GroundN/AN/AAB2GroundN/AN/AAB1GroundN/AAN1GroundN/AAS1GroundN/AAS1GroundN/AAS1GroundN/AAS1GroundN/AM/AGroundN/AM/AGroundN/AM/AGroundN/AM/AGroundN/AM/AGroundN/ABB2GroundN/AM/AGroundN/AM/AGroundN/AM/AGroundN/AM/AGroundN/AM/AGroundN/AM/AGroundN/AM/AGroundN/A	D09	L	Fast	AJ2	СК2			
D11LFastAK2CH1D12LFastAK1CH2D13LFastAL2CF2D14LFastAM2CD2D15LFastAM2CD2UUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUU	D10	L	Fast	AJ1	CJ2			
D12LFastAK1CH2D13LFastAL2CF2D14LFastAL1CE2D15LFastAM2CD2CO2LFastBU2EJ2C0LFastBT2EF2PALFastAM1CC1PBLFastAM2CS1BSYLFastBV1EE1NTRLFastBU1EJ1,FC1%SYNLFastBU1EJ1,FC1%GroundN/AN/AAR1GroundN/AAN1SC2GroundN/AAN1MIGroundN/AAN1GroundN/AAN1GroundN/AAN1GroundN/AAN1GroundN/AAN1GroundN/AAN1GroundN/AAN1GroundN/AAN1GroundN/AAN1GroundN/AAN1GroundN/AAN1GroundN/AM/AAN1GroundN/AN/AAN1GroundN/AN/AAN1GroundN/AMAAN1GroundN/AMAAN1GroundN/AMAAN1GroundN/AMABN2GroundN/AMABD1<	D11	L	Fast	AK2	CH1			
D13LFastAL2CF2D14LFastAL1CE2D15LFastAM2CD2D15LFastBU2EJ2C0LFastBT2EF2C1LFastAM1CC1PALFastAM2CS1BBSYLFastAP2FD1MSYNLFastAB1EE1NTRLFastAB1FM1SSYNLFastAB2I1,FC1%GroundN/AAA2XC2SC1GroundN/AAA1AS1GroundN/AAS1ST1GroundN/AAS1GroundN/AAS1GroundN/AAS1GroundN/AAS1GroundN/AAS1GroundN/ABB2GroundN/ABC2GroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/A	D12	L	Fast	AK1	CH2			
D14LFastAL1CE2D15LFastAM2CD2D15LFastBU2CD2C0LFastBU2EJ2C1LFastBT2EF2PALFastAM1CC1PBLFastAN2CS1BSYLFastBV1EE1MSYNLFastBU1E11NTRLFastBU1E11SSYNLFastBU1E11,FC1%GroundN/AN/AAB2SGroundN/AN/AAB1GroundN/AN/AAP1GroundN/AN/AAS1GroundN/AN/AAS1GroundN/AN/AAS1GroundN/AN/ABB2GroundN/AN/ABB2GroundN/AN/ABB2GroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGround <td>D13</td> <td>L</td> <td>Fast</td> <td>AL2</td> <td>CF2</td>	D13	L	Fast	AL2	CF2			
D15LFastAM2CD2CD4LFastBU2EJ2C1LFastBT2EF2PALFastAM1CC1PBLFastAN2CS1BBSYLFastBV1EE1MSYNLFastBU1EE1INTRLFastBU1EJ1,FC1%SSYNLFastBU1EJ1,FC1%GroundN/AN/AAB2AP2GroundN/AN/AAB2AP2GroundN/AN/AAB2AP2GroundN/AN/AAB2AP2GroundN/AN/AAT1GroundN/AAK1GroundN/AAV2GroundN/AAV2GroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/A	D14	L	Fast	AL1	CE2			
ControlControlC0LFastBU2EJ2C1LFastBT2EF2PALFastAM1CC1PBLFastAN2CS1BSSYLFastAP2FD1MSYNLFastBU1EE1INTRLFastBU1EI1, FC1%SSYNLFastBU1EJ1, FC1%GroundN/AN/AAB2AC2GroundN/AN/AAC2xC2GroundN/AN/AAR1GroundN/AN/AAS1GroundN/AN/AAS1GroundN/AN/ABB2GroundN/AN/ABC2GroundN/AN/ABD1GroundN/AN/ABN2SC2GroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/AM/AN/AGroundN/AM/AN/AGroundN/AM/AN/AGroundN/AM/AN/AGroundN/AM/AN/AGroundN/AM/	D15	L	Fast	AM2	CD2			
C0LFastBU2EJ2C1LFastBT2EF2PALFastAM1CC1PBLFastAN2CS1BSYLFastAP2FD1MSYNLFastBV1EE1MSYNLFastBU1EJ1, FC1%SSYNLFastBU1EJ1, FC1%GroundN/AN/AAB2GroundN/AN/AAP1GroundN/AAN1GroundN/AAS1GroundN/AAS1GroundN/AAV2GroundN/AAS1GroundN/AAD1GroundN/AAS1GroundN/AAS1GroundN/AAD2GroundN/ABB2GroundN/AN/ABD1GroundN/AM/ABD1GroundN/AN/ABD1M/AGroundN/AM/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/A <td< td=""><td colspan="8">Control</td></td<>	Control							
C1LFastBT2EF2PALFastAM1CC1PBLFastAN2CS1BBSYLFastAP2FD1MSYNLFastBV1EE1MSYNLFastBU1EJ1, FC1%SSYNLFastBU1EJ1, FC1%GroundN/AN/AAB2GroundN/AN/AAC2xC2GroundN/AAN1GroundN/AAR1GroundN/AAR1GroundN/AAS1GroundN/AAS1GroundN/ABB2GroundN/ABC2GroundN/ABD1GroundN/AN/ABB2M/AM/AGroundN/ABD1GroundN/ABD1GroundN/ABD1GroundN/ABD1GroundN/AN/ABD1M/AGroundN/ABD1GroundN/AN/ABD1M/AGroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/A<	C0	L	Fast	BU2	EJ2			
PALFastAM1CC1PBLFastAN2CS1BBSYLFastAP2FD1MSYNLFastBV1EE1MSYNLFastAB1FM1SSYNLFastBU1EJ1, FC1%SSYNLFastAB2GroundN/AN/AAB2GroundN/AN/AAC2xC2GroundN/AN/AAN1GroundN/AN/AAP1GroundN/AN/AAS1GroundN/AN/AAS1GroundN/AN/AAS1GroundN/AN/AAS1GroundN/AN/AAS1GroundN/AN/ABB2GroundN/AN/ABB2GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABD1GroundN/A	C1	L	Fast	BT2	EF2			
PBLFastAN2CS1BBSYLFastAP2FD1MSYNLFastBV1EE1INTRLFastAB1FM1SSYNLFastBU1EJ1,FC1%GroundN/AAB2GroundN/AN/AAB2XC2GroundN/AN/AAN1GroundN/AN/AAP1GroundN/AN/AAS1GroundN/AAS1GroundN/AAV2GroundN/AAS1GroundN/AAS1GroundN/AB2GroundN/ABB2GroundN/ABC2GroundN/ABD1GroundN/ABE1GroundN/ABE1GroundN/ABD1	PA	L	Fast	AM1	CC1			
BBSYLFastAP2FD1MSYNLFastBV1EE1INTRLFastAB1FM1SSYNLFastBU1EJ1,FC1%SroundN/AAB2Image: Common Sector Se	PB	L	Fast	AN2	CS1			
MSYNLFastBV1EE1INTRLFastAB1FM1SSYNLFastBU1EJ1, FC1%FowerGroundN/AN/AAB2GroundN/AN/AAC2xC2GroundN/AN/AAN1GroundN/AN/AAP1GroundN/AN/AAS1GroundN/AN/AAS1GroundN/AN/AAV2GroundN/AN/ABB2GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABE1GroundN/AN/ABT1	BBSY	L	Fast	AP2	FD1			
INTRLFastAB1FM1SSYNLFastBU1EJ1, FC1%SSYNLFastBU1EJ1, FC1%GroundN/AN/AAB2GroundN/AN/AAB2xC2GroundN/AN/AAN1GroundN/AN/AAP1GroundN/AN/AAR1GroundN/AN/AAS1GroundN/AN/AAS1GroundN/AN/AAS1GroundN/ABB2GroundN/AN/ABB2GroundN/AN/ABD1GroundN/AN/ABD1GroundN/AN/ABE1GroundN/AN/ABT1	MSYN	L	Fast	BV1	EE1			
SSYNLFastBU1EJ1, FC1%GroundN/AN/AAB2GroundN/AN/AAB2GroundN/AN/AAC2xC2GroundN/AN/AAN1GroundN/AN/AAP1GroundN/AN/AAR1GroundN/AN/AAS1GroundN/AN/AAT1GroundN/AN/AAV2GroundN/AN/ABB2GroundN/AN/ABC1GroundN/AN/ABE1GroundN/AN/ABE1GroundN/AN/ABT1	INTR	L	Fast	AB1	FM1			
PowerGroundN/AN/AAB2GroundN/AN/AAC2xC2GroundN/AN/AAN1GroundN/AN/AAP1GroundN/AN/AAR1GroundN/AN/AAR1GroundN/AN/AAR1GroundN/AN/AAS1GroundN/AN/AAT1GroundN/AN/AAV2GroundN/AN/ABB2GroundN/AN/ABC2GroundN/AN/ABD1GroundN/AN/ABE1GroundN/AN/ABT1	SSYN	L	Fast	BU1	EJ1, FC1%			
GroundN/AN/AAB2GroundN/AN/AAC2xC2GroundN/AN/AAN1GroundN/AN/AAP1GroundN/AN/AAR1GroundN/AN/AAS1GroundN/AN/AAT1GroundN/AN/AAV2GroundN/AN/ABB2GroundN/AN/ABC1GroundN/AN/ABE1GroundN/AN/ABT1				Power				
GroundN/AAC2xC2GroundN/AN/AAN1GroundN/AN/AAP1GroundN/AN/AAR1GroundN/AN/AAS1GroundN/AN/AAS1GroundN/AN/AAT1GroundN/AN/ABB2GroundN/AN/ABC2GroundN/AN/ABD1GroundN/AN/ABE1GroundN/AN/ABT1	Ground	N/A	N/A	AB2				
GroundN/AN/AAN1GroundN/AN/AAP1GroundN/AN/AAR1GroundN/AN/AAS1GroundN/AN/AAT1GroundN/AN/AAV2GroundN/AN/ABB2GroundN/AN/AGroundN/ABC2GroundN/AN/AGroundN/ABD1GroundN/AN/ABE1N/AGroundN/AN/A	Ground	N/A	N/A	AC2	xC2			
GroundN/AN/AAP1GroundN/AN/AAR1GroundN/AN/AAS1GroundN/AN/AAT1GroundN/AN/AAV2GroundN/AN/ABB2GroundN/AN/ABC2GroundN/AN/AGroundN/AN/AGroundN/AN/AGroundN/ABD1GroundN/AN/ABE1N/AN/A	Ground	N/A	N/A	AN1				
GroundN/AAR1GroundN/AAS1GroundN/AAT1GroundN/AAV2GroundN/ABB2GroundN/ABC2GroundN/ABD1GroundN/ABE1GroundN/ABT1	Ground	N/A	N/A	AP1				
GroundN/AAS1GroundN/AAT1xT1GroundN/AAV2GroundN/ABB2GroundN/ABC2GroundN/ABD1GroundN/ABE1GroundN/ABT1	Ground	N/A	N/A	AR1				
GroundN/AAT1xT1GroundN/AN/AAV2GroundN/AN/ABB2GroundN/AN/ABC2GroundN/AN/ABD1GroundN/AN/ABE1GroundN/AN/ABT1	Ground	N/A	N/A	AS1				
GroundN/AAV2GroundN/AN/ABB2GroundN/AN/ABC2GroundN/AN/ABD1GroundN/AN/ABE1GroundN/AN/A	Ground	N/A	N/A	AT1	xT1			
GroundN/ABB2GroundN/AN/AGroundN/AN/AGroundN/AN/ABD1N/ABE1GroundN/AN/ABT1	Ground	N/A	N/A	AV2				
GroundN/ABC2GroundN/AN/AGroundN/AN/ABD1N/ABE1GroundN/AN/ABT1	Ground	N/A	N/A	BB2				
GroundN/ABD1GroundN/AN/ABE1GroundN/AN/A	Ground	N/A	N/A	BC2				
GroundN/ABE1GroundN/AN/ABT1	Ground	N/A	N/A	BD1				
Ground N/A N/A BT1	Ground	N/A	N/A	BE1				
	Ground	N/A	N/A	BT1				

Ground	N/A	N/A	BV2	
+5	N/A	N/A	AA2	xA2
+5	N/A	N/A	BA2	
-15	N/A	N/A	N/A	xB2 (except 1A, 1B, 4A, 4B)

Entries of the form 'xYN' mean that that is available on all 4 connectors (A, B, C and D) in each slot.

% For forward compatibility, use the first pin rather than the second

## See also

- Extended UNIBUS
- Small Peripheral Controller
- Modified UNIBUS Device
- UNIBUS memories
- QBUS

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