AccessionIndex: TCD-SCSS-T.20150608.005
Accession Date: 16-Apr-2015
Accession By: Dr.Brian Coghlan
Object name: Parallel Processing Cell for MFP
Vintage: c.1987
Synopsis: Signal processor for the underwater Microstructure Flux Probe (MFP) developed for University of Western Australia.

Description:
This signal processor was designed and constructed by Dr.Brian Coghlan of the Dept.Computer Science, Trinity College Dublin, whilst on leave at the Centre for Environmental Fluid Dynamics (CEFD) at the University of Western Australia, supported by the CEFD and particularly by its Director, Prof.Jorg Imberger. The design was integral to a new *Microstructure Flux Probe* (MFP), a totally autonomous underwater probe with a unique combination of instrumentation, including a 2-d laser Doppler anenometer (LDA) and a submarine bouyancy system.

The general principle of an LDA may be illustrated by illuminating a sample volume within a fluid with two coherent beams of monochromatic light. Where they intersect a fringe pattern will be established. Particles transported with the fluid through the volume will scatter a burst of light with an intensity variation as per the fringe pattern, where the Doppler frequency of variation will depend upon the particle velocity.

In the MFP, each dimension of the LDA signal processing was performed as a 2-stage pipeline. Firstly, an adaptive burst-searching constant-false-alarm-rate (CFAR) detection algorithm in the frequency domain was used to detect the presence of a valid burst. Secondly, once the burst was isolated, the Doppler-shift frequency (proxy for velocity) estimation was performed.

Each dimension was processed on a separate Qbus board (i.e. one per axis) that had two simple, low-power, parallel processing cells, each with a Transputer to handle concurrency and communications, plus loosely-coupled slave and vector processors.

The slave processor consisted of a Weitek WTL7136 Program Sequencer (PSU), WTL7137 Integer Processor (IPU) and WTL3132 FPU, executing 64-bit micro-instructions that had been written by the Transputer to a writeable control store (WCS). The FPU and IPU were connected to a transputer link adapter and RAM. Microprograms were effectively OCCAM processes, communicating via the link.

The vector signal processor was a Zoran ZR34161 VSP and RAM, attached to the Transputer bus, plus bus arbitration. Once commanded to start by the Transputer, the VSP executed its own instruction stream and fetched its own data.

Accession Index	Object with Identification
TCD-SCSS-T.20150608.005.01	Parallel Processing Cell (PPC).
TCD-SCSS-T.20150608.005.02	Vector Signal Processor (VSP).
TCD-SCSS-T.20150608.005.03	QBus Chassis. S/N: ???

References

1. Coghlan,B.A., *A public-domain MicroVAX-compatible vector processor optimised for signal processing*, Proc. International Symposium for Signal Processing and its Applications, Brisbane, Aug.26-28th 1987.

2. Coghlan,B.A., *A velocity extraction system for a 2-d Laser Doppler Anenometer in an underwater probe*, unpublished paper, see associated folder in this catalog.

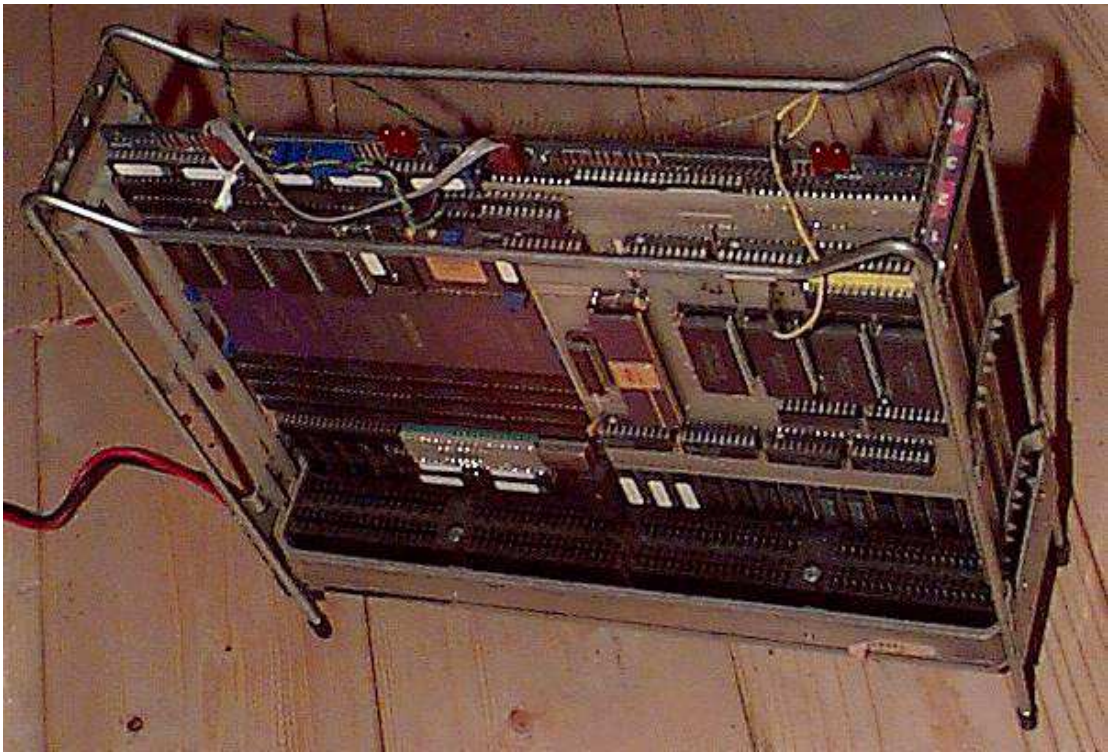

Figure 1: Parallel Processing Cell Board in Qbus Chassis, three-quarter view

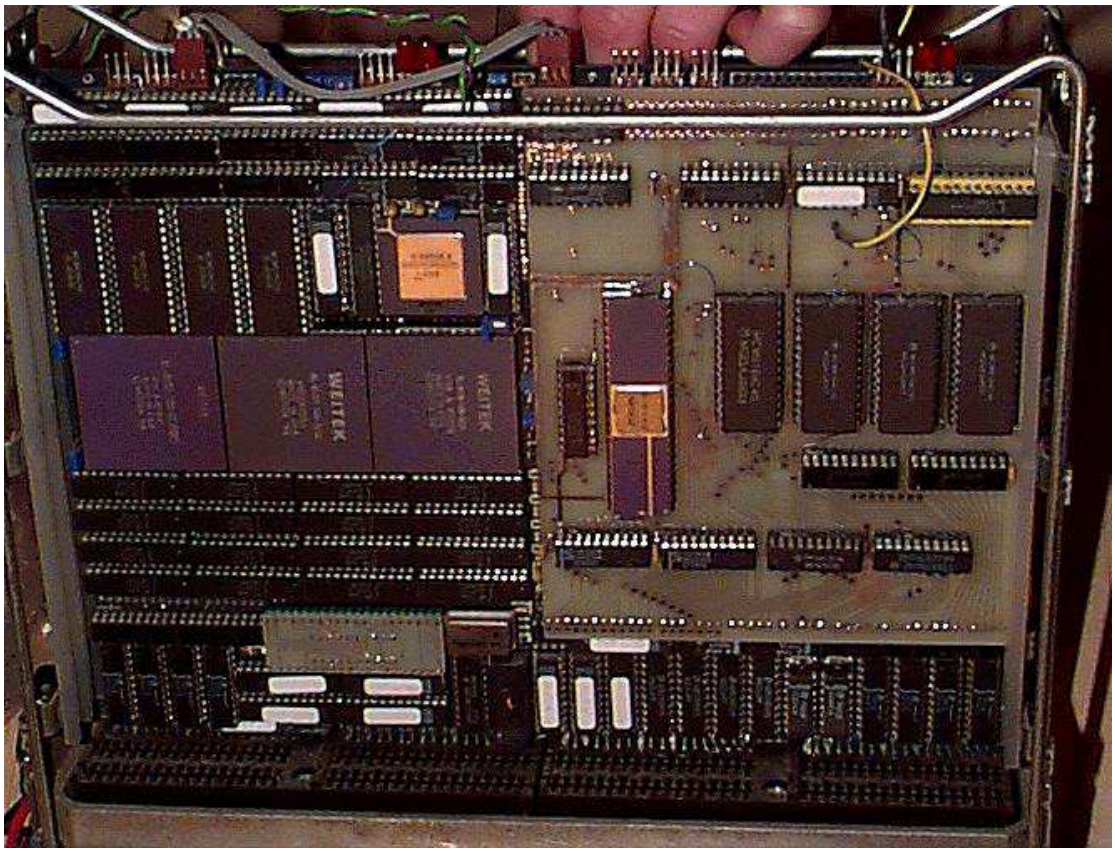

Figure 2: Parallel Processing Cell Board front view

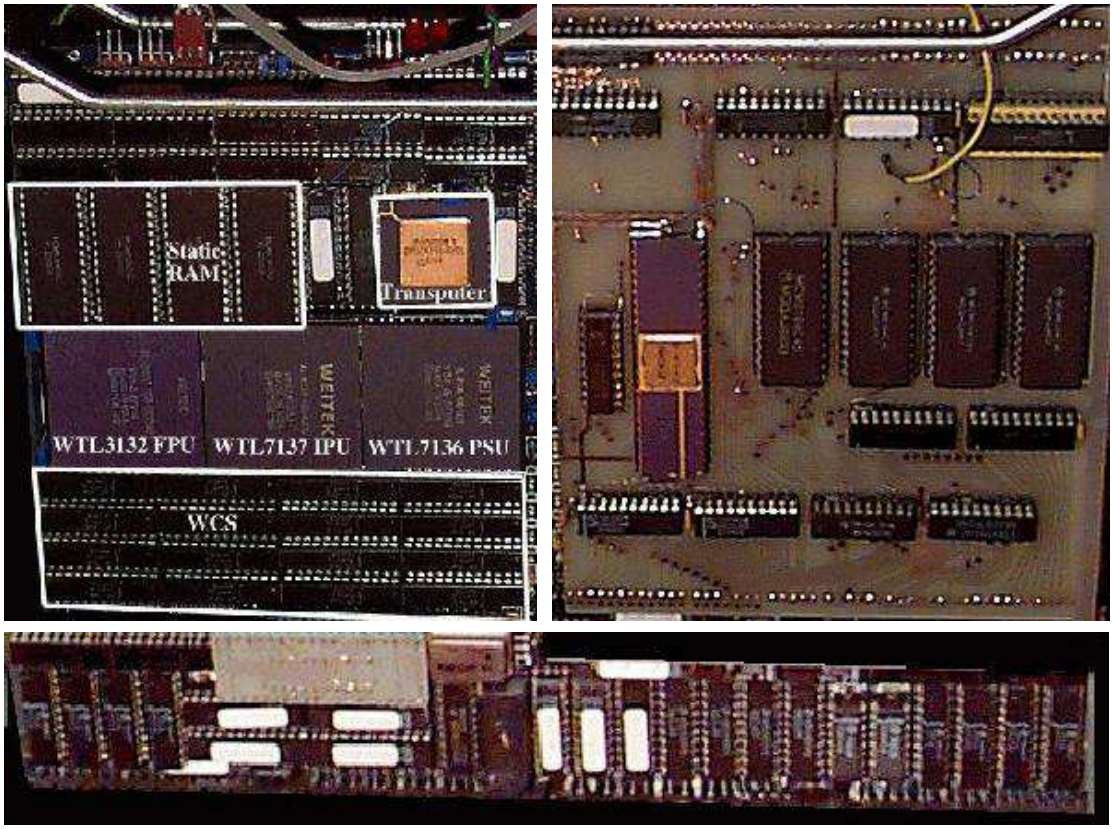

Figure 3: Parallel Processing Cell Board functional blocks
Top Left: left Parallel Processing Cell (PPC)
Top Right: Vector Signal Processor (VSP) mounted on top of right PPC
Bottom: Qbus Interface