AccessionIndex: TCD-SCSS-T.20150126.001
Accession Date: 26-Jan-2015
Accession By: Dr.Brian Coghlan
Object name: InMOS IMS-B003
Vintage: c.1986
Synopsis: Transputer evaluation board with four T414 Transputers, each with 256kB
DRAM. S/N: 221-CBRD-015 A039.

Description:
The IMS-B003 Transputer Evaluation Board was manufactured by InMOS Ltd,
Bristol, UK, to support basic evaluation and development of the transputer
technologies. As the transputer was a pragmatic realisation of Tony Hoare's CSP
(Communicating Sequential Processes) it was widely used for teaching concurrency
principles and parallel programming in the European third-level computer science
community.

A transputer can be viewed as a process that runs its own process tree, where the sub-
processes communicate via internal channels. Collections of transputers can be
aggregated as a higher-level process tree, communicating via external channels. The
processes and channels are managed by a built-in microcoded kernel. The internal
channels signal via memory slots, whereas external channels are real physical 20Mbps
links. The transputer has a stack-oriented RISC-inspired microcoded instruction set
that includes kernel primitives. Each transputer included fast on-chip SRAM and a
built-in configurable DRAM controller.

The transputer was a brainchild of Iann Barron, David May and Robert Milne of
InMOS. The company was set up by Barron and Americans Dick Petritz and Paul
Schroeder with funding from the British Government. InMOS's first transputer
product was the T414, with 32-bit integer arithmetic instructions and 2kB memory,
announced in 1983 and released in 1984. This was followed in 1987 by the T800 that
included 64-bit IEEE754 floating-point instructions and 4kB memory. Both were
supported by a new programming language, Occam, for which compilers and the
interactive Transputer Design System (TDS) were supported on various platforms,
most notably the IBM PC and VAX VMS.

Ref: InMOS B003 technical note 10, see tn10.pdf in folder:
The B003 is a double-extended Eurocard with four T414 Transputers, each with
256kB DRAM. Each transputer has four 20Mbps communication links. Links 2 and 3
of each of the transputers are connected in a square ringlet, and the other two links of
each transputer are connected to an edge connector.

The interface from the B003 is via a 96 way DIN-41612 edge connector. Links 0 and
1 from each transputer are brought out via the edge connector together with the
system services signals. The connector is a simple superset of the 64 way connector
used by B001, B002 and other InMOS evaluation boards.

The board uses a minimum of glue logic. The system services shared by all the
transputers consist of a single 5 MHz clock and three TTL chips. Each transputer uses
a further three TTL chips to interface to its eight DRAM chips. The minimal glue

logic introduces minimal access time overhead for the DRAM, and the T414-15 completes a memory access in four processor cycles.

The square ringlet connection of transputers makes it possible to test the board down a single link, minimizes edge connector pin count, and makes it possible to build a wide variety of networks.

Accession Index	Object with Identification
TCD-SCSS-T.20150126.001	InMOS IMS-B003 Rev.A Transputer Evaluation Board. S/N: 221-CBRD-015 A039

Trivia: Iann Barron was also the designer of the Elliot 803 and the CTL Modular One machines.
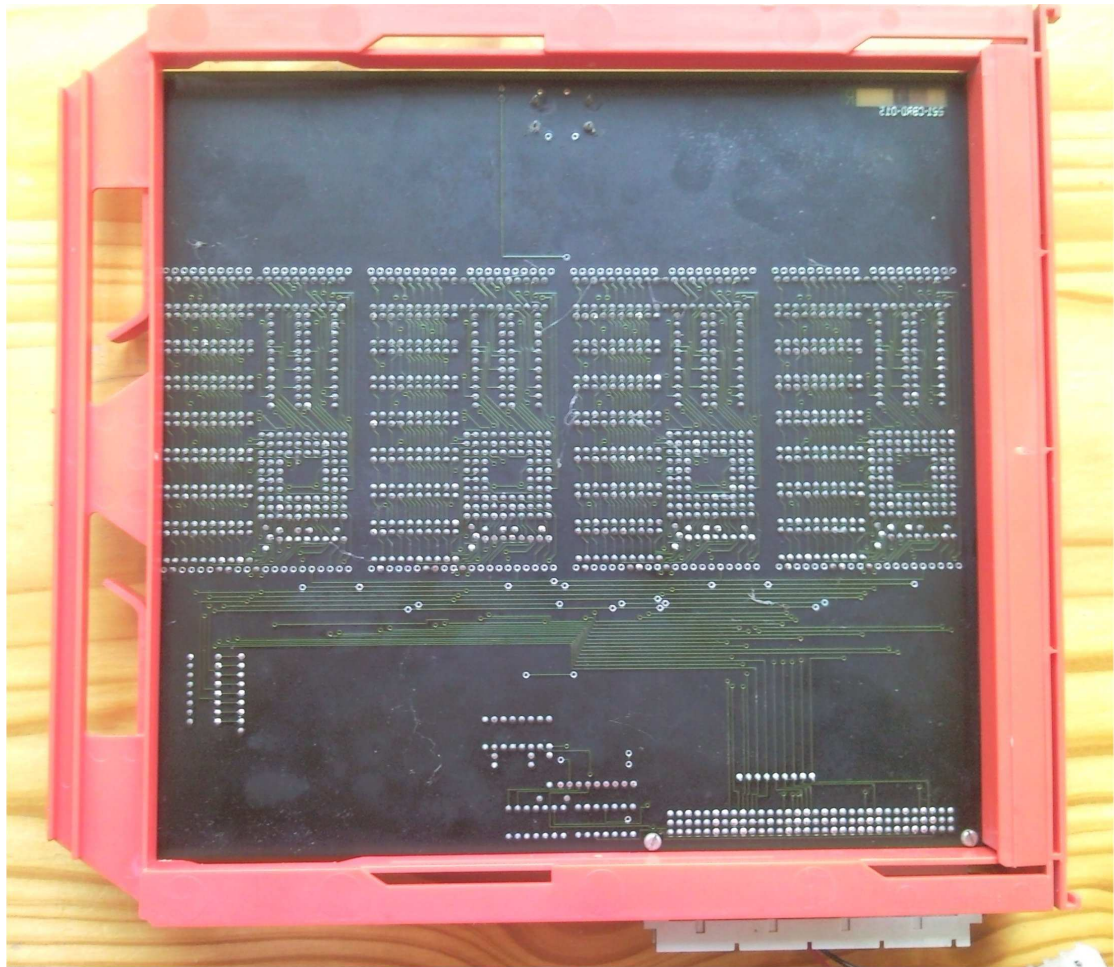

Figure 1: InMOS IMS-B003 front three-quarter view
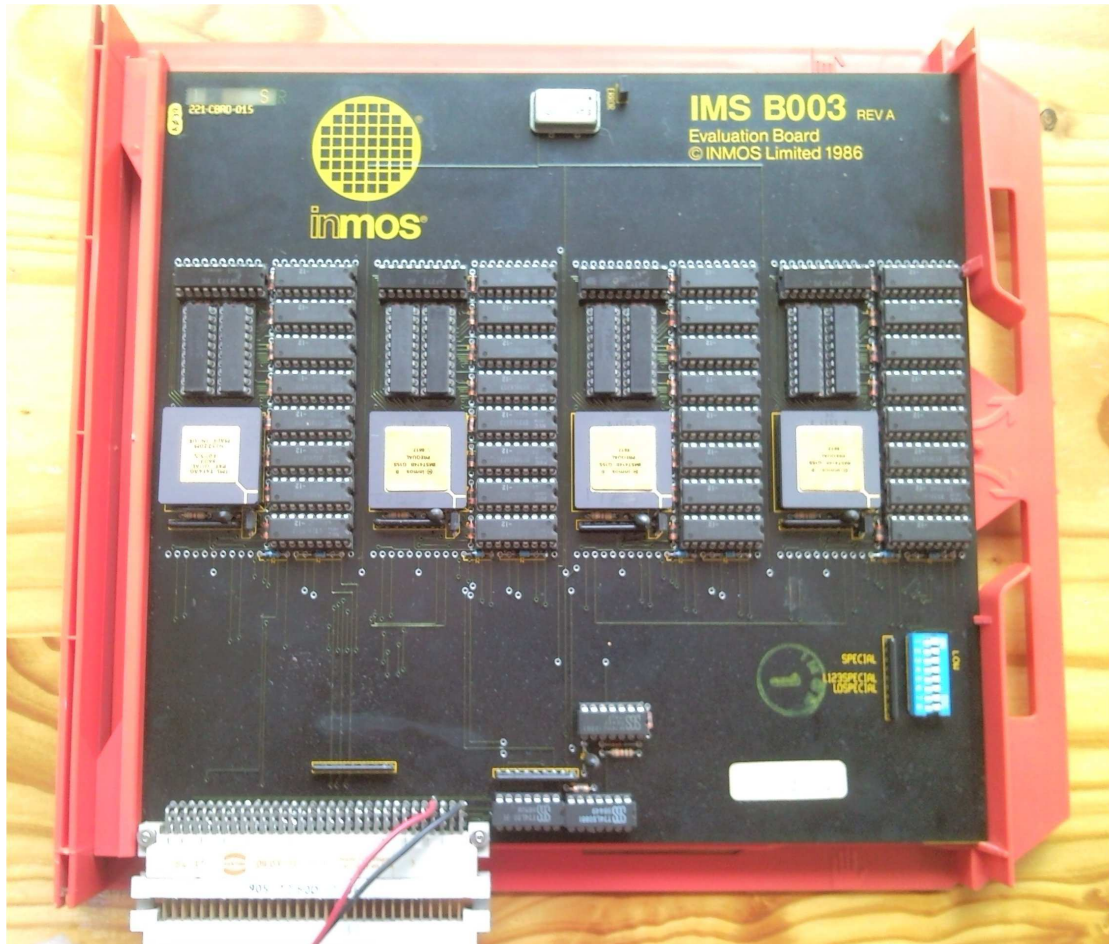
Figure 2: InMOS IMS-B003 front view
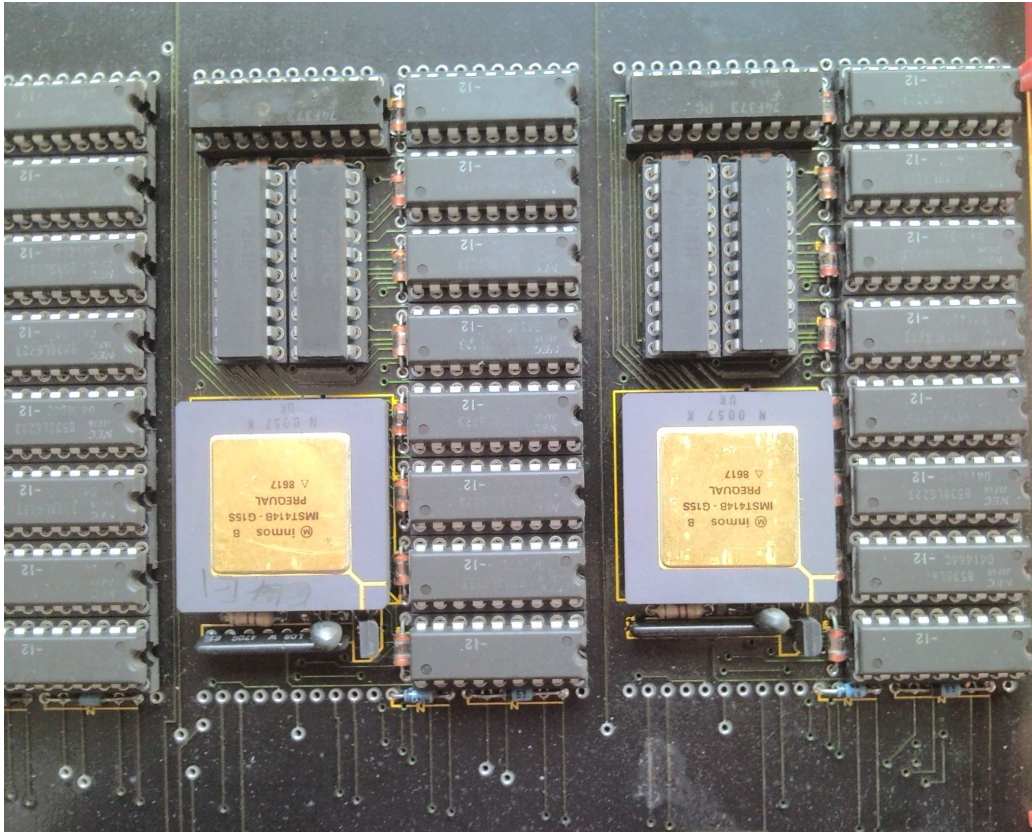
Figure 3: InMOS IMS-B003 rear view

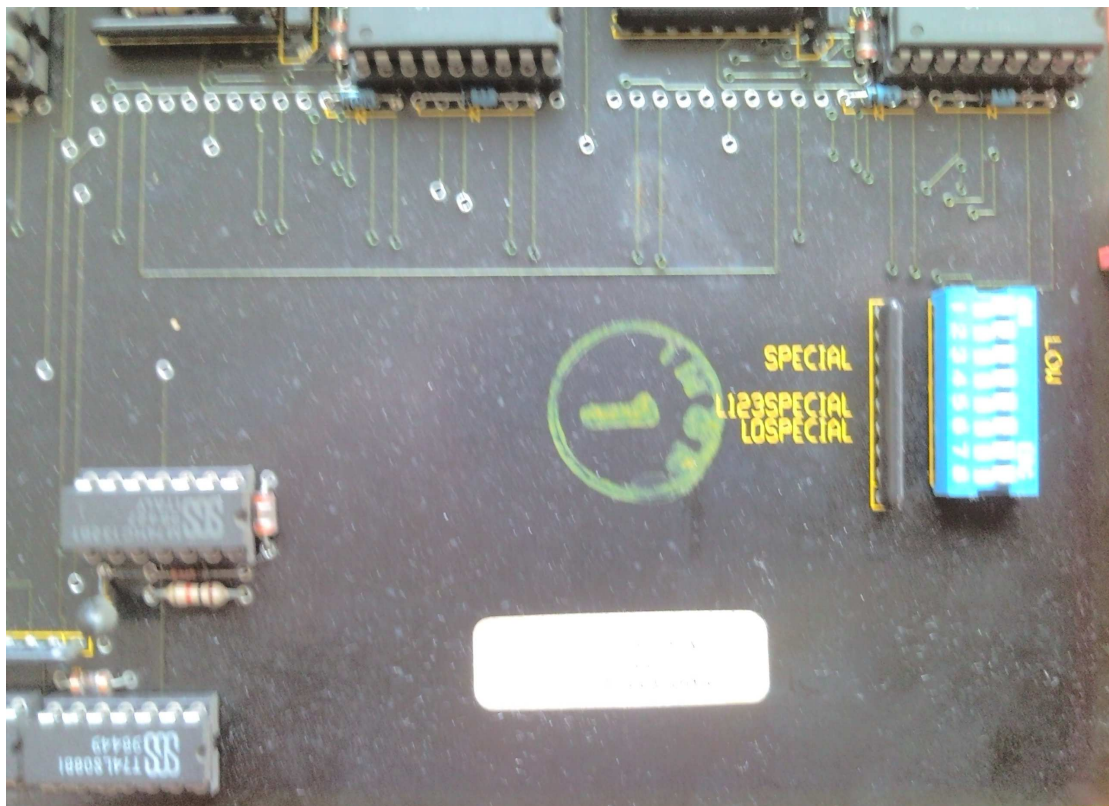*Figure 4: InMOS IMS-B003 transputer subunit closeup*
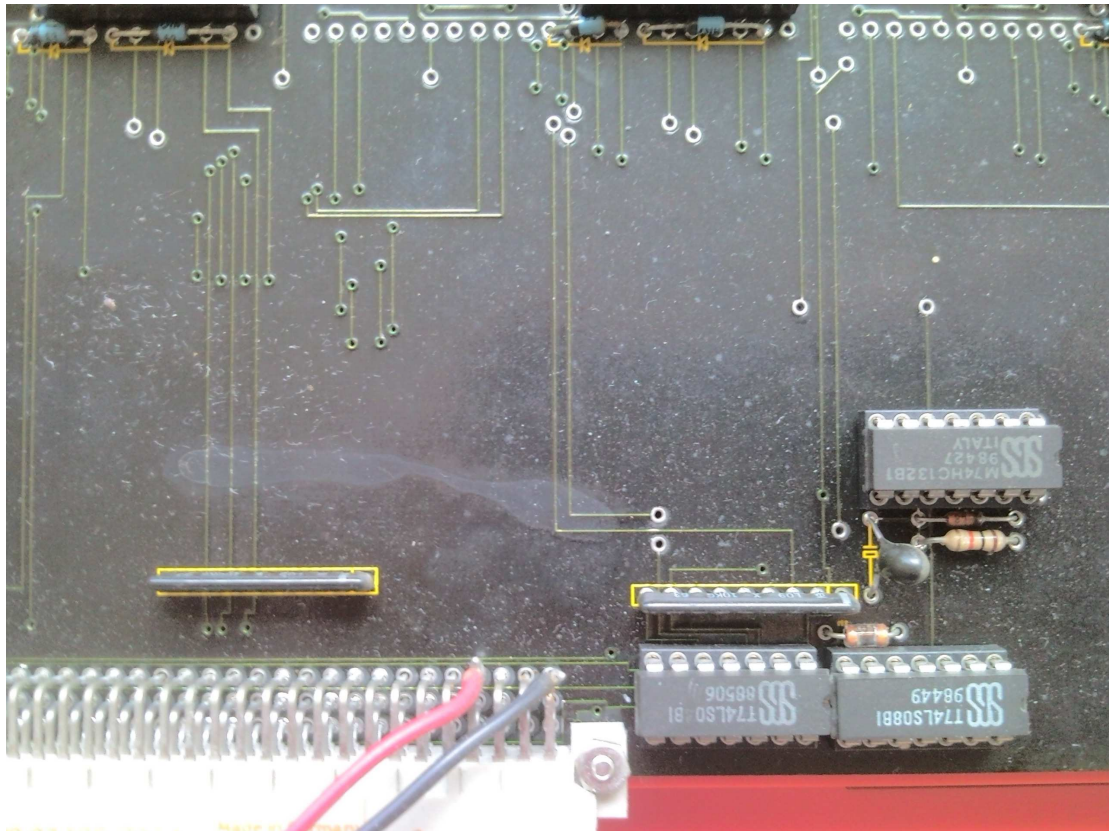

Figure 5: InMOS IMS-B003 configuration switch closeup
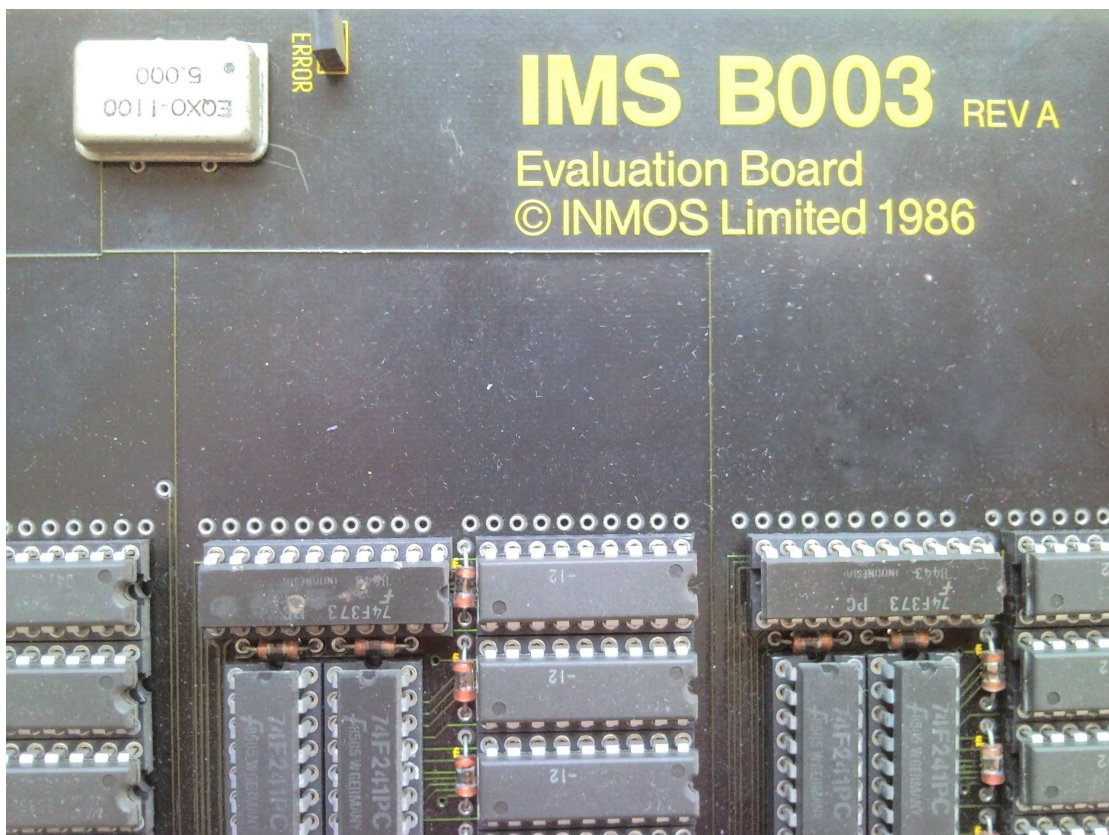
Figure 6: InMOS IMS-B003 system services logic closeup

Figure 7: InMOS IMS-B003 manufacturing label
InMOS IMS B003 Rev.A

Figure 8: InMOS IMS-B003 serial number
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