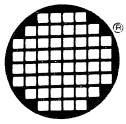


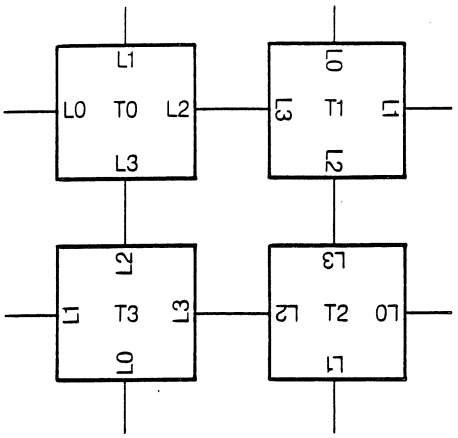
IMS B003 evaluation board

Disclaimer

Every effort has been made to test this product and its operation with the transputer development system. Note, however, that the board contains a 'prequal' version of the transputer on which engineering characterization and life tests have not been performed.

72 BRD 018 00

Contents



The IMS B003 evaluation board is a double extended Eurocard containing four T414 transputers, each with 256 Kbytes of dynamic RAM.

The board is one of a family of compatible evaluation boards, and is the first in this family to include more than one transputer. The B003 will normally be used with one of these other evaluation boards, from which programs are downloaded to the B003. This manual assumes the user has, and is familiar with, such an evaluation board.

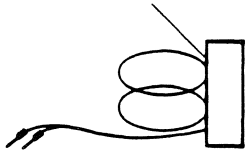
This manual details the product specific aspects of the IMS B003, and contains all the data necessary to power up, test and program the board.

Other information relevant to all transputer products is contained in the occam programming manual (supplied with INMOS software products and available as a separate publication), and the transputer reference manual (supplied with this board). This board is designed to be used in conjunction with a transputer development system, and reference should be made to the transputer development system user manual (supplied with the development system), for details of how to compile and load programs for a network of boards.

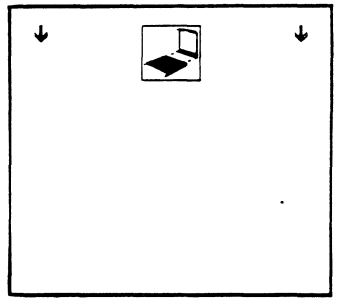
Two application notes are particularly relevant to the B003. One (The design of a multitransputer evaluation board) describes the B003 design and how the four transputers and their RAM were put into the small area they occupy. The other (Configuring various networks using the IMS B003) gives diagrams and occam configuration programs for a wide variety of networks. These include a ring, a square array, a 'butterfly' - folded binary structure, and a hypercube. The application note also shows how to bootstrap a fully connected network.

1.1 Opening the bag

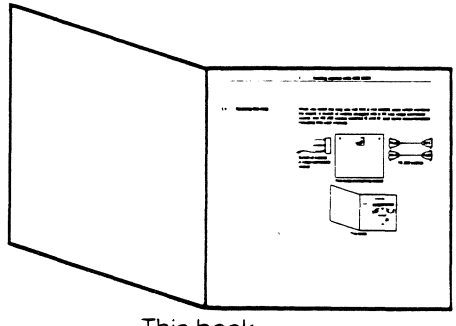
When you open the bag you will find a red plastic case which contains the board, a set of cables plugged into a 96 way edge connector socket, and some documentation including this user manual.



Bunch of cables in edge connector socket



Red case containing board



This book

1.2 Mounting the board for use

The red plastic case which holds the board also acts as a mounting rack for up to six boards. The board itself is mounted on a frame, which slides into the top of the case.

To remove the board and mount it on the top of the case:

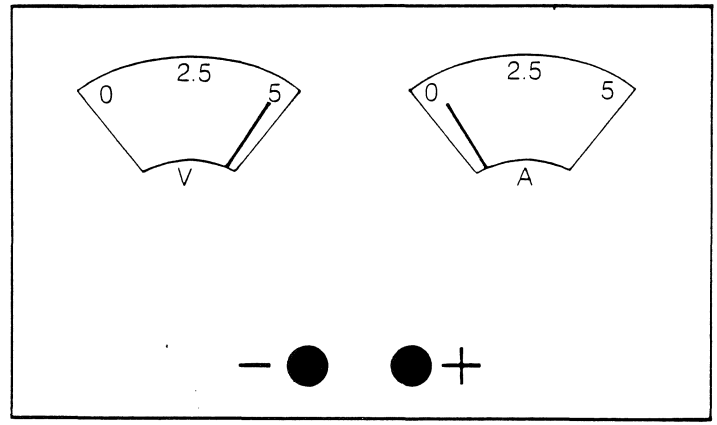
1. Place the red case on a table so the white arrows are facing towards you. You should also be able to see the Anti-Static warning facing you on the frame.
2. With your thumbs, gently push apart the clips on either side of the frame so that the frame is released.
3. Tilt the case so that the frame slides out.
4. Without touching the circuit board, withdraw the frame from the case.
5. When you do touch the board, touch it first at either end of the 96 way edge connector; the pins at both ends are GND.
6. Turn the frame so the Anti-Static warning faces down and the component side of the board faces you.
7. Place the frame over the white arrows on the case. Gently slide the frame towards you into the slots either side of the case, as shown in the white painted picture on the case.
8. When you come to plug the cables into the board, do so carefully.

Up to six frames can be mounted onto the case.

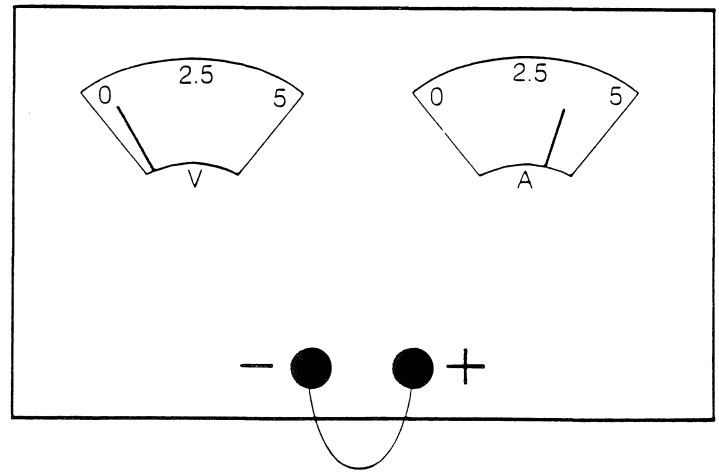
1.3 Power supply

If you already have a freestanding transputer evaluation board (such as B001 or B002) and wish to use the B003 with it, the current limit on the power supply should be increased by 4 Amps, and the banana plugs of the B003 plugged into the back of the freestanding board's banana plugs.

If you wish to use the B003 with a B004, or other transputer evaluation board which is mounted in a host computer, find a Lab power supply capable of delivering 5 Amps at 5V, and set it to 5V, current limiting at 4 Amps.



Voltage setup



Current setup

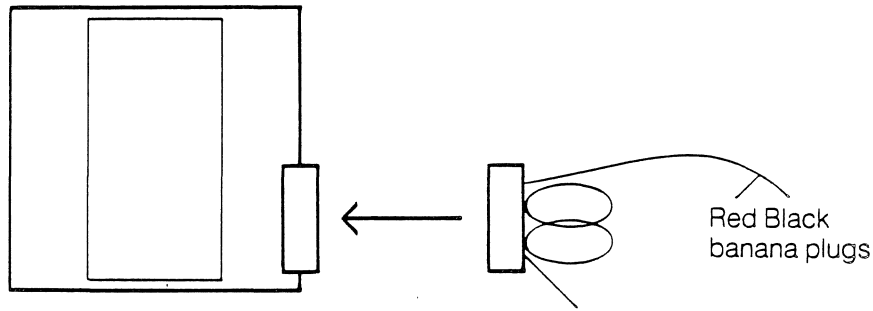
1.4 Connecting up to the power supply

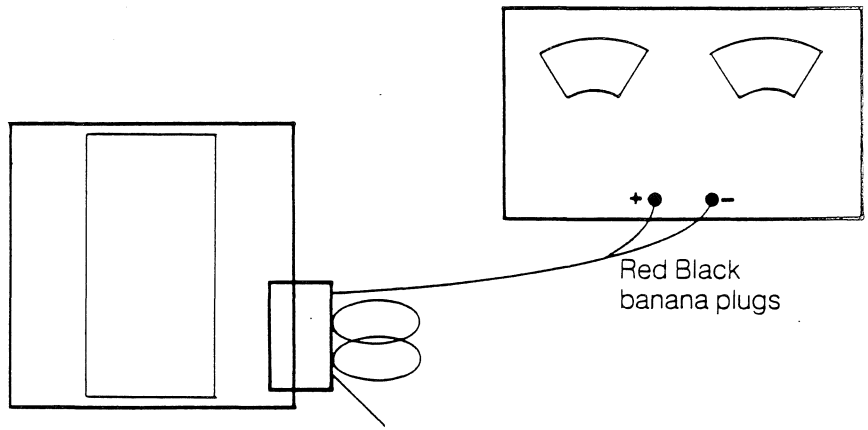
Switch the power supply off.

Leave the cables plugged into the edge connector socket and plug this socket onto the board.

Among the cables you will find a red banana plug and a black banana plug. The black banana plug connects to 0V of a power supply and the red banana plug connects to +5V of the power supply. Check you have connected the power the right way round and switch on.

The B003 does not have a LED to show that the power is switched on. The yellow Error LED may (or may not) light when the board is switched on.

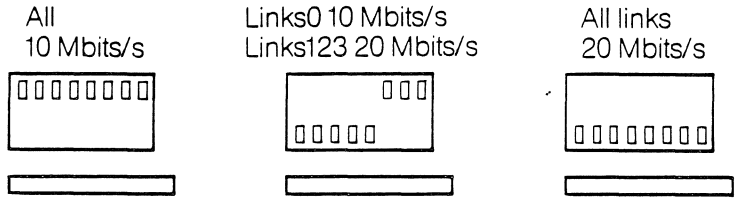




1.5 Checking the setting of the coding switches

Check the coding switches on the board. To run the links on the board at the standard frequency of 10 Mbits/s, all the coding switches should be set to ON.

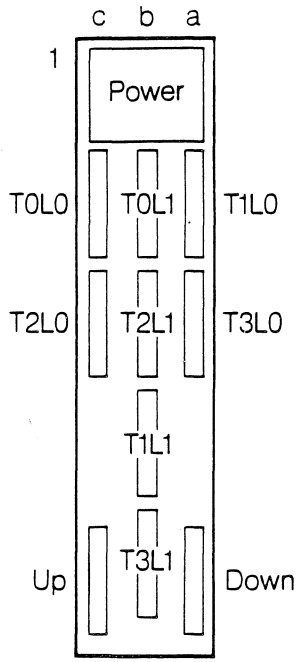
The simplest way to select other link speed selections is shown below.



The allocation of the individual switches is as follows:

Switch	Signal (which is true when switch is OFF)
6	Link0Special
5	Link123Special
3	SpecialSpeed

1.6 Connecting The B003 to another evaluation board



The B003 uses an edge connector pinout compatible with other INMOS transputer evaluation boards. The pinout is described in detail later in the user manual, but the figure in the margin shows what you need to know to connect to another board. The pins are grouped in sets of five, suitable for the five way sockets which terminate the various cables which plug into the edge connector. Each five way socket is coded to make it difficult to connect it to the wrong pins.

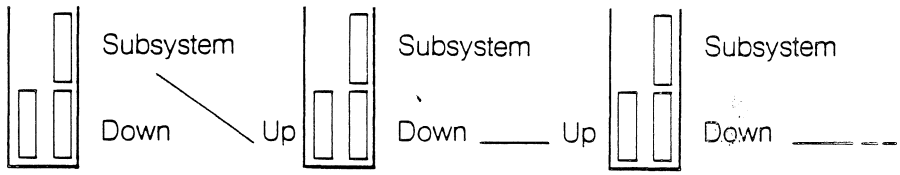
The power supply and link sockets are self explanatory. The banana plugs allow several boards to use the same power supply, which should be capable of providing the total current required.

The Up and Down sockets are concerned with system control - initialization and error handling. The simplest way to use them is to connect the Subsystem socket of the board connected to the TDS to the Up socket of the next board, and then daisy chain Down of one board to Up of the next board. This connection means that when you reset the board connected to the TDS, all the other boards are reset at the same time.

(If connecting to a B002 or B004, you may find it easier to use the Down socket instead of the Subsystem socket)

The link connections to the B003 depend on the program you want to run.

The arrangement of the link sockets is designed to simplify interconnections between boards. In particular, if jumpers are put between the links on the 'b' column of the connector, the B003 is turned into a recursive transputer (tetrahedron configuration) with its four external links appearing as if they were the links of a single transputer.



Board connected to TDS

1.7 Testing the board

Connect Link1 from a B001, B002, or B004, to T0L0 of the B003, as well as the Up socket of the B003 to the Down or Subsystem socket of the other evaluation board.

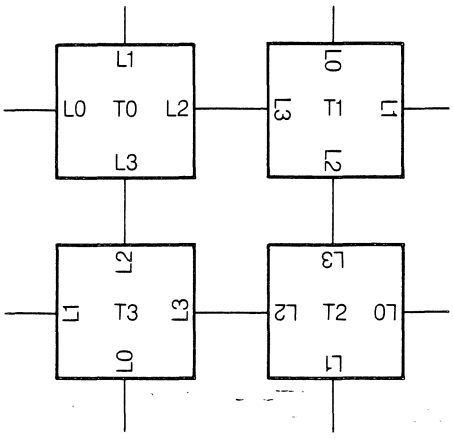
A test program for the B003 (or for any similar configuration of four transputers) is given in releases of the TDS made after first shipments of the B003. You will need to compile program this with the terminal driver for the board which is connected between the TDS and the B003.

The program runs a memory test on the four transputers, and in doing so checks the links between the transputers on the board. The program can also test the other links which are brought out to the edge connector.

In the absence of the test program from your release of the TDS, use the multiboard echo test supplied to establish confidence that the B003 is working. Alternatively write a small RAMtest program to write something different to each location and then check that the data is remembered.

The B003 is compatible with the evaluation board architecture of the B001, B002 and B004. The edge connector pinout is a simple superset of the connectors used on these boards.

2.1 Links



The transputers on the board are connected in a square, as shown in the margin. The square has rotational symmetry, with link 2 of each transputer connected to link 3 of the next transputer.

Links 0 and 1 of each transputer are taken to the edge connector. Although the links on the B003 are not buffered as on the other evaluation boards, the links are totally compatible between boards.

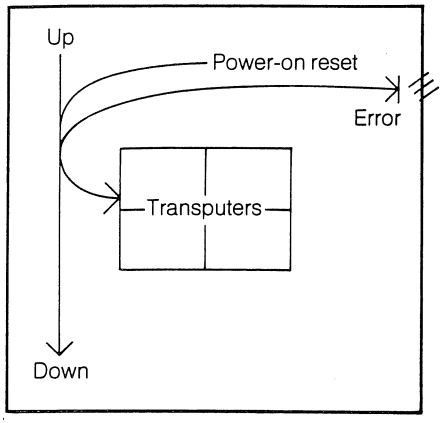
The LinkIn signals have static diode protection and pull down resistors. Protection of the link signals is designed to ensure that the board can withstand 2kV electrostatic discharges to its edge connector pins. The pulldowns ensure that links which are not connected do not see spurious data.

The LinkOut signals are not buffered but have a series resistor which, together with the output impedence of the transputer, matches a 100 ohm transmission line.

The coding switches for the link speed selection make it possible to have the internal links on the board running at 20 Mbits/s, while Link 0s are connected off the board and running at 10 Mbits/s. Alternatively, all the links may be set to run at 10 Mbits/s or 20 Mbits/s.

If running extarnal links at 20 Mbits/s, ensure that the link connections are short.

2.2 System control through the Up and Down sockets



The Up and Down sockets are connected as shown in the margin.

The Reset and Analyse signals flow in the direction of the arrows shown: asserting UpReset resets this board and any board(s) connected to the Down socket.

The Error signal flows in the reverse direction from Down to Up, and indicates that an error has occured on this board or on a board further down from this board.

All the B003's transputers are reset on power ON.

A single Error LED (yellow) lights if an error has occured on this board or on a board below this one.

The B003 does not have reset or analyse switches.

The detail of the reset, analyse, and error logic is shown in the circuit diagram.

2.3 Edge connector pinout

The boards use a two part edge connector conforming to DIN 41612, the same sort of connector as is used on VME boards and Multibus II boards.

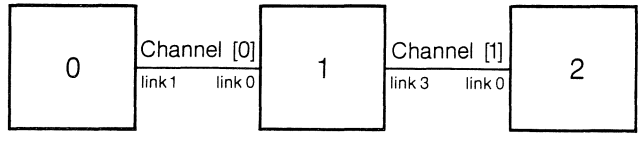
IMS B003 boards use the 96 way version of this connector, with the pinout shown.

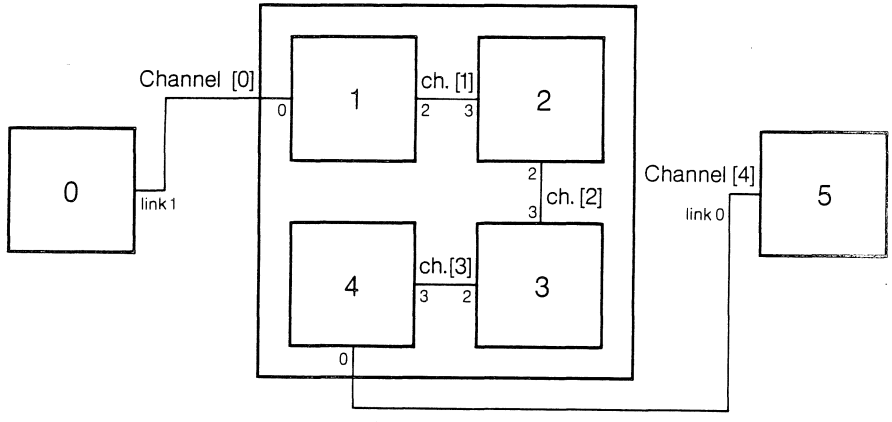
The GND pins c31,32 on the board are convenient for scope earth leads.

Pin	c	b	a
1	GND	GND(cut short)	GND
2	VCC	VCC(cut short)	VCC
3	(cut short)	(cut short)	(cut short)
4	VCC	VCC(cut short)	VCC
5	GND	GND(cut short)	GND
6	VCC(sleeved)	VCC(sleeved)	VCC(sleeved)
7	GND	GND	GND
8	(cut short)	(cut short)	(cut short)
9	LinkOutT0L0	LinkOutT0L1	LinkOutT1L0
10	LinkInT0L0	LinkInT0L1	LinkInT1L0
11	GND	GND	GND
12	nc	nc	nc
13	GND	GND	GND
14	(cut short)	(cut short)	(cut short)
15	LinkOutT2L0	LinkOutT2L1	LinkOutT3L0
16	LinkInT2L0	LinkInT2L1	LinkInT3L0
17	GND	GND	GND
18	VCC(sleeved)	VCC	VCC(sleeved)
19	nc	nc	nc
20	nc	(sleeved)	nc
21	nc	GND	VCC(sleeved)
22	nc	(cut short)	nc
23	nc	LinkOutT1L1	nc
24	nc	LinkInT1L1	nc
25	nc	GND	GND(cut short)
26	nc	nc	(cut short)
27	VCC(sleeved)	GND	VCC(sleeved)
28	UpNotReset	(cut short)	DownNotReset
29	UpNotAnalyse	LinkOutT3L1	DownNotAnalyse
30	UpNotError	LinkInT3L1	DownNotError
31	GND	GND	GND(cut short)
32	GND(cut short)	VCC(sleeved)	GND(cut short)

A B003 board may be used in place of (or in addition to) an existing B001 or B002 board to provide an increase in processing power. For example, a simple pipeline of three nodes can be expanded to a pipeline of six nodes by replacing the middle transputer (housed on a B002) with four transputers (housed on a B003). Example programs for these configurations are shown on the following pages. For further configuration examples, consult the B003 user application note.

Note from the diagrams below that there is no change in the wiring between boards; the only change required is to the board and the program.





```
{{{ 3-node pipeline configured for B002s
{{{ define link/channel numbers - T4
VAL  link0in  IS 4 :
VAL  link0out IS 0 :
VAL  link1in  IS 5 :
VAL  link1out IS 1 :
VAL  link2in  IS 6 :
VAL  link2out IS 2 :
VAL  link3in  IS 7 :
VAL  link3out IS 3 :
}}}
{{{ COMMENT create internal mapping arrays
}}}
{{{ declare size of structure
VAL  n     IS 3:
VAL  nodes IS n:
}}}
{{{ declare sizes of channel array
[nodes-1] CHAN channel:
}}}

{{{ SC first.node
{{{
PROC first.node (CHAN channel.out)
  SKIP
:
}}}
}}}
{{{ SC node
{{{
PROC node (CHAN channel.in,
                channel.out)
  SKIP
:
}}}
}}}
{{{ SC nth.node
{{{
```

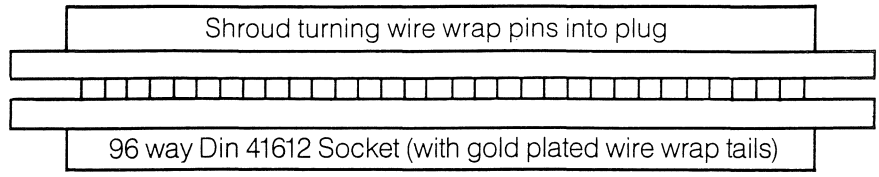
```
PROC nth.node (CHAN channel.in)
  SKIP
:
}}}
}}}

{{{ pipe.line of n processes
PLACED PAR
  PROCESSOR 0 T4
    PLACE channel[0] AT link1out:
    first.node (channel[0])
  PLACED PAR machine = 1 FOR (nodes-2)
    PROCESSOR machine T4
      {{{ place channels
      PLACE channel  [machine-1]  AT  link0in:
      PLACE channel  [machine]    AT  link3out:
      }}}
      node  (channel [machine-1], channel [machine])
  PROCESSOR (nodes-1) T4
    PLACE channel[nodes-2] AT link0in:
    nth.node (channel[nodes-2])
}}}
}}}


{{{ wiring diagram
Connectivity Diagram
--------------------

occam 2, beta.1, 18-Apr-86

CONNECT processor 0 link 1 to processor 1 link 0
CONNECT processor 1 link 3 to processor 2 link 0
}}}
```

```
{{{ 6-node pipeline configured for a B003 application
{{{ define link/channel numbers - T4
VAL  link0in  IS 4 :
VAL  link0out IS 0 :
VAL  link1in  IS 5 :
VAL  link1out IS 1 :
VAL  link2in  IS 6 :
VAL  link2out IS 2 :
VAL  link3in  IS 7 :
VAL  link3out IS 3 :
}}}
{{{ create internal mapping arrays
VAL link.in       IS  [link0in,  link3in,  link3in,  link3in]:
VAL link.out      IS  [link2out, link2out, link2out, link0out]:

-- each soft channel is associated with a table
-- which is indexed when the soft channel is
-- placed on to a hard channel.
}}}
{{{ declare size of structure
VAL  n     IS 6:
VAL  nodes IS n:
}}}
{{{ declare sizes of channel array
[nodes-1] CHAN channel:
}}}

{{{ SC first node
{{{
PROC first.node (CHAN channel.out)
  SKIP
:
}}}
}}}
{{{ SC node
{{{
```

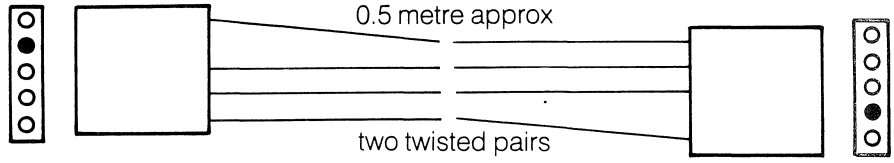
```
PROC node (CHAN channel.in,
                channel.out)
  SKIP
:
}}}
}}}
{{{ SC nth.node
{{{
PROC nth.node (CHAN channel.in)
  SKIP
:
}}}
}}}

{{{ pipe.line of n processes
PLACED PAR
  PROCESSOR 0 T4
    PLACE channel[0] AT link1out:
    first.node (channel[0])
  PLACED PAR machine = 1 FOR (nodes-2)
    PROCESSOR machine T4
      {{{ evaluate map.index
      VAL  map.index   IS  machine-1:
                                                    -- position of node within
                                                    -- B003 group (0..3)
      }}}
      {{{ place channels
      PLACE channel  [machine-1]  AT  link.in  [map.index]:
      PLACE channel  [machine]    AT  link.out [map.index]:
      }}}
      node  (channel [machine-1], channel [machine])
  PROCESSOR (nodes-1) T4
    PLACE channel[nodes-2] AT link0in:
    nth.node (channel[nodes-2])
}}}
}}}
```

```
{{{ wiring diagram
Connectivity Diagram
--------------------

occam 2, beta.1, 18-Apr-86

CONNECT processor 0 link 1 to processor 1 link 0
CONNECT processor 1 link 2 to processor 2 link 3
CONNECT processor 2 link 2 to processor 3 link 3
CONNECT processor 3 link 2 to processor 4 link 3
CONNECT processor 4 link 0 to processor 5 link 0
}}}
```

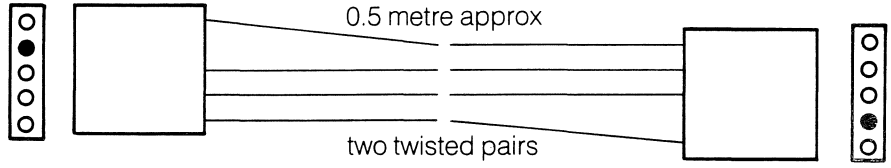
Edge connector



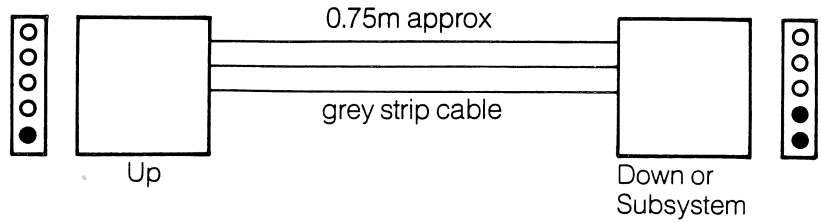
Standard Link cables (4 off per board)



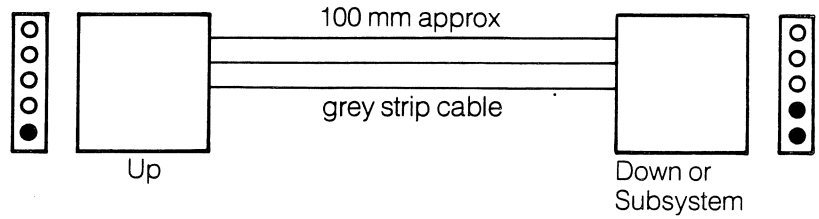
Short Link cables (4 off per board)



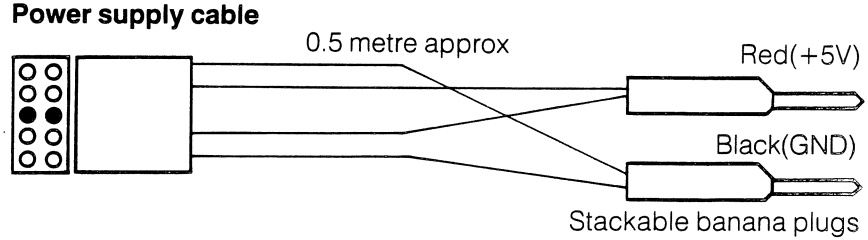
Long reset cable

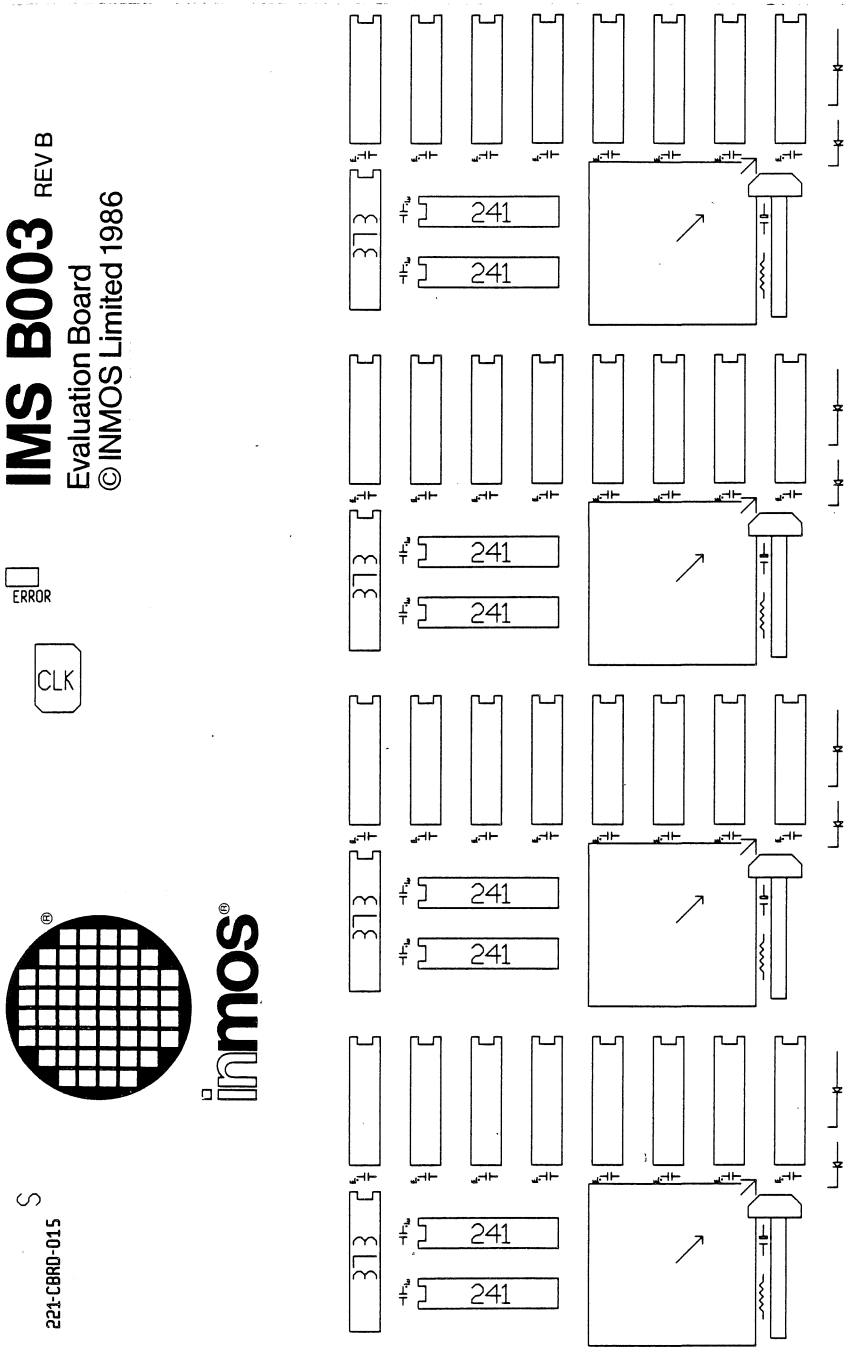


Short reset cable

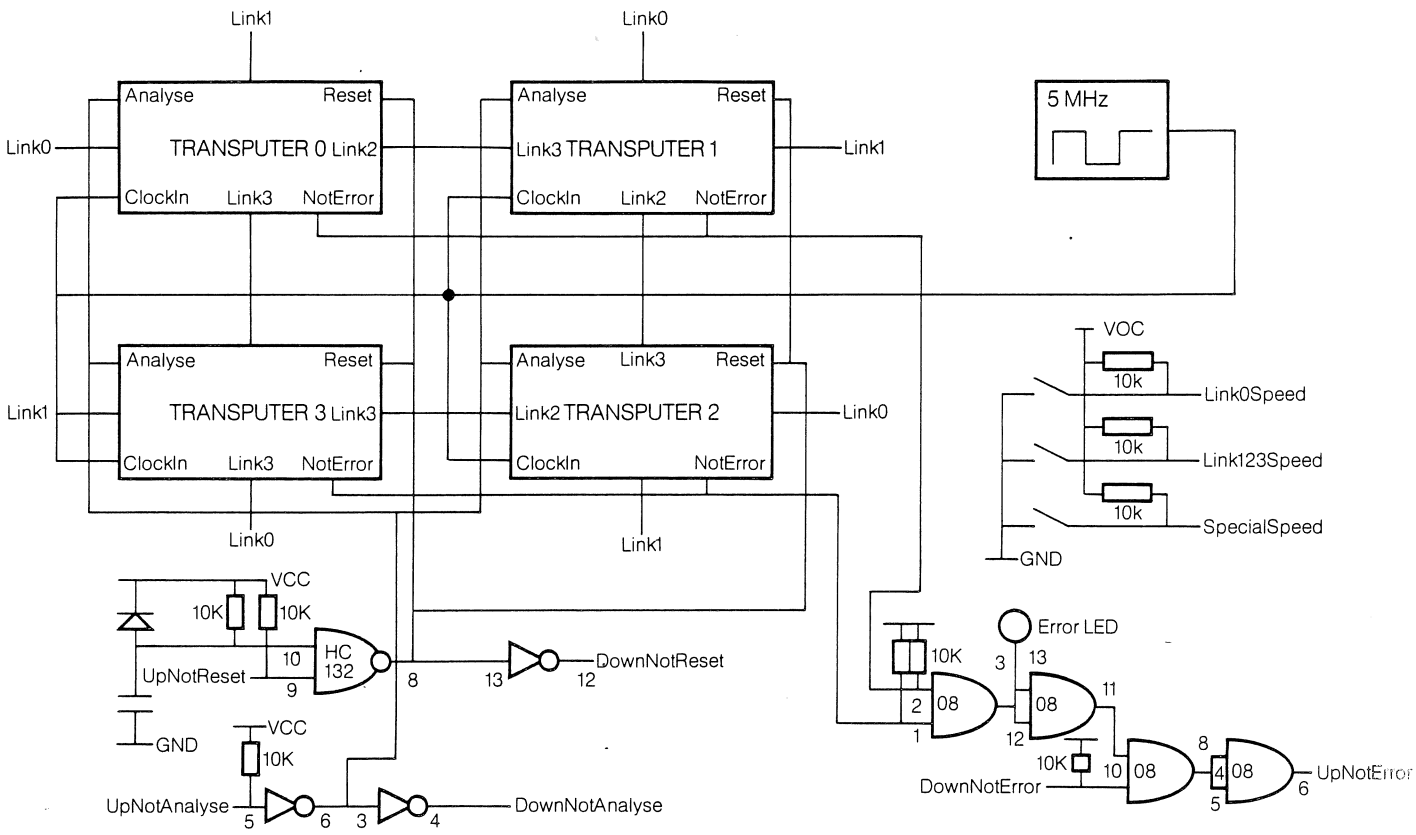


Power supply cable

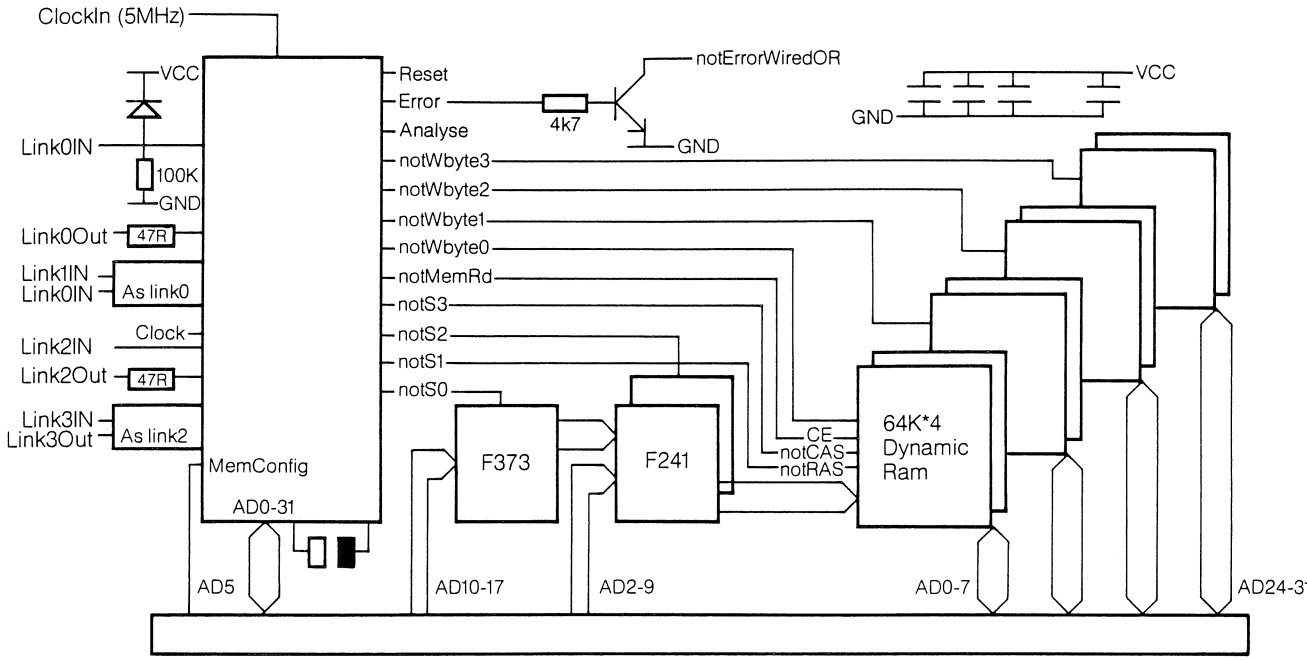



IMS B003 REV B
Evaluation Board
© INMOS Limited 1986
ERROR
CLK
inmos
221-CBRD-015
373
241
LOW
THIS WAY UP
SPECIAL
L123SPECIAL
L05SPECIAL
74HC32
08
04

This diagram shows the logic shared by all four transputers:



This diagram shows the logic that is replicated four times. The pin numbers of the ICs are shown in tables on the following pages.



The signals on each pin of the RAMs and TTL for each transputer are most easily given as a table:

Pin	All RAMs	RAM1	RAM2	RAM3	RAM4	RAM5	RAM6	RAM7	RAM8
1	notMemRd(OE)								
2		AD13	AD10	AD6	AD4	AD17	AD19	AD25	AD27
3		AD14	AD12	AD7	AD5	AD16	AD20	AD29	AD31
4		WB3	WB3	WB2	WB2	WB0	WB0	WB1	WB1
5	notMemS1(RAS)								
6	MuxA0								
7	MuxA1								
8	MuxA2								
9	VCC								
10	MuxA3								
11	MuxA4								
12	MuxA5								
13	MuxA6								
14	MuxA7								
15		AD8	AD15	AD3	AD0	AD21	AD23	AD28	AD26
16	notMemS3(CAS)								
17	AD9	AD11	AD2	AD1	AD18	AD22	AD24	AD30	
18	GND								

Pin	F241 (lo)	F241 (hi)	F373
1	notMemS2	notMemS2	GND
2	LA11	LA10	LA16
3	MuxA0	MuxA1	AD16
4	LA13	LA17	AD10
5	MuxA2	MuxA3	LA10
6	LA12	LA16	LA12
7	MuxA6	MuxA5	AD12
8	LA14	LA15	AD11
9	MuxA7	MuxA4	LA11
10	GND	GND	GND
11	AD5	AD4	notMemS0
12	MuxA7	MuxA4	LA13
13	AD9	AD8	AD13
14	MUXA7	MUXA5	AD14
15	AD2	AD3	LA14
16	MUXA2	MUXA3	LA17
17	AD7	AD6	AD17
18	MuxA0	MuxA1	AD15
19	notMemS2	notMemS2	LA15
20	VCC	VCC	VCC

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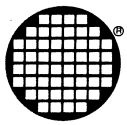

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