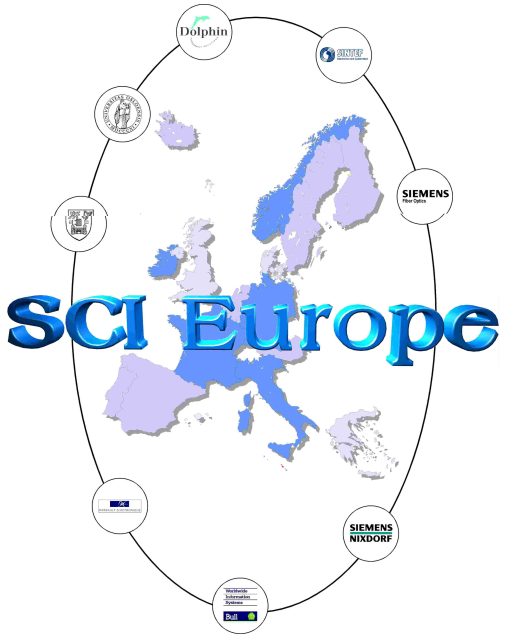
SCI Europe number: P25257
Deliverable number: D2.2.1b
Contractual date: 30th April, 1999
Work package: 2.2.1

Document version: 1.0
Document status: Complete
Confidentiality: Consortium
Document date: April, 1999

Deliverable



Prototype Trace Probe and Probe Adapter

Partner: Trinity College Dublin
Author(s): B.A.Coghlan, M.Manzke
Editor: B.A.Coghlan

Keywords: SCI, trace, probe, analysis

Abstract:

In this document we present the technical manual for the prototype trace probe and probe adapter developed within the project.

esprit project 25257

Contents

ESPRIT Project P25257 SCIEurope

Deliverable D 2.2.1b

Prototype Trace Probe and Probe Adapter

April 1999

Dr.B.A.Coghlan
Department of Computer Science
Trinity College Dublin
coghlan@cs.tcd.ie

M.Manzke
Department of Computer Science
Trinity College Dublin
michael.manzke@cs.tcd.ie

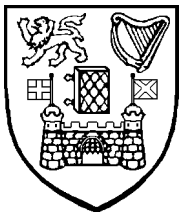
Introduction

The definition of Task 2.2.1 is as follows :

Task	**2.2.1**	**Test Tools Development**		
Market and User Need	There are no commercially available SCI test tools on the market for the SCI community today.			
Objectives	To develop the first generation of tracing and debugging tools for use in work package 3 Applications.			
Approach	The tools will be based on needs identified in the Test Requirements Specification from Task 2.1. There will probably be developed two tools – one tool able to trace the SCI traffic and either show online or store the results. This tool will be based as much as possible on present hardware and software platforms. The other tool will be able to send and receive SCI traffic according to some traffic profile in order to load systems with traffic without using real nodes. The prototype tools will be evaluated during the debugging phase of the Embedded Avionics System demonstrator in Task 3.3, and the results will be summarised in a report.			
Lead Partner	Trinity	24 person months		
Other Partners	D.E. SINTEF	4 person months 12 person months		
Major deliverables	D 2.2.1 D 2.2.2 D 2.2.3	Q4 Q6 Q8	Trinity SINTEF Trinity	Prototype Tracer/Analyzer Traffic Generation Tool Tracer/Analyzer Mk.II

B-Link traces can be acquired via a probe card supplied by Dolphin, that attaches to their SCI cards via elastomeric connectors, and breaks out the B-Link signals to a number of connectors that will accept cables for a HP16500 series logic analyser. Trinity have designed a trace probe and probe adapter that will attach to these to distribute the B-Link signals to a multiple of the DT200.1 Deep Trace boards previously described in Deliverable D2.2.1a

The objective of this document is to present the Technical Manual for the Prototype Trace Probe and Probe Adapter. These represent the SCI-specific hardware resources of the Prototype Tracer/Analyzer.



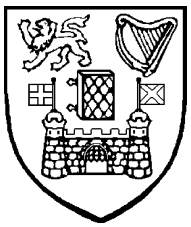
Computer Architecture Group
Department of Computer Science
Trinity College Dublin
Ireland

Tel : +353-1-6081765
Fax : +353-1-6772204

Trace Probe DT204.1

Technical Manual

B.A.Coghlan
M.Manzke



Trace Probe DT204.1

Technical Manual

Introduction

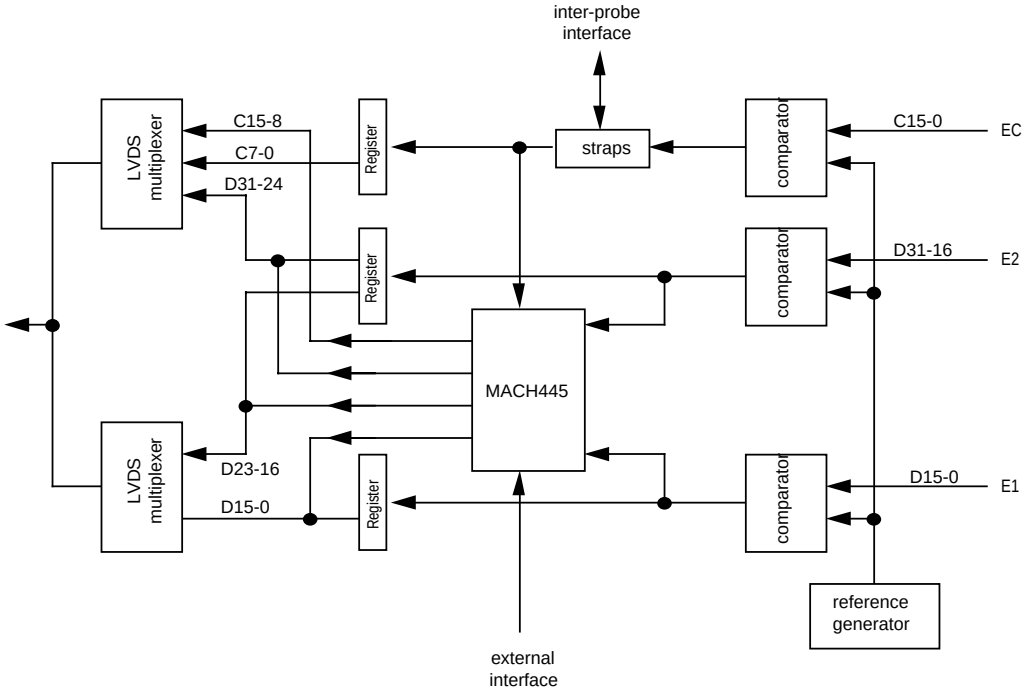
The DT204.1 Trace Probe is designed for interfacing IEEE 1596 Scalable Coherent Interconnect (SCI) systems to the DT200.1 Deep Tracer, which is a modular data collection system designed specifically for gathering very long state traces for performance analysis of SCI systems. Two trace probes are needed, each to attach via a DT205.1 Probe Adapter to one of the two deep trace boards.

Features

- 96bit tracing
  Max Sample Rate 66MHz.
- Tracing Dolphin's D310 B-Link
  Attaches to Dolphin Probe Card.
- Tracing SCI cable via SCILab's SCITrac tracer
  Attaches to SCILab tracer, replacing a logic analyzer.
- Co-ordinated trace of host activity
  16bit header for attaching host tracer.
- Simple deep tracer interface
  34-wire LVDS cable.
- Programmable logic via JTAG
  May be used for test pattern generation or data pattern matching.

Trace Probe Functional Overview

A simplified schematic of the trace probe is shown below.



Each trace probe attaches to 48bits of a 96bit sample data path. All data signals are parallel terminated by 390 ohms to a reference voltage that is generated by voltage regulator VREG2. One of three reference voltages may be selected via strap J22 as follows :

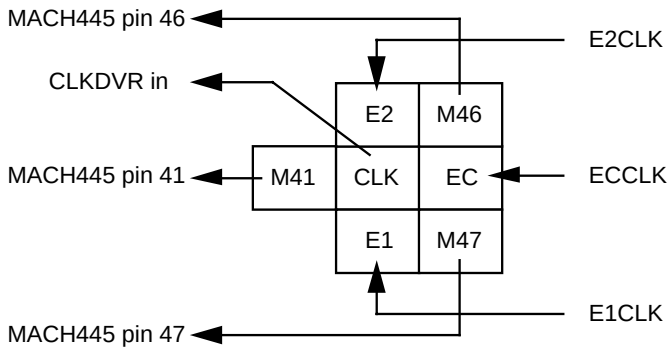
Voltage	J22 Strap
140mV	none
220mV	B-A
TBD	B-C

Six DS92L90A 9bit LVDS tranceivers are configured to compare the sample data to the selected reference voltage. The comparator outputs are low-voltage TTL. Care is taken to minimize any data skews.

Two trace probes are synchronized via an inter-probe cable that connects to IPCON. Its pinout is as follows:

IPCLK	GND
GND	GND
IP0	GND
IP1	GND
IP2	GND
IP3	GND
IP4	GND
IP5	GND
IP6	GND
IP7	TXSYN

The sample clock may be derived from four different sources : input connectors E1, E2 or EC, or the inter-probe connector IPCON. Three of the the clock sources are selected via J21:



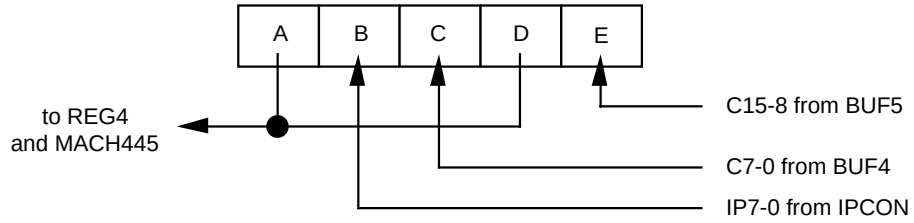
Strapblock J21

Clock Source	J21 Straps
E1CLK	E1-CLK
E2CLK	E2-CLK
ECCLK	EC-CLK

The unselected clocks may be utilized if specifically desired by strapping them to the MACH445 inputs and programming the MACH445 accordingly. A CDC340 clock driver, CLKDVR, buffers the selected clock to independently drive a number of destinations, including J11, which determines the function of the IPCLK signal at the inter-probe connector IPCON. J11 may be set up to output the selected clock to the other trace probe, or to input a clock from the other trace probe. Care is taken to minimize any clock skews.

IPCLK	J11 Strap
IPCLK as input to CLKDVR	B-A
IPCLK as output from CLKDVR	B-C

The data and control fields are treated differently. The data signals from E1 & E2 are pipelined via 74646 registers REG0-3, as well as being fed to a MACH445 pal. The control signals from EC are connected to the J3-10 straps, from which they may be strapped to a further 74646 register REG4 as well as the MACH445 pal, or to the inter-probe connector IPCON as signals IP7-0, see below. Those control signals strapped to the inter-probe connector are pipelined by the matching register REG4 on the other trace probe, which must also derive its clock from the inter-probe connector using the strapping given above.



Strapblock J3-10

Control Signals	Register Strap	Inter-probe Strap
C7-0 to register C15-8 to IP7-0	J3-10 C-D	J3-10 B-E
C15-8 to register C7-0 to IP7-0	J3-10 D-E	J3-10 B-C
C7-0 to register	J3-10 C-D	-
C15-8 to register	J3-10 D-E	-
IP7-0 to register	-	J3-10 A-B

The 74646 registers' direction control input DIR, which is also connected to the DE input of the DS92L90, is resistively pulled down to ground, while their output enable input /G, which is connected to the /RE input of the DS92L90, is resistively pulled up to +3.3V (their SAB and SBA inputs are also resistively pulled up to +3.3V); these connections allow the possibility of using the trace probe to generate synthetic trace data. Both of the above signals connect to and can be driven by the MACH445.

The MACH445 pal also pipelines an 8bit portion of a 16bit external data input from EXTCON that can be connected to any external source, but is intended for connection to a host tracer, such as a VMetro PCI analyzer. Its pinout is :

Top	Bottom
GND	extCLK
GND	ExtD0
GND	ExtD1
GND	ExtD2
GND	ExtD3
GND	ExtD4
GND	ExtD5
GND	ExtD6
GND	ExtD7
GND	ExtD8
GND	ExtD9
GND	ExtD10
GND	ExtD11
GND	ExtD12
GND	ExtD13
GND	ExtD14
GND	ExtD15
GND	GND
GND	GND
GND	GND

Each trace probe is strapped to trace an appropriate 8bit field of the external data as follows :

External Data	Strap
extD7-0	J12-19 B-C
extD15-8	J12-19 B-A

These signals are parallel terminated with 220 ohms to +5V and 330 ohms to ground. The external clock is separately terminated, with 22 ohms in series followed by 220 ohms to +5V and 330 ohms to ground.

The MACH445 pal can also be used as a test pattern generator, deriving its clock from a local crystal oscillator OSC (typically 100MHz), which is buffered by a CDC340 clock driver OSCDVR. It may be programmed via a JTAG interface using the MACHXL software.

The MACH445 pal can further be employed to match specific input data patterns, again programmed via the JTAG interface using the MACHXL software. The match results can be pipelined to the tracer via the control fields. This would also be useful if the host tracer required data input rather than generating output, since pattern matching could be utilized to indicate SCI events to the host tracer by programming the MACH445 to generate event identifiers on the external interface.

Two JTAG connectors are provided. The upstream of the JTAG chain connects to JTAGIN, and the downstream connects to JTAGOUT. Their pin connections are :

/ENABLE	/TRST
GND	TDO
TVCC	TDI
GND	TMS
ZCTL	TCK

In the event that there is no downstream chain, TDI should be strapped to TDO at connector JTAGOUT. Note that signals /TRST, /ENABLE and TVCC are resistively pulled up to +5V, while signal ZCTL is resistively pulled down to ground.

The MACH445 may be programmed in-circuit, but since it does not program reliably in-circuit if any of its I/O pins are toggling, any signals that drive the MACH445 are disabled with the JTAG /ENABLE signal, and thus the trace probe is unusable while programming.

The pipelined outputs are converted to multiplexed LVDS using two DS90C283 devices, TX1 for the low 24bits, and TX0 for the high 24bits. These devices multiplex a 28bit TTL data path onto a LVDS cable. Since the data from different devices may be skewed (relative to each other) at the end of the LVDS cables, a synchronizing pulse TXSYN is sent over the 25th bit (and over the inter-probe connector as IPSYN); this repeats every 3 clock cycles. The synchronizing pulse is selected as follows :

TXSYN	**J2 Strap**
MACH445 generates IPSYN	B-C
IPSYN is an input	-

A 34-way flat cable (typically a floppy-disk cable), carrying eight differental signals plus two differential clocks, connects the LVDS ouputs at LVDSCON to the probe adapter at the deep trace board. The pinout is :

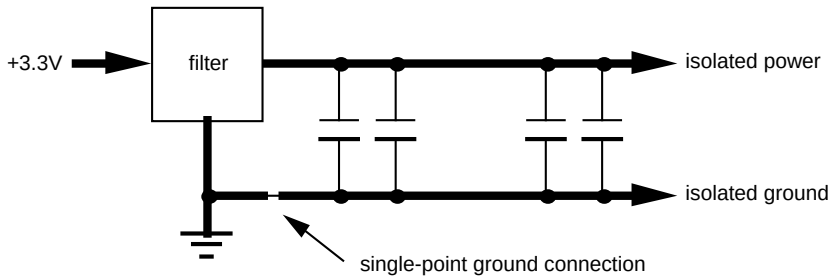
Left	**Right**
Tx1CLKP	Tx1CLKM
AGND	AGND
Tx1OUT2P	Tx1OUT2M
AGND	Tx1OUT3P
Tx1OUT3M	AGND
Tx1OUT1P	Tx1OUT1M
AGND	AGND
Tx1OUT0P	Tx1OUT0M
N.C.	N.C.
Tx0CLKP	Tx0CLKM
AGND	AGND

Tx0OUT2P	Tx0OUT2M
AGND	Tx0OUT3P
Tx0OUT3M	AGND
TX0OUT1P	Tx0OUT1M
AGND	AGND
Tx0OUT0P	Tx0OUT0M

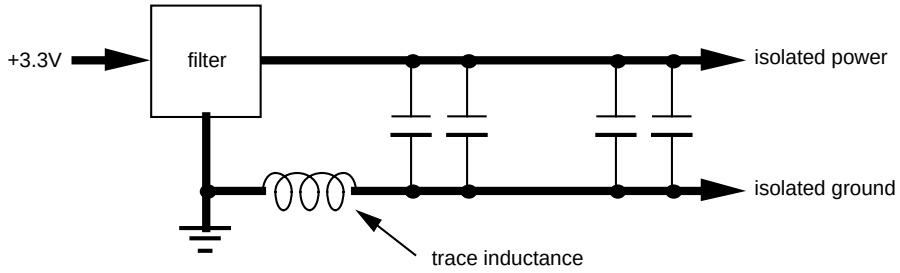
The pipelined outputs are also connected to two 40-way flat cable connectors, NSCON0 for the low 24bits, and NSCON1 for the high 24bits These are intended both for debugging and for connection to the National Semiconductor LVDS demo hardware, and would not normally be used. Their pinout is :

signal	pin no.	pin no.	signal
VCC	1	2	SAFE12V
VEESAFE	3	4	VEEADJ
EBABLK	5	6	GND
M	7	8	DE
GND	9	10	LP(HSYNC)
FLM(VSTNC)	11	12	GND
SHFCLK	13	14	GND
P0	15	16	P1
GND	17	18	P2
P3	19	20	GND
P4	21	22	P5
GND	23	24	P6
P7	25	26	GND
P8	27	28	P9
GND	29	30	P10
P11	31	32	GND
P12	33	34	P13
GND	35	36	P14
P15	37	38	GND
P16	39	40	P17
GND	41	42	P18
P19	43	44	GND
P20	45	46	P21
GND	47	48	P22
P23	49	50	GND

5V power is normally obtained from PWRCON0, or alternatively from PWRCON1. An LED, PWRLED, indicates when power is present. A 3.3V voltage regulator, VREG1, then generates 3.3V for those devices that need it. There are four internal PCB power planes : +5V, +3.3V, digital ground and analog ground. A substantial reference voltage area approximates a fifth internal power plane. The DS92L90 devices have isolated power and grounds for their LVDS interfaces; power is isolated via filters while ground is isolated via an approximation to single-point connection of the analog ground plane.



The DS9C283 devices also have isolated power and grounds for both the LVDS interfaces and their phase-lock loops; power is isolated via filters while ground is isolated via trace inductances.



Either a 3.3V or a 5V MACH445 pal can be used, but the appropriate supply voltage must be selected via J20 :

Voltage	J20 Strap
3.3V	B-A
5V	B-C

Strap J1 can be shorted to power down the DS90C283 devices.

Trace Example 1: Trace from Dolphin's D310 B-Link

A Dolphin probe card must first be attached to the D310. Two DT204.1 trace probes can be attached to the Dolphin probe card as follows :

1. Trace probe 0 : E1 connects to probe card E1
   E2 connects to probe card E2
   EC connects to probe card E5
2. Trace probe 1 : E1 connects to probe card E3
   E2 connects to probe card E4
   EC connects to probe card E6

3. An inter-probe cable must interconnect IPCON of trace probes 0 & 1.

4. The upstream JTAG daisy chain should be connected to JTAGIN of trace probe 0. A JTAG cable should interconnect JTAGOUT of trace probe 0 to JTAGIN of trace probe 1. The downstream chain should be connected to JTAGOUT of trace probe 1, but in the event of there being no downstream chain, its TDI should be strapped to its TDO.

5. Trace probes 0 & 1 must be connected via a DT205.1 probe adapter to deep trace board 0 & 1, respectively.

6. A synchronizing cable must interconnect J6 of probe adapters 0 & 1, respectively.

7. A trigger/trace cable must interconnect EXTCON of deep trace boards 0 & 1, respectively.

Then the straps must be selected as follows.

8. For both trace probes, the reference voltage must be selected via strap J22:

Voltage	J22 Strap
140mV	none

9. For trace probe 0, E1 must be selected as the clock source, and the IPCLK signal must be set up to output the selected clock to the other trace probe :

Clock Source	J21 Straps
E1	E1-OUT

IPCLK	J11 Strap
IPCLK as output from CLKDVR	B-C

10. For trace probe 1, the clock source must come from IPCLK rather than E1, and the IPCLK signal must be set up to input the selected clock from the other trace probe :

Clock Source	J21 Straps
IPCLK	-

IPCLK	J11 Strap
IPCLK as input to CLKDVR	B-A

11. For trace probe 0, the C7-0 must be strapped to register REG4, and C15-8 must be strapped to the inter-probe connector :

Control Signals	Register Strap	Inter-probe Strap
C7-0 to register C15-8 to IP7-0	J3-10 C-D	J3-10 B-E

12. For trace probe 1, the IP7-0 must be strapped to the register :

Control Signals	Register Strap	Inter-probe Strap
IP7-0 to register	-	J3-10 A-B

13. Each trace probe is strapped to trace an appropriate 8bit field of the external data as follows :

External Data	Strap
extD7-0	J12-19 B-C
extD15-8	J12-19 B-A

14. For trace probe 0, TXSYN must be output to the inter-probe connector:

TXSYN	J2 Strap
MACH445 generates IPSYN	B-C

15. For trace probe 1, IPSYN must be treated as an input :

TXSYN	J2 Strap
IPSYN is an input	-

The aggregated sample data fields are then as follows :

Functional Overview

SDxx	DT200 board 0	DT200 board 1	MACH445 I/O no.
SCLOCK	bclk	bclk	i0/clk0
0	d0	d32	8
1	d1	d33	9
2	d2	d34	10
3	d3	d35	11
4	d4	d36	12
5	d5	d37	13
6	d6	d38	14
7	d7	d39	15
8	d8	d40	16
9	d9	d41	17
10	d10	d42	18
11	d11	d43	19
12	d12	d44	20
13	d13	d45	21
14	d14	d46	22
15	d15	d47	23
16	d16	d48	24
17	d17	d49	25
18	d18	d50	26
19	d19	d51	27
20	d20	d52	28
21	d21	d53	29
22	d22	d54	30
23	d23	d55	31
24	d24	d56	32
25	d25	d57	33
26	d26	d58	34
27	d27	d59	35
28	d28	d60	36
29	d29	d61	37
30	d30	d62	38
31	d31	d63	39
32	-	dok	7
33	breq0	uok	6
34	breq1	brstn	5
35	breq2	brst1	4
36	breq3	brst0	3
37	frame	prstn	2
38	here	mclr	1
39	busy	cfgin	0
40	y0	y8	63
41	y1	y9	62
42	y2	y10	61
43	y3	y11	60
44	y4	y12	59
45	y5	y13	58
46	y6	y14	57
47	y7	y15	56

MACH445 I/O no.	DT200 board 0	DT200 board 1
i1/clk1	oscout	oscout
i2		
i3/clk2	extclk	extclk
i4/clk3		
i5		
40	bufre	bufre
41		
42		(userr)
43		(attn)
44		(int0)
45		(obs0)
46		(int1)
47		(obs1)
48	extd0	extd8
49	extd1	extd9
50	extd2	extd10
51	extd3	extd11
52	extd4	extd12
53	extd5	extd13
54	extd6	extd14
55	extd7	extd15

Trace Example 2: Trace from SCI cable via SCILab's SCITrac tracer

A SCITrac tracer must first be attached to the SCI cable. Two DT204.1 trace probes can be attached to the SCILab tracer as follows :

1. Trace probe 0 : E1 connects to pod1
   E2 connects to pod2
   EC connects to pod5
2. Trace probe 1 : E1 connects to pod3
   E2 connects to pod4
   EC not connected

3. An inter-probe cable must interconnect IPCON of trace probes 0 & 1.

4. The upstream JTAG daisy chain should be connected to JTAGIN of trace probe 0. A JTAG cable should interconnect JTAGOUT of trace probe 0 to JTAGIN of trace probe 1. The downstream chain should be connected to JTAGOUT of trace probe 1, but in the event of there being no downstream chain, its TDI should be strapped to its TDO.

5. Trace probes 0 & 1 must be connected via a DT205.1 probe adapter to deep trace board 0 & 1, respectively.

6. A synchronizing cable must interconnect J6 of probe adapters 0 & 1, respectively.

7. A trigger/trace cable must interconnect EXTCON of deep trace boards 0 & 1, respectively.

Then the straps must be selected as follows.

8. For both trace probes, the reference voltage must be selected via strap J22:

Voltage	J22 Strap
220mV	B-A

9. For trace probe 0, E1 must be selected as the clock source, and the IPCLK signal must be set up to output the selected clock to the other trace probe :

Clock Source	J21 Straps
E1	E1-OUT

IPCLK	J11 Strap
IPCLK as output from CLKDVR	B-C

10. For trace probe 1, the clock source must come from IPCLK rather than E1, and the IPCLK signal must be set up to input the selected clock from the other trace probe :

Clock Source	J21 Straps
IPCLK	-

IPCLK	J11 Strap
IPCLK as input to CLKDVR	B-A

11. For trace probe 0, the C7-0 must be strapped to register REG4, and C15-8 must be strapped to the inter-probe connector :

Control Signals	Register Strap	Inter-probe Strap
C7-0 to register C15-8 to IP7-0	J3-10 C-D	J3-10 B-E

12. For trace probe 1, the IP7-0 must be strapped to the register :

Control Signals	Register Strap	Inter-probe Strap
IP7-0 to register	-	J3-10 A-B

13. Each trace probe is strapped to trace an appropriate 8bit field of the external data as follows :

External Data	Strap
extD7-0	J12-19 B-C
extD15-8	J12-19 B-A

14. For trace probe 0, TXSYN must be output to the inter-probe connector:

TXSYN	J2 Strap
MACH445 generates IPSYN	B-C

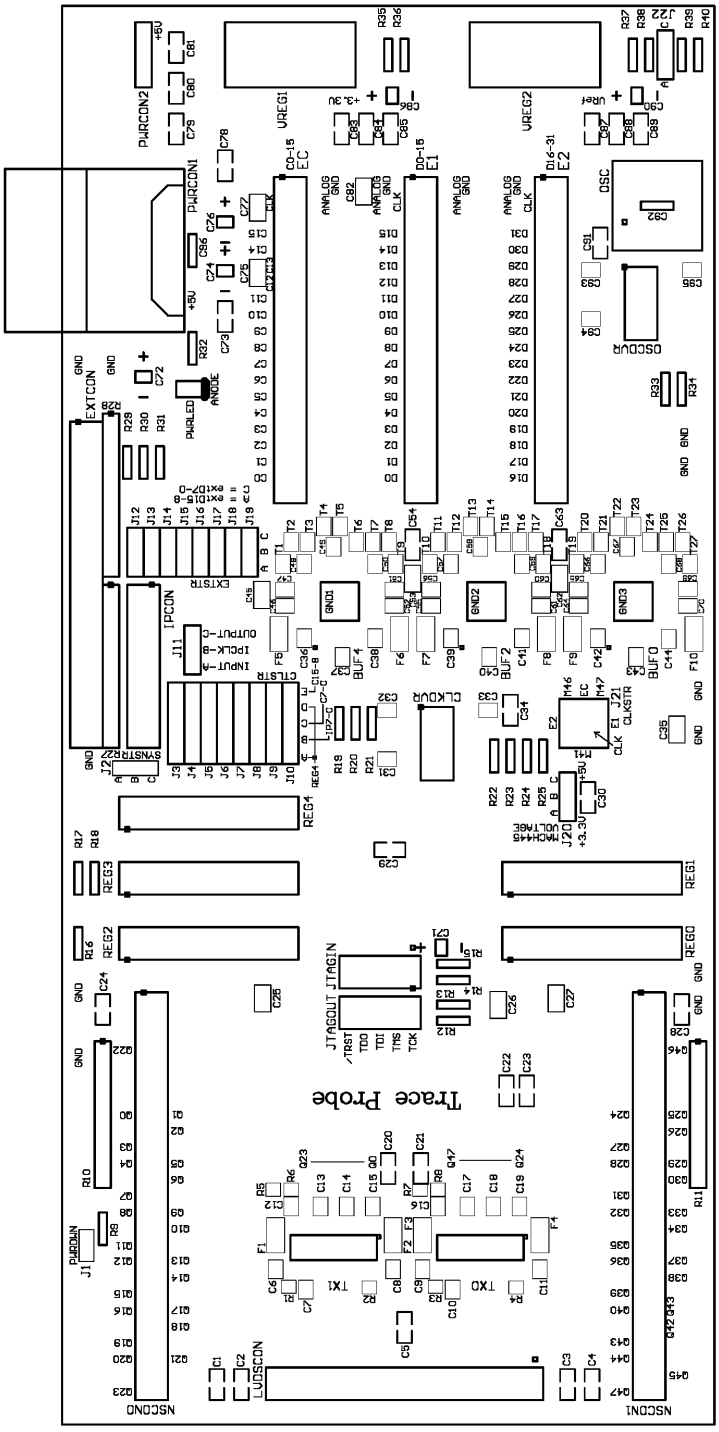
15. For trace probe 1, IPSYN must be treated as an input :

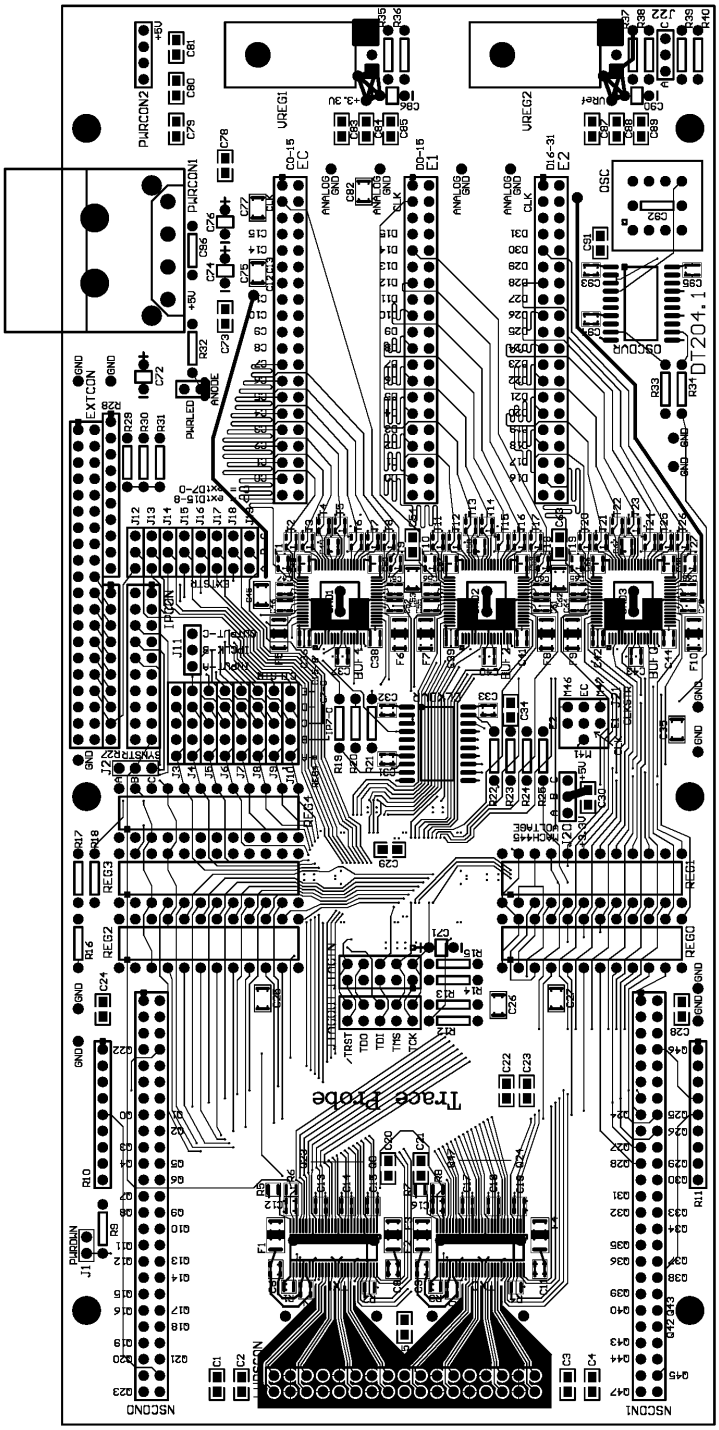
TXSYN	J2 Strap
IPSYN is an input	-

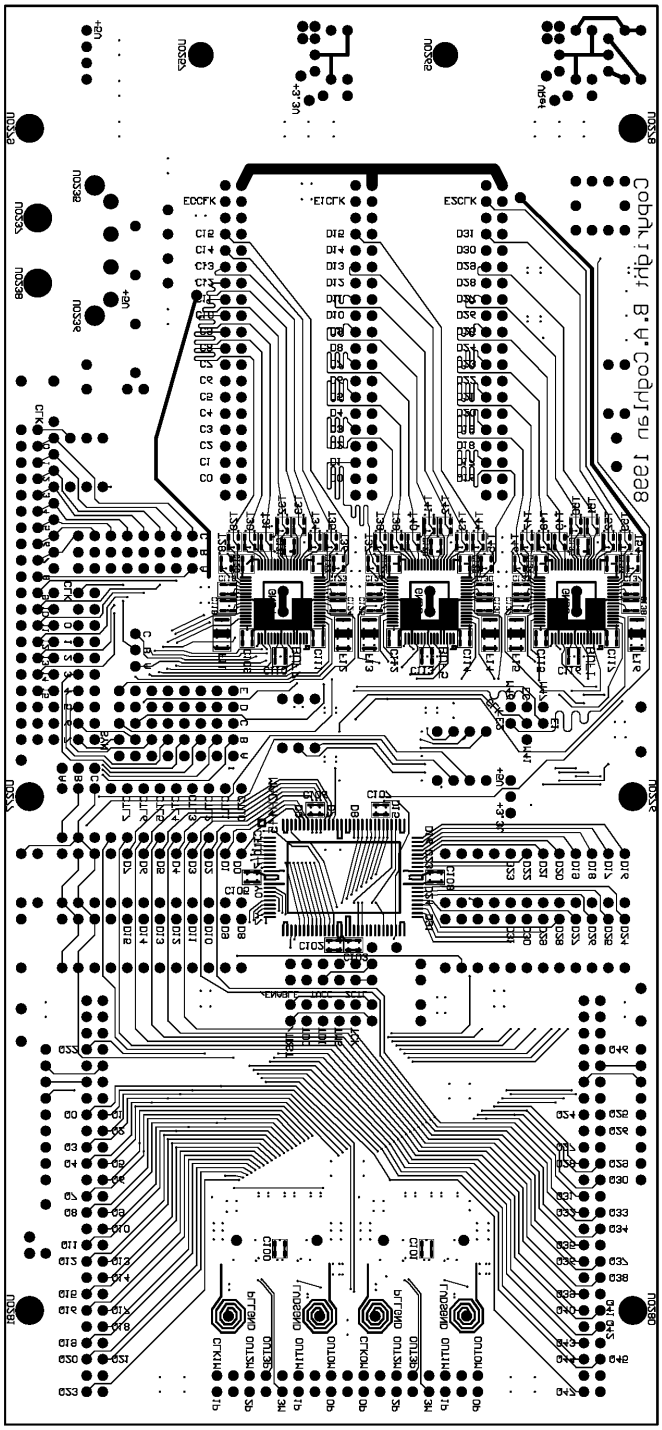
The aggregated sample data fields are then as follows :

SDxx	DT200 board 0	DT200 board 1	MACH445 I/O no.
SCLOCK	bclk	bclk	i0/clk0
0	d0	d32	8
1	d1	d33	9
2	d2	d34	10
3	d3	d35	11
4	d4	d36	12
5	d5	d37	13
6	d6	d38	14
7	d7	d39	15
8	d8	d40	16
9	d9	d41	17
10	d10	d42	18
11	d11	d43	19
12	d12	d44	20
13	d13	d45	21
14	d14	d46	22
15	d15	d47	23
16	d16	d48	24
17	d17	d49	25
18	d18	d50	26
19	d19	d51	27
20	d20	d52	28
21	d21	d53	29
22	d22	d54	30
23	d23	d55	31
24	d24	d56	32
25	d25	d57	33
26	d26	d58	34
27	d27	d59	35
28	d28	d60	36
29	d29	d61	37
30	d30	d62	38
31	d31	d63	39
32	s1[F]	qc0[3]	7
33	s2[F]	qc0[2]	6
34	s3[F]	qc0[1]	5
35	s4[F]	qc0[0]	4
36	qc[3]	N.U.	3
37	qc[2]	sync	2
38	qc[1]	L1[1]	1
39	qc[0]	L1[0]	0
40	y0	y8	63
41	y1	y9	62
42	y2	y10	61
43	y3	y11	60
44	y4	y12	59
45	y5	y13	58
46	y6	y14	57
47	y7	y15	56

MACH445 I/O no.	DT200 board 0	DT200 board 1
i1/clk1	oscout	oscout
i2		
i3/clk2	extclk	extclk
i4/clk3		
i5		
40	bufre	bufre
41		
42		(userr)
43		(attn)
44		(int0)
45		(obs0)
46		(int1)
47		(obs1)
48	extd0	extd8
49	extd1	extd9
50	extd2	extd10
51	extd3	extd11
52	extd4	extd12
53	extd5	extd13
54	extd6	extd14
55	extd7	extd15


Trace Probe
PWRCON2
PWRCON1
VREG1
VREG2
OSC
OSCDUP
EXTCON
PWRLED
ANODE
EXTSTR
IPCON
CTLSTR
SYNSTR
CLKOUT
CLKSTR
BUF1
BUF2
BUF0
GND1
GND2
GND3
REG4
REG3
REG2
REG1
REG0
JTAGOUT
JTAGIN
/TRST
TDO
TDI
TMS
TCK
TXI
TXO
PWRDWN
LVDSCON
NSCONO
NSCONI


DT204.1
Trace Probe
VREG1
VREG2
OSC
EXTCON
PWRLED
PWRDWN
PWRCON1
PWRCON2
NSCON0
NSCON1
REG0
REG1
REG2
REG3



Electrical Characteristics

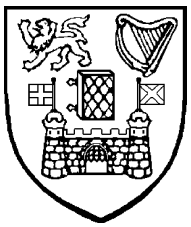
minimum sample data logical 1 input voltage	240 mVolts
maximum sample data logical 1 input voltage	550 mVolts
minimum sample data logical 0 input voltage	-50 mVolts
maximum sample data logical 0 input voltage	80 mVolts
resistive loading per input under test	390 ohms
capacitive loading per input under test	5pF
minimum TTL logical 1 input voltage	2.0 Volts
maximum TTL logical 1 input voltage	5.5 Volts
minimum TTL logical 0 input voltage	-0.5 Volts
maximum TTL logical 0 input voltage	0.8 Volts
minimum E1 clock frequency	0 Hz
maximum E1 clock frequency	66 MHz
minimum E1 clock logical 0 duration	5 nS
minimum E1 clock logical 1 duration	5 nS
D[0..31] setup time relative to E1 clock positive transition	5 nS
D[0..31] hold time relative to E1 clock positive transition	1 nS
C[0..15] setup time relative to E1 clock positive transition	5 nS
C[0..15] hold time relative to E1 clock positive transition	1 nS
extD[0..15] setup time relative to extCLK positive transition	5 nS
extD[0..15] hold time relative to extCLK positive transition	1 nS
supply current	TBD

Parts List

The parts list is :

	Part No	Supplier	Description	Quantity
	DT2041	ECS	PCB	1
BUF0-7	NatSemi DS92L90A	EBV	LVDS tranceiver	8
TX0-1	NatSemi DS90C283	EBV	LVDS multiplexer	2
MACH445	AMD M4LV-128/64-7YC	Lyco	MACH445 GAL	1
CLKDVR OSCDVR	TI CDC340	Farnell 149-230 (NEWK4063)	Clock driver	2
REG0-4	TI SN74ABT646	Farnell 204250	8bit registers	5
XOSC	IQD 100MHz oscillator		100MHz 8pin oscillator	1
F1-4	SMD Filter	Radionics CNF41	3-terminal bypass filter	16
C92 C96	axial capacitor	Farnell 430-870	0.1uF axial capacitor	2
C25-27 C35 C45 C53 C62 C75 C77 C82	SMD tantalum capacitor	Farnell 197-130	10uF 10V 1206 capacitor	10
C1-5 C20-24 C28-30 C34 C54 C63 C73 C78-85 C87-89 C91	SMD capacitor	Farnell 317-640	1uF 10% 0805 capacitor	28
C71	ceramic capacitor	Farnell 286-930	100pF capacitor	1
C72 C74 C76 C86 C90	tantalum capacitor	Farnell 643-701	22uf 16V capacitor	5
C6-19 C31-33 C36-44 C46-52 C55-61 C64-70 C93-95 C100-103 C105-138	SMD capacitor	Farnell 499-146	0.01uF 10% 0603 capacitor	88

C6-19 C31-33 C36-44 C46-52 C55-61 C64-70 C93-95 C100-103 C105-138	SMD capacitor	Farnell 578-174	0.022uF 10% 0603 capacitor	88
T1-54	SMD capacitor	Farnell 317-275	0.47uF 80% 0603 capacitor	54
T1-54	SMD resistor	Farnell 911-185	390ohm 1% 0603 resistor	54
R1-8	SMD resistor	Farnell 911-318	4.7Kohm 1% 0603 resistor	8
R9 R12-18	Metal film resistor	Farnell 514-184	4.7Kohm 10% resistor	8
R19-25 R29 R33-34	Metal film resistor	Farnell 513-623	22ohm 10% resistor	10
R30	Metal film resistor	Farnell 513-866	220ohm 10% resistor	1
R31-32	Metal film resistor	Farnell 513-908	330ohm 10% resistor	2
R35	Metal film resistor	Farnell	?ohm 10% resistor	1
R36	Metal film resistor	Farnell	?ohm 10% resistor	1
R37	Metal film resistor	Farnell	?ohm 10% resistor	1
R38	Metal film resistor	Farnell	?ohm 10% resistor	1
R39	Metal film resistor	Farnell	?ohm 10% resistor	1
R40	Metal film resistor	Farnell	?ohm 10% resistor	1
R27-28	SIP resistor	Farnell 106-466	220/330ohm 16 resistors	2
R10-11	SIP resistor	Farnell 148-983	4.7Kohm 8 resistors	2
VREG1-2	NatSemi LM39401T-3.3	Farnell 412-132	3.3V voltage regulator	2
PWRLED	LED	Farnell 595-524	wide angle LED	1
GND1-6	Ground pins	Farnell 329-551	test point pins	6
J1-22	strap block	Farnell 312-230	32pin strap block	3
PWRCON1	Socket Cable plug		4pin right angle socket 4pin cable plug	1
PWRCON2	Socket cable plug	Farnell 588-738 Farnell 588-910	4pin right angle socket 4pin cable plug	1
LVDSCON	Socket cable plug flat cable	Farnell 972-605 Farnell 525-418 Farnell 296-879	34pin right angle socket 34pin flat cable plug 30metres 34-way flat cable	1
JTAGIN JTAGOUT	Socket cable plug flat cable	Farnell 468-885 Farnell 525-364 Farnell 296-806	10pin socket 10pin flat cable plug 30metres 10-way flat cable	2
XTLCON	Socket cable plug flat cable	Farnell 468-915 Farnell 525-390 Farnell 296-843	20pin socket 20pin flat cable plug 30metres 20-way flat cable	1
E1-2 EC EXTCON	Socket cable plug flat cable	Farnell 468-940 Farnell 525-420 Farnell 296-892	40pin socket 40pin flat cable plug 30metres 40-way flat cable	4
NSCON0-1	Socket cable plug flat cable	Farnell 468-952 Farnell 525-431 Farnell 296-909	50pin socket 50pin flat cable plug 30metres 50-way flat cable	2



Trace Probe DT204.1

Patch List

1. Surface Wire Patches

1.1 none so far.

2. Internal Trace Patches

2.1 none so far.

3. Remaining Problems

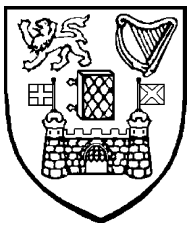
3.1 none so far.

4. Major Recent Fixes

4.1 dd-MMM-yyyy : none so far.

5. Still to be Done

5.1 Need to buffer the external interface so that it can be disabled with the JTAG /ENABLE signal to allow in-circuit programming of the MACH445 even when an external source is connected.



Trace Probe DT204.1

Document History

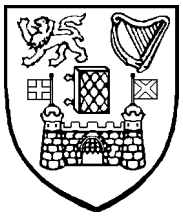
1. Created for DT202.1 on 3-JAN-1999.

2. Discontinued following decision to switch to designing DT203.1 trace probe for direct attachment to Dolphin D310 SCI board B-Link pads.

3. Revived and revised following Dassault's comments at Berlin meeting 17-MAR-1999, requiring attachment to Hewlett Packard HP1600 series probe sockets as per Dolphin's probe card. Changed to use DS90C283/DS90C284 in same way as DT203.1, since DS90C387/DS90CF388 development is delayed.

4. Revised following discussion with Bernhard Skaali 30-MAR-1999, to provide for attachment to SCILab tracer. DT200.1 database definitions also changed to match.

5. 18-MAY-1999 : TXSYN is on 25th bit, not 28th bit.



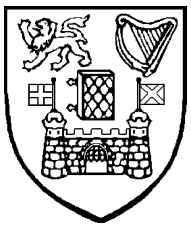
Computer Architecture Group
Department of Computer Science
Trinity College Dublin
Ireland

Tel : +353-1-6081765
Fax : +353-1-6772204

Probe Adapter DT205.1

Technical Manual

B.A.Coghlan
M.Manzke



Probe Adapter DT205.1

Technical Manual

Introduction

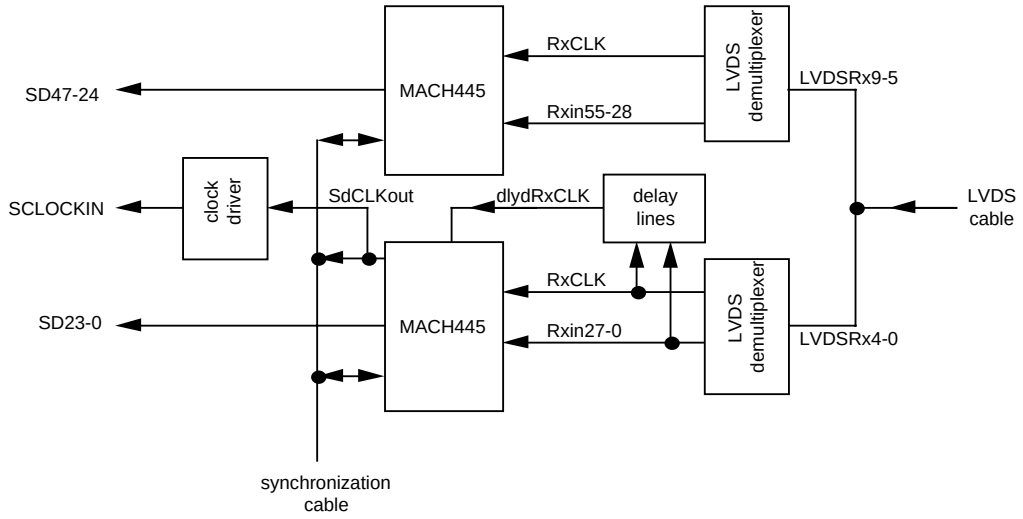
The DT205.1 Probe Adapter allows simple attachment of the DT200.1 Deep Tracer to trace probes for IEEE 1596 Scalable Coherent Interconnect (SCI) systems. Two trace probes and probe adapters are needed, one pair of each to attach to each one of the two deep trace boards

Features

- Simple deep tracer interface
  34-way LVDS cable.
- 48bit trace data samples
  Max Sample Rate 66MHz.
- Synchronizing buffer
  +/-25nS skew tolerance.

Probe Adapter Functional Overview

A simplified schematic of the probe adapter is shown below.



Each probe adapter attaches to 48bits of a 96bit sample data path. A flat 34-way cable (typically a floppy-disk cable), carrying eight differental signals plus two differential clocks, connects the LVDS inputs to J1 on the probe adapter at the deep trace board. The cable pinout is as follows :

Left	Right
Tx0OUT0M	Tx0OUT0P
AGND	AGND
TX0OUT1M	Tx0OUT1P
AGND	Tx0OUT3M
Tx0OUT3P	AGND
Tx0OUT2M	Tx0OUT2P
AGND	AGND
Tx0CLKM	Tx0CLKP
N.C.	N.C.
Tx1OUT0M	Tx1OUT0P
AGND	AGND
Tx1OUT1M	Tx1OUT1P
AGND	Tx1OUT3M
Tx1OUT3P	AGND
Tx1OUT2M	Tx1OUT2P
AGND	AGND
Tx1CLKM	Tx1CLKP

Two probe adapters are synchronized via a cable that connects to J6, which has the following pinout :

GND	SCLOCKIN
GND	SDSYN
GND	RDADR[0]
GND	RDADR[1]
GND	N.C.

The LVDS data signals are parallel terminated by 100 ohms across each differential pair. These multiplexed LVDS signals are then demultiplexed using two DS90C284 devices, IC2 for the low 24bits, and IC1 for the high 24bits. Each generates a 28bit demultiplexed low voltage TTL data output, representing a 24bit trace sample stream plus four control signals.

Since the data from different devices may be skewed (relative to each other) at the end of the LVDS cables, a synchronizing pulse RXSYN is received over the 25th output bit; which repeats every 3 clock cycles. This is used to synchronize the four 24bit trace sample streams over two probe adapters into one synchronous 96bit stream.

The synchronizer is programmed into two MACH445 pals, IC4 for the low 24bits and IC3 for the high 24bits. These create a three-stage buffer that is written to by the DS90C284, and read from by the deep tracer. A buffer write address counter is clocked from the DS90C284, but is reset every 3 cycles by the synchronizing pulse. Three stages allow a LVDS skew tolerance of +/-25nS, more than twice the minimum margin for a DS90C284 at 66MHz.

A delayed clock and synchronizing pulse are generated by the delay lines IC6 and IC7; these are fed to each MACH445 pal on a probe adapter. One of the four MACH445 pals of a pair of probe adapters is selected as master via strap J7 as follows:

Role	J7 Strap
Master	A-B
Slave	-

The master then generates a read clock and synchronizing pulse, and uses these to clock and reset a buffer read address counter. From this it generates read address outputs, which are used by all four MACH445 pals to read the buffer. The clock, synchronizing pulse and read address signals are distributed over the two probe adapters via the synchronizing cable.

The MACH445 pal can also be used as a test pattern generator. It may be programmed via a JTAG interface using the MACHXL software.

The MACH445 pal can further be employed to match specific input data patterns, again programmed via the JTAG interface using the MACHXL software. The match results can be pipelined to the tracer via the control fields.

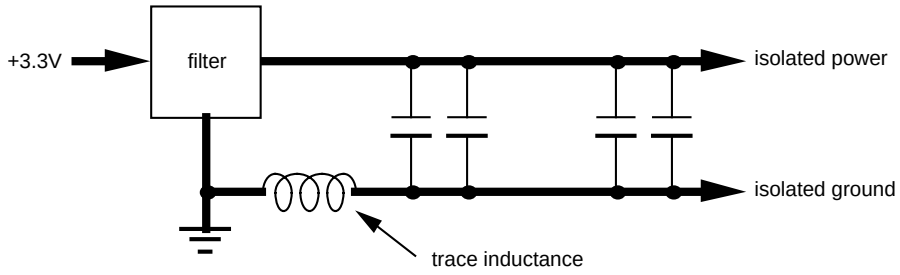
Two JTAG connectors are provided. The upstream of the JTAG chain connects to J3, and the downstream connects to J4. Their pin connections are :

TCK	ZCTL
TMS	GND
TDI	TVCC
TDO	GND
/TRST	ENABLE

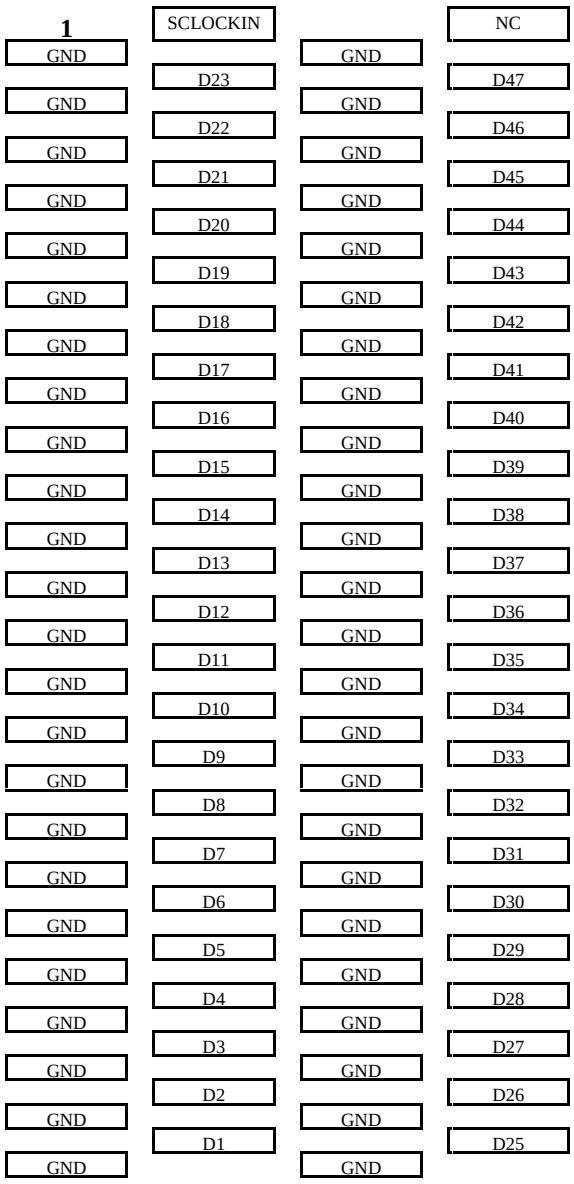
In the event that there is no downstream chain, TDI should be strapped to TDO at connector J4. Note that signals /TRST, /ENABLE and TVCC are resistively pulled up to 5V, while signal ZCTL is resistively pulled down to ground.

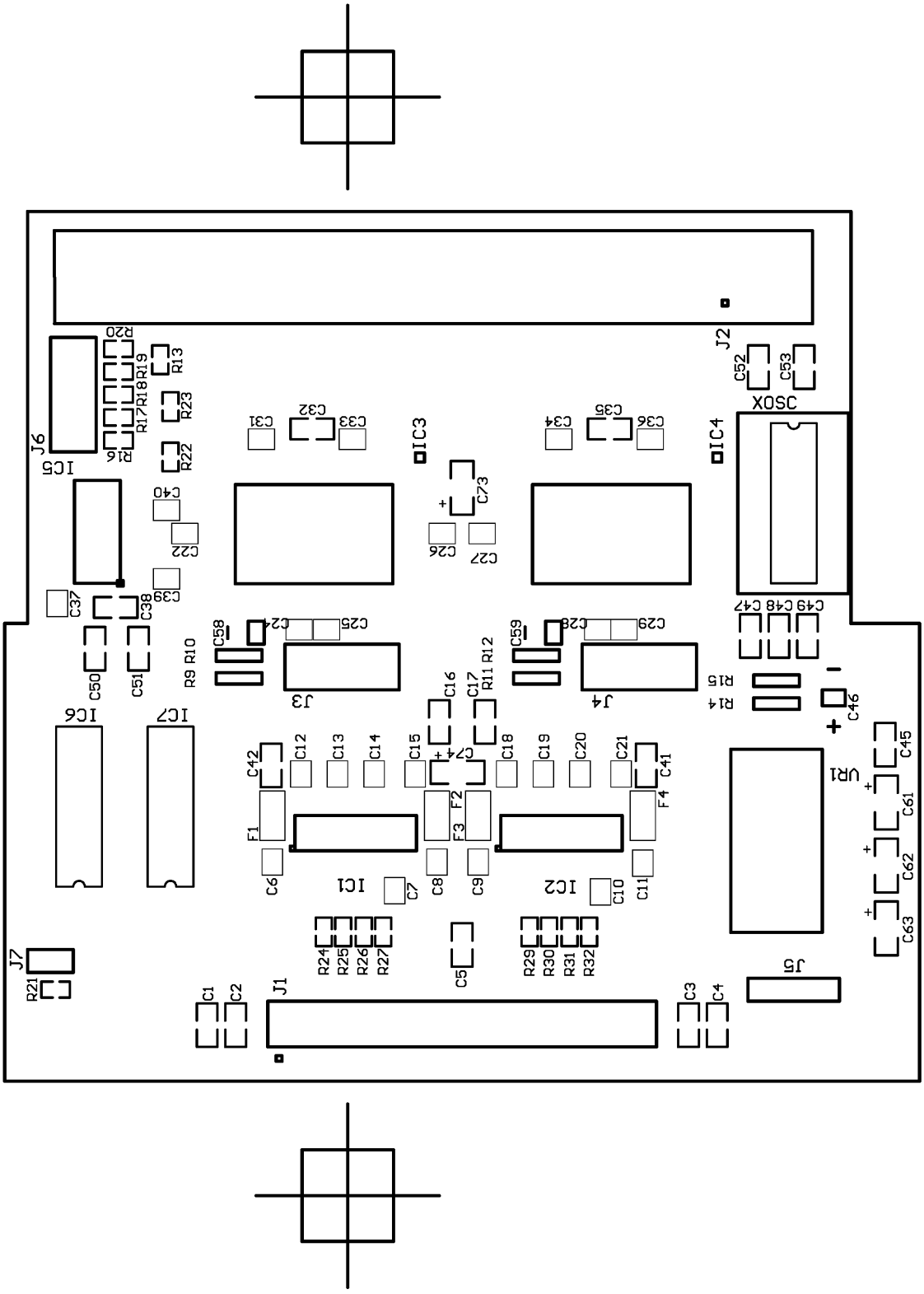
Strap J8 can be shorted to power down the DS90C284 devices.

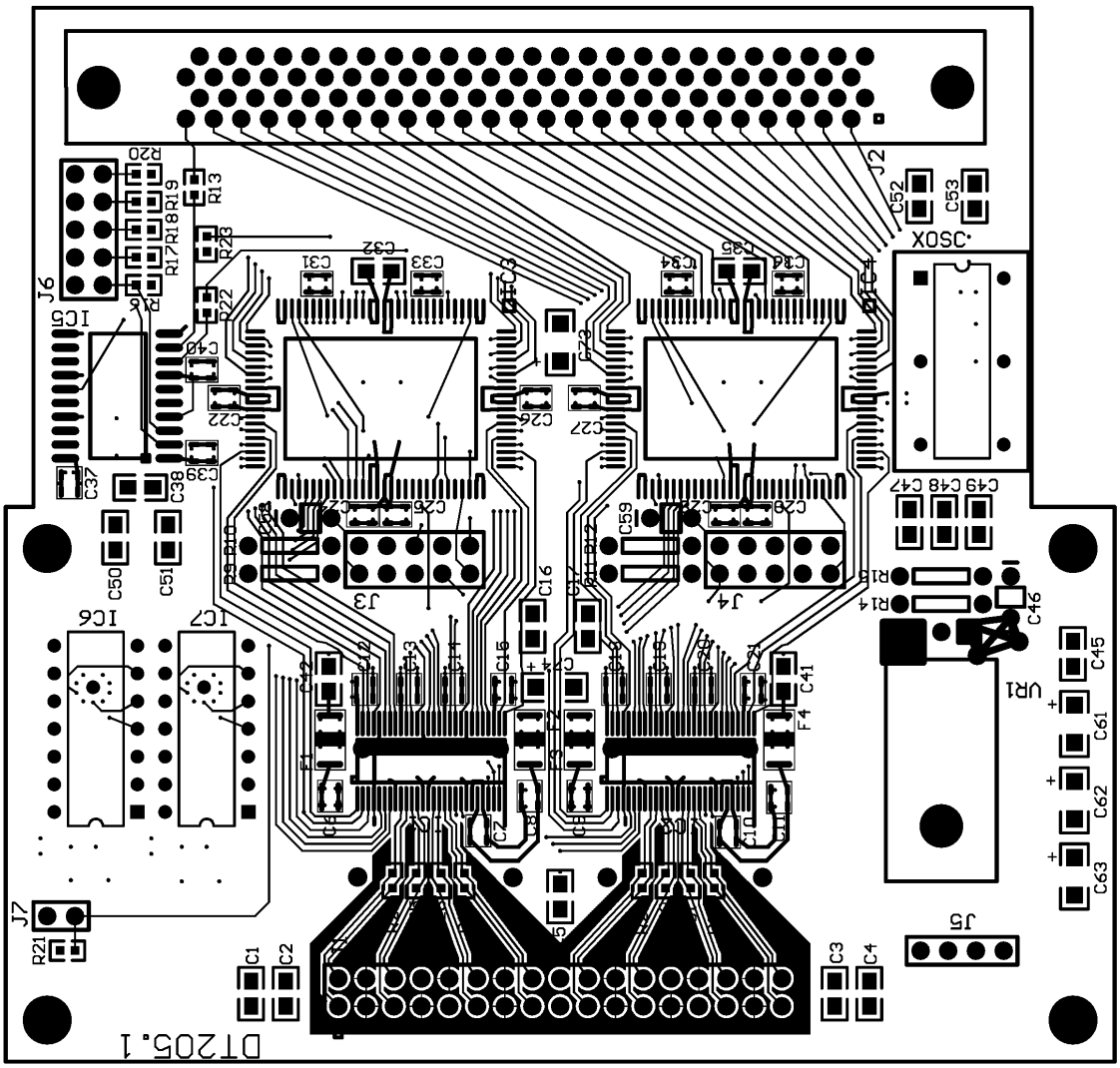
5V power is normally obtained from J2, but for standalone debugging it can be supplied via J5. A 3.3V voltage regulator then generates 3.3V for the DS90C284 and MACH445 devices. There are three internal PCB power planes : +5V, +3.3V and ground. The DS90C284 devices have isolated power and grounds for both the LVDS interfaces and their phase-lock loops; power is isolated via filters while ground is isolated via trace inductances.

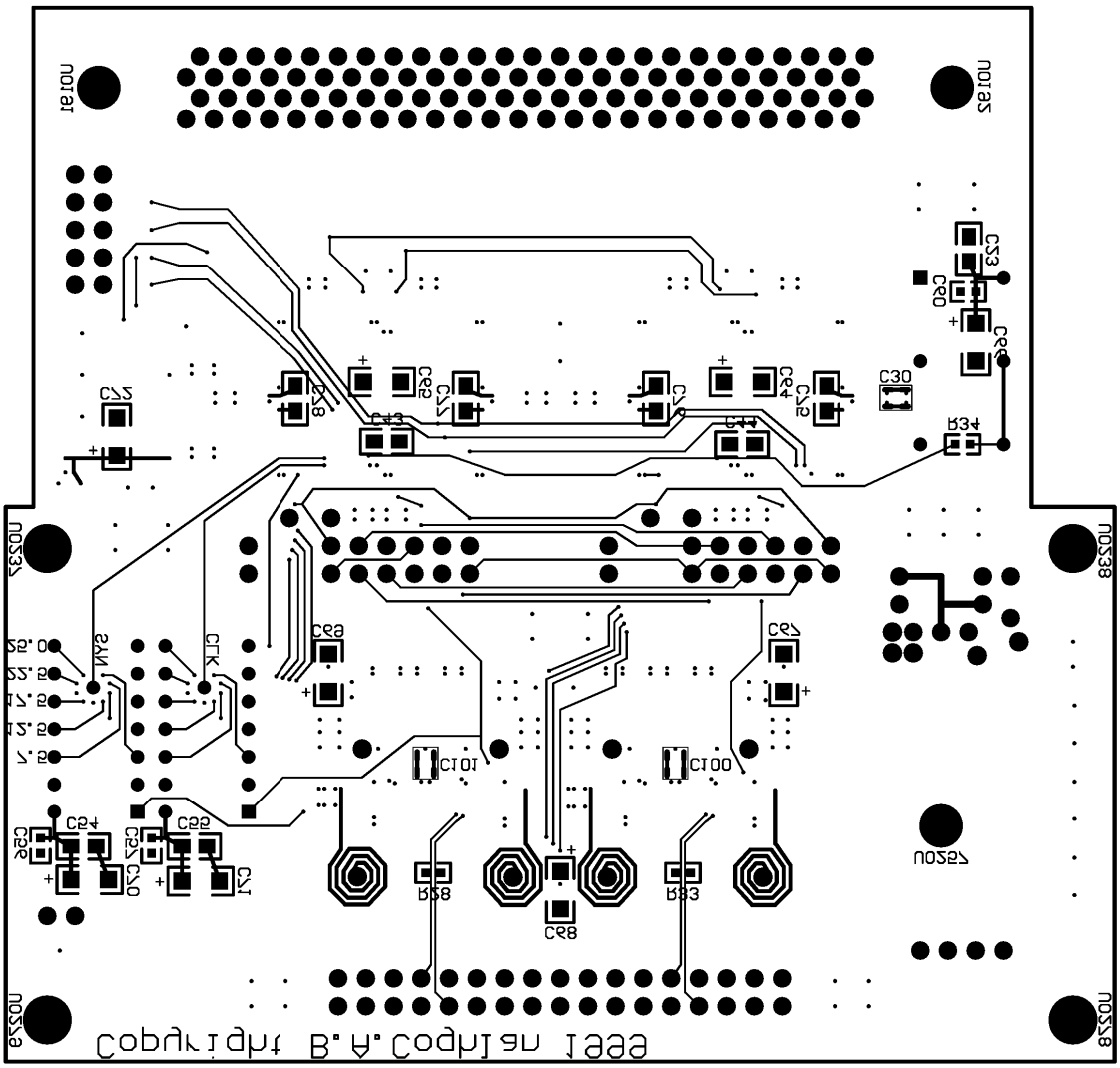


The MACH445 pals output the 48bit sample stream to the deep tracer via J2. A CDC340 clock driver buffers the clock to drive the deep tracer. The pinout of J2 board (from the component side of the connector) is as follows :


1
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
SCLOCKIN
D23
D22
D21
D20
D19
D18
D17
D16
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
NC
D47
D46
D45
D44
D43
D42
D41
D40
D39
D38
D37
D36
D35
D34
D33
D32
D31
D30
D29
D28
D27
D26
D25


J6
IC5
R20
R19
R18
R17
R16
R13
R23
R22
C40
C22
C37
C38
C39
C50
C51
R9
R10
C58
C24
C25
J3
C16
C17
R11
R12
C59
C28
C29
J4
R15
R14
C46
C45
C61
C62
C63
VR1
IC6
IC7
C42
C12
C13
C14
C15
C74
C18
C19
C20
C21
C41
F1
F2
F3
F4
C6
IC1
C7
C8
C9
IC2
C10
C11
J7
R21
R24
R25
R26
R27
C5
R29
R30
R31
R32
J5
C1
C2
J1
C3
C4
J2
C52
C53
XOSC
IC3
C31
C32
C33
IC4
C34
C35
C36
C73
C26
C27
C49
C48
C47


DT205.1
J2
J3
J4
J5
J6
J7
IC5
IC6
IC7
XOSC
VR1



Electrical Characteristics

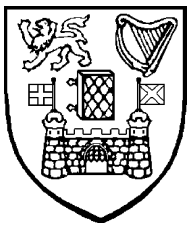
minimum logical 1 input voltage	2.0 Volts
maximum logical 1 input voltage	5.5 Volts
minimum logical 0 input voltage	-0.5 Volts
maximum logical 0 input voltage	0.8 Volts
capacitive loading per input under test	TBD
minimum SCLOCKIN frequency	0 Hz
maximum SCLOCKIN frequency	66 MHz
minimum SCLOCKIN logical 0 duration	5 nS
minimum SCLOCKIN logical 1 duration	5 nS
SD[0..47] setup time relative to SCLOCKIN positive transition	5 nS
SD[0..47] hold time relative to SCLOCKIN positive transition	1 nS
supply current	TBD

Parts List

The parts list is :

No.	Part No	Supplier	Description	Quantity
	DT2051	ECS	PCB	1
IC1 IC2	NatSemi DS90C284	EBV	LVDS demultiplexer	2
IC3 IC4	AMD M4LV-128/64-7YC	Lyco	MACH445 GAL	2
IC5	TI CDC340	Farnell 149-230 (NEWK4063)	Clock driver	1
IC6 IC7	Newport 50A10250	Farnell 203-208	25nS Delay line	2
XOSC	IQD 100MHz oscillator	Farnell 101-412	100MHz 14pin oscillator	1
F1-4	SMD Filter	Radionics CNF41	3-terminal bypass filter	4
C58 C59	ceramic capacitor	Farnell 286-930	100pF capacitor	1
C1-5 C16-17 C23 C32 C35 C38 C41-45 C47-55 C75-78	SMD capacitor	Farnell 317-640	1uF 10% 0805 capacitor	25
C46	tantalum capacitor	Farnell 643-701	22uF/16V capacitor	1
C6-15 C18-22 C24-31 C33-34 C36-40 C100 C101	SMD capacitor	Farnell 499-146	0.01uF 10% 0603 capacitor	31
C6-15 C18-22 C24-31 C33-34 C36-40 C56-57 C60 C100 C101	SMD capacitor	Farnell 578-174	0.022uF 10% 0603 capacitor	34
C61-74	SMD tantalum capacitor	Farnell 197-130	10uF 10V 1206 capacitor	14
R9-12 R14-15	Metal film resistor	Farnell 514-184	4.7Kohm 10% resistor	6
R24-33	SMD resistor	Farnell 911-112	100ohm 1% 0603 resistor	10
R13 R16-20 R22-23 R34	SMD resistor	Farnell 911-033	22ohm 1% 0603 resistor	9
R21	SMD resistor	Farnell 911-239	1kohm 1% 0603 resistor	1
VR1	NatSemi LM39401T-3.3	Farnell 412-132	3.3V voltage regulator	1
J7	strap block	Farnell 312-230	32pin strap block	1

J5	Socket cable plug	Farnell 588-738 Farnell 588-910	4pin right angle socket 4pin cable plug	1
J1	Socket cable plug flat cable	Farnell 972-605 Farnell 525-418 Farnell 296-879	34pin right angle socket 34pin flat cable plug 30metres 34-way flat cable	1
J3-4 J6	Socket cable plug flat cable	Farnell 468-885 Farnell 525-364 Farnell 296-806	10pin socket 30metres 10pin flat cable plug 10-way flat cable	3
J2	plug	AMP 749084-9	100pin right angle plug	1



Probe Adapter DT205.1

Patch List

1. Surface Wire Patches

1.1 none so far.

2. Internal Trace Patches

2.1 none so far.

3. Remaining Problems

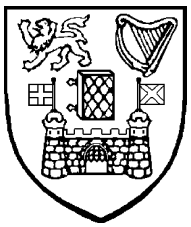
3.1 none so far.

4. Major Recent Fixes

4.1 dd-MMM-yyyy : none so far.

5. Still to be Done

5.1 none so far.



Probe Adapter DT205.1

Document History

1. Created 10-MAR-1999.

2. 18-MAY-1999 : added layouts, updated J1 pinout, and RXSYN is on 25th bit, not 28th bit.