AccessionIndex: TCD-SCSS-T.20121208.063
Accession Date: 8-Dec-2012
Accession By: Dr.Dan McCarthy
Object name: Intel iPSC Hypercube
Vintage: c.1985
Synopsis: First commercial hypercube parallel machine. S/N: ???.

Description:
Hypercube machines were invented in 1981 by Chuck Seitz and Geoffrey Fox at Caltech. Seitz constructed a series of hypercubes, starting with a 4-node proof-of-concept with nodes containing an Intel i8086/8087 CPU/FPU and 128kB RAM. He and his students then built the famous 64-node *Cosmic Cube*, dimensioned 4 x 4 x 4 specifically to accelerate Fox's QCD calculations.

Hypercube machines are homogenous ensembles that have a computing node at each vertex of an N-dimensional cube, and interconnections along the cube's edges. One virtue is that each node only connects to its N neighbouring nodes, not to all 2^N nodes.

Intel's director of engineering, Gordon Moore (of *Moore's Law*), was a Caltech alumni and Board member, and after a demo of the Cosmic Cube at a board meeting decided that Intel should develop a commercial version, and shortly afterwards founded a new group, Intel Scientific Computers, led by Justin Rattner, where Ratther and Cleve Moler led a team that developed the Intel iPSC/1 Hypercube.

The iPSC/1 was the first parallel computer built from commercial off-the-shelf parts, and the first commercial hypercube parallel machine. Intel announced the iPSC/1 in 1985, with 32-128 compute nodes connected into a hypercube, managed by a Multibus-based *cube manager* host (an Intel 286/310 with 2MB RAM, 140MB disk, running Xenix, plus VT100-compatible terminal for user interactions). Each node consisted of an Intel i80286 CPU with i80287 math coprocessor, 512kB of 16-bit RAM, seven hypercube communication ports plus another to connect to the host, and a Multibus iLBX-II expansion interface. Eight Intel i82586 10Mbps Ethernet communications coprocessors interconnected the nodes via a 34-slot backplane within a cabinet and via Ethernet between cabinets. Communication was by message-passing. On each node a green LED indicated 'working' and a red LED indicated 'idle' (on later models a yellow LED indicated 'FPU working'), so users could observe the LEDs and imply behaviour and even efficiency. Overall performance was about 2MFlops, about 10% of a Cray-1, the fastest machine of the time.

The overheads and latencies of the relatively immature networking technologies of the time significantly degraded performance (iPSC/1 packet-switched routing took several mS and latency was proportional to hops), so in 1986 William J.Dally, then a PhD student of Seitz, developed the also-famous *Torus Routing Chip* that introduced byte-wide deadlock-free cut-through routing over virtual channels, yielding 10-times better performance than the Cosmic Cube or Intel iPSC networks.

The Department of Computer Science in TCD was given a 16-node (???) Intel iPSC/1 Hypercube in 1985 <<<< ***Date??? How???*** >>>, which was installed in the O'Reilly Institute. The principal users were Dr.Dan McCarthy and students who took his 3rd-year undergraduate computer architecture course. The original configuration had:

Qty	Item	Description
1	Intel 286/310	Cube manager
16	Intel iPSC/1 nodes	Hypercube compute nodes
1	Terminal	Console

<<< ***This was later expanded ???*** >>>

The iPSC/1 included a
<<< ***OS, utilities, assembler, FORTRAN IV, scientific libraries ???*** >>>.

The collection retains the iPSC/1 Hypercube but not the cube manager or its terminal.

Accession Index	Object and Identification
TCD-SCSS-T.20121208.063	Intel iPSC/1 Hypercube.

References:

1. Cosmic Cubism, Engineering & Science, March 1984,
   http://calteches.library.caltech.edu/3419/1/Cubism.pdf

2. Birth of the Hypercube,
   http://www.netlib.org/utk/lsi/pcwLSI/text/node13.html

3. Bitsavers iPSC/1 product summary,
   https://archive.org/details/bitsavers_inteliPSCimary_9667685
   Downloaded 12-May-2015.

See the associated set of documents in the related folder in this catalog.

Figure 1: Intel iPSC Hypercube front three-quarter view, doors closed
Photograph courtesy Tom Kearney

Figure 2: Intel iPSC Hypercube front three-quarter view, doors open
Photograph courtesy Tom Kearney

Figure 3: Intel iPSC Hypercube left rack front three-quarter view
Photograph courtesy Tom Kearney

Figure 4: Intel iPSC Hypercube left rack closeup
Photograph courtesy Tom Kearney

Figure 5: Intel iPSC Hypercube left rack upper blade chassis
Photograph courtesy Tom Kearney

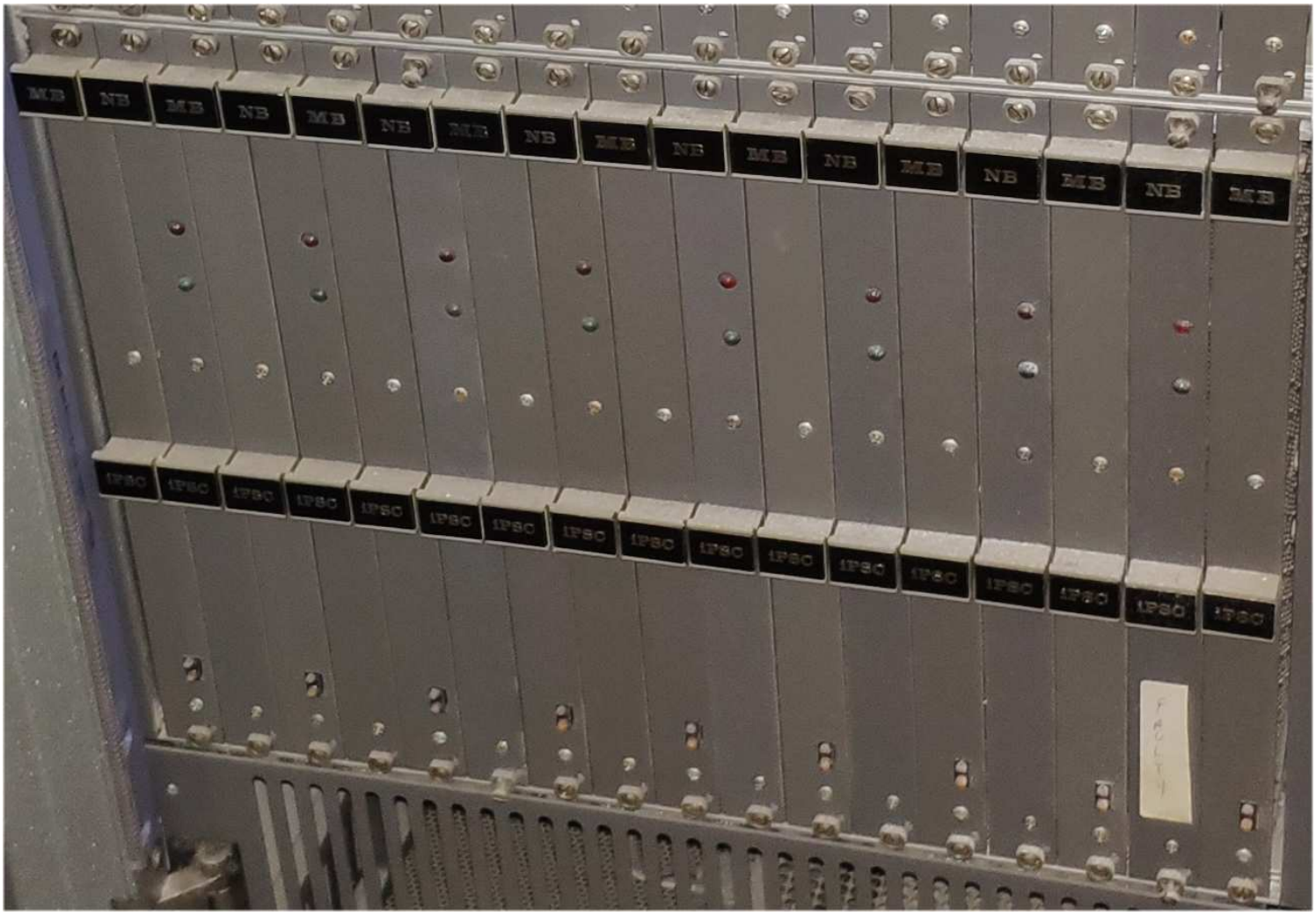

Figure 6: Intel iPSC Hypercube left rack lower blade chassis
Photograph courtesy Tom Kearney