AccessionIndex: TCD-SCSS-T.20121208.032
Accession Date: 8-Dec-2012
Accession By: Prof.J.G.Byrne
Object name: Burroughs 1714
Vintage: c.1972
Synopsis: Commercial zero-instruction-set computer used by the Dept.Computer Science from 1973-1979. Just two prototyping boards survive.

Description:
The Burroughs 1714 was one of their B1700 family, introduced in 1972 to compete with IBM's System/3. The original research for the B1700 series, initially codenamed the *Proper Language Processor* or *Program Language Processor* (PLP) was done at the Burroughs Pasadena plant. The family were known as the Burroughs Small Systems, as distinct from the Burroughs Medium Systems (B2000, etc) and the Burroughs Large Systems (B5000, etc). All the Burroughs machines had high-level language architectures. The large were ALGOL machines, the medium COBOL machines, but the small were universal machines.

The principal designer of the B1700 family was Wayne T. Wilner. He designed the architecture as a zero-instruction-set computer, an attempt to bridge the inefficient semantic gap between the ideal solution to a particular programming problem and the real physical hardware. The B1700 architecture executed idealized virtual machines for any language from virtual memory. It achieved this feat by microprogramming, see the microinstruction set further below. The Burroughs MCP (Master Control Program) would schedule a particular job to run, then preload the interpreter for whatever language was required into a writeable control store, allowing the machine to emulate the desired virtual machine.

The hardware was optimised for this. It had bit-addressable memory, a variable-width ALU, could OR in data from a register into the instruction register (for very efficient instruction parsing), and the output of the ALU was directly addressable as X+Y or X-Y read-only registers. The machines had 16-bit microinstructions and 24-bit datapaths, and a disk file as the virtual memory device. They used Fairchild Semiconductor’s CTL logic, multiplexers and PROMs.

The B1714 (along with the B1714 and B1726) was introduced in Jun-1972 in the price range of $75,000-$200,000. It had a processor cycle time of 250nS. Memory could be expanded from 16-64kB in 8kB increments. Up to 8 buffered I/O channels could be added, as well as relatively fast and large removable disks. A cassette tape reader was used for boot loading and diagnostics.

The Department of Computer Science in TCD installed a Burroughs 1714 in 1973. Quite a lot of work migrated from the IBM 360/44 to the B1714, as it relieved the pressure on the over-utilised and near-end-of-life IBM machine in the period prior to its replacement by a DEC-2020.

The original configuration had:

Qty	Item	Description
1	B1714 CPU and SPO	
1	64kB memory	666nS 24-bit memory
1	Console	
1	A9480-12 dual disk drive	
1	A9115 card reader	
1	A9359.2 line printer	

The B1714 used by the Dept.Computer Science from 1973-1979, was disposed of in 1984(?) to Peter Tully (now at IT-Tallaght), and its last known location was in his brother's warehouse in Sandyford, long gone but dearly desired. Any further information on its subsequent location is very much welcomed.

What has survived are two Burroughs 1714 prototyping boards with wirewrap logic designed and implemented c.1978 by Peter Chadwick (in fulfilment of his MSc) to implement a serial interface between the Dept.Computer Science's Burroughs 1714 and its IBM 360/44. It incorporated a General Instrument CP1600 16-bit microprocessor, 2kB RAM, 8kB EPROM, 2 x UART, a board full of CTL and TTL discrete logic for a B1714 I/O bus controller with 16 x 16-bit LIFO buffer (the inter-processor interface, or IPIF), and switches and lights.

Accession Index	**Object with Identification**
TCD-SCSS-T.20121208.032.01	Burroughs 1714 prototyping board 1. Principal components: Intel C1702A-2 256 x 8-bit EPROM marked F7 Intel C1702A-2 256 x 8-bit EPROM marked G7 2 x Intel P8212 4 x Intel P3101A 2 x Intel P3205 4 x Intel D8216 Various resistors and small transistors Markings: ‘Copyright P.Chadwick 1975’
TCD-SCSS-T.20121208.032.02	Burroughs 1714 prototyping board 2. Principal components: Northern Engineering Labs quartz crystal NE-6A SMC 7607 COM 5016 6 x Intel D8216 3 x Intel P3408A 2 x Intel P3212 Motorola MC6850L ACIA AMI S6850P ACIA Exar XR1488 Exar XR1489A 16 x General Instrument RA-3-4402 4K x 1-bit SRAM Markings: ‘Copyright P.Chadwick 1975’

The G.I. CP1600 CPU is itself interesting, the result of joint work with Honeywell, based on the PDP-11. It had eight 16-bit special-purpose registers, where R0 was an accumulator, R1-3 were counters, R4-5 auto-incremented, R6 was the stack pointer, and R7 the PC. Instructions were one to three words long, but 6 unused instruction bits appear to have been reserved for coprocessors. I/O was memory-mapped. It was an nMOS design in a 40-pin DIP package, needed +12, +5, -3 V, and ran at 3.3 MHz, and had a multiplexed address/data bus. It appears to be missing, and indeed there is no 40-pin socket to accommodate it, so it must have been elsewhere.

<<<<<< ***Where was the G.I. CP1600 ???*** >>>>>>

<<<<<< ***Was it on an 'evaluation board' connected via flat cable ???*** >>>>>>

<<<<<< ***OR, was it on another (now missing) board ???*** >>>>>>

References:

1. Wilner, W.T., B1700 Design and Implementation, Burroughs Corporation, Santa Barbara, USA, May-1972.

2. B1714 Maintenance and Basic Software Performance Oriented Training, http://www.textfiles.com/bitsavers/pdf/burroughs/B1700/1093671_B1714mntTrain_Mar76.pdf Burroughs Corporation, Detroit, Michigan, USA, 1976.

3. Bitsavers B1700 documents and brochures, http://www.bitsavers.org/pdf/burroughs/B1700/B1700_brochures/ Downloaded 21-Apr-2015.

4. Chadwick, P., A Microcomputer Based Data Communications Controller for the Burroughs B1714, MSc Thesis, Dept.Computer Science, Trinity College Dublin, 8-Aug-1978.

See the extensive set of documents in the related folder in this catalog.

Burroughs
B 1714
Central System

The B 1714 is an exceptionally productive, responsive, and efficient system for business, industrial and financial data processing and engineering / scientific computation. Its outstanding capabilities are provided through:

- "Fourth generation" design
  Combines microprograming with the latest circuitry design and integrated circuit memory technology.

- Variable micrologic
  Alters the processor's logical operation dynamically to optimize performance with a variety of program languages. You determine which standard languages are best for your requirements. As programs are being run, variable micrologic creates the ideal processor environment for each one. This innovative technique provides a new level of multi-language efficiency in the B 1714 cost/performance range.

- Master Control Program
  A comprehensive executive system which supervises B 1714 operation. This powerful tool, which has fully proven its superiority in use with larger Burroughs data processing systems, manages system resources so that your manpower resources can be devoted to constructive problem solving. The Master Control Program assigns memory, manages input/output functions, communicates with the operator, logs system use, loads programs, maintains a library of all files, and supervises other functions, all of which contribute to simpler programing, ease of system operation, and maximization of throughput.

- A complete range of peripheral devices:
  96-Column Punched Card Input/Output.
  80-Column Punched Card Input/Output.
  Line Printers.
  Disk Cartridge Drives.
  Magnetic Tape Input/Output.
  MICR Input.
  Console Printer with keyboard for operator/machine communication and inquiry.
  Data Communications.

- Complete, powerful system software:
  Master Control Program (MCP).
  COBOL Compiler.
  FORTRAN Compiler.
  RPG Compiler.
  BASIC Compiler.
  SORTS.
  UTILITIES.

Figure 1: Burroughs B1714 brochure

Features Summary

Burroughs leadership in multiprograming systems spans over a decade of development, refinement, and achievement in the "real world" of customer installations. Burroughs systems consistently deliver superior multiprograming performance on-the-job.

The Master Control Program (MCP II) is a unique operating system adapted to the B 1700's advanced fourth generation design. Inherent MCP capabilities lend power to the B 1700 and Business Management Systems to produce the results you want.

Description	Characteristics	Benefits	Results
VARIABLE MICROLOGIC			
The B 1700 instantly alters its logical operation to optimize the performance of a given language. In effect, one processor acts as many processors to fit the specific needs of the program language of the moment.	Unique microprogramed interpreters complement your high level programing languages.	Less memory required.	EFFICIENCY
		Faster execution.	IMPROVED COST/ PERFORMANCE
DYNAMIC MULTIPROGRAMING			
The MCP dynamically reassigns otherwise idle processor cycles to multiple, independent jobs.	Multiple, independent jobs share processor cycles.	Reduced idle time. Improved system use. Greater scheduling flexibility.	INCREASED THROUGHPUT
	Memory management technique keeps the processor fully employed on segments of independent programs.	Virtual memory operation. Reentrant programs. Memory modularity.	BETTER SYSTEM USE
	The I/O subsystem handles reads and writes of multiple, independent programs without conflict or congestion.	Data transfer at memory speed. Pseudo-peripherals.	FASTER TURN-AROUND FOR JOB STREAMS
REENTRANT PROGRAMS			
The capability of allowing program logic to be used by two or more independent users at the same time.	Program code is never modified, so multiple users may execute the same job at the same time.	Memory space is truly shared by multiple users.	GREATER PRODUCTIVITY
	User data integrity is enforced through BASE and LIMIT registers.	Several people may share memory and program logic while independent sets of data are being analyzed and modified.	MAXIMIZED MEMORY USE
VIRTUAL MEMORY			
Automatically brings routines and data into memory from disk storage during processing only as they are required.	Programs need not occupy contiguous memory space. No partitions in memory.	Greater use of memory. More jobs in memory.	GREATER SCHEDULING FLEXIBILITY
	Memory space for data, program code, and files is not allocated until run time.	Large programs occupy minimum memory space. More jobs in memory to keep peripherals busy.	LESS MEMORY REQUIRED

Figure 2: Burroughs B1714 brochure

Description	Characteristics	Benefits	Results
DYNAMIC RESOURCE ALLOCATION			
The B 1700's automatic assignment of system resources to meet job requirements.	Assignment of disk file space is based upon file growth requirements. Files do not require contiguous areas on disk.	Less storage space is required. Ease of growth without reprograming.	SIMPLICITY IN SYSTEMS DESIGN AND PROGRAMING
	New components (memory, peripherals, disk) are recognized immediately and used to process work faster than before.	Immediate productivity per processing dollar. No reprograming. Easier systems design.	RESPONSIVENESS
	A comprehensive job priority system permits management to direct the system in favor of one job over another.	Scheduling flexibility. More manageable system.	MANAGEMENT CONTROL
COMPLETE SELF-REGULATION			
The B 1700 can analyze and decide how to make the utmost use of its own resources.	Program modules and memory space are managed dynamically.	Less machine idle time. Less memory required. Fewer operator decisions.	EFFICIENCY OF OPERATION
	Processor is efficiently shared according to job priorities.	Responsiveness to change. Equipment is fully utilized.	GREATER THROUGHPUT
	Peripherals, pseudo-peripherals, and disk file space are assigned dynamically.	Fewer real peripherals needed. Less disk required. Growth without reprograming.	LOWER COST
POWERFUL I/O DESIGN			
The B 1700's input/output subsystem eliminates the congestion usually found in most other I/O subsystems, and makes truly flexible multiprograming possible.	Each peripheral control has its own logic to communicate with a predetermined peripheral device.	Control operates concurrently with processor.	GREATER THROUGHPUT
	Each peripheral control has its own buffer for accumulating data prior to transferring that data to memory for program use.	Less congestion in system. Data is transferred from control to memory at memory speed.	MAXIMIZED SYSTEM PERFORMANCE

Burroughs B 1700 Systems deliver large system results at small to medium system cost to meet all your data processing requirements economically at peak efficiency. A demonstration can prove it!

Figure 3: Burroughs B1714 brochure

COMPUTERWORLD

THE NEWSWEEKLY FOR THE COMPUTER COMMUNITY

Weekly Newspaper

Second-class postage paid at Boston, Mass., and additional mailing offices

Price: $9/year | June 14, 1972 | Vol. VI No. 24

NEWSPAPER

NEWS IN BRIEF

1,202 Candidates Pass '72 CDP Exam

PARK RIDGE, Ill. – Of the 2,603 candidates who sat for the 1972 Certificate in Data Processing (CDP) examination last February, 1,202 passed.

The new CDP recipients bring to 13,142 the total number granted the certificate, out of 24,742 candidates who sat for the examination, since the first exam was given in 1962, according to the Certification Council.

The Certification Council is responsible for policy-making, planning and directing the CDP exam which covers five areas: data processing equipment; computer programming and software; principles of management; quantitative methods; and systems analysis and design.

2 Workers Have Short Stay On Job Thanks to NCIC

NEW ORLEANS – A police demonstration of the computer terminal that communicates with the FBI's National Crime Information Center (NCIC) "terminated" the employment of two city employees, after one hour on the job.

The employees were the subjects of two separate inquiries this spring.

Small-Scale Series

B1700s Use Variable Micrologic

By Frank Piasta
Of the CW Staff

DETROIT – The newest of the B700s, the B1700 Series demonstrated last week by Burroughs, may be the hottest of them all.

The small-scale business computer system incorporates user and technical features unique for its class. These include such advanced features as variable micrologic, word length variable down to one bit, high-level programming through micrologic interpreters rather than conventional compilers, virtual memory techniques and solid state memories.

The B1700 systems, three so far, can be equipped with a variety of peripherals, including both 80- and new 96-column card equipment, and a new series of MICR readers as well as a selection of tapes, disks and communications gear.

The software has not been neglected by Burroughs, as shown by the availability of a full operating system with multiprogramming, program relocation, automatic spooling, job scheduling, operator communication and utilities.

A basic configuration of the Burroughs B1712 includes the multipurpose card unit for 96-column cards, console typewriter, two disk cartridge drives and a line printer.

The user has a choice of four programming languages – Cobol, Fortran, RPG and Basic – with more promised for the future. Object code is compatible among all B1700 systems but not with other B700 systems, Burroughs said.

Main memory for all systems is of the integrated circuit type with a cycle time of 666 nsec/24 bits (3 bytes). The addressability of the memory to the bit level eliminates the need for predefined data structures such as words or bytes and results in more efficient use of memory, Burroughs explained.

The virtual memory structure of the B1700 resembles that of the larger B5500 and B5700 systems. All code segments are reentrant and overlayable. Data can be either saved or overlayed, under program control. A base-to-limit register is used for addressing data in storage. The virtual memory device is a disk file with a minimum of 4.6M bytes.

The smallest of the systems, the B1712 has a processor cycle time of 500 nsec. Basic memory is 16K bytes, expandable to 40K in 8K-byte increments. Up to

(Continued on Page 2)

HEW Questions DP Use Of SS Numbers for ID

By Edward J. Bride
Of the CW Staff

WASHINGTON, D.C. – The increasing use of the Social Security number as an "identifier" of individuals, plus "potendation from a task force of the American National Standards Institute (Ansi), which proposed a standard personal identifier for information interchange.

This identifier, Martin continued, would

Figure 4: Burroughs B1714 introduction

Virtual Memory Included

(Continued from Page 1)

eight I/O controls with buffers can be attached to handle such peripherals as 80- and 96-column card equipment, line printers, disk cartridge drives, magnetic tape drives and a console with I/O printer.

Purchase prices for the B1712 range from $70,000 to $120,000, with comparable monthly lease prices from $1,500 to $2,800.

The second of the series, the B1714, boasts a processor cycle time of 250 nsec. The basic memory of 16K bytes can be expanded to 64K in increments of 8K. Up to eight buffered I/O controls can handle MICR readers and data communications equipment in addition to the peripherals available with the B1712.

B1714 purchase prices range from $75,000 to $200,000. Comparable monthly lease prices range from $1,600 to $3,500.

The largest of the three models, the B1726, has a processor speed of 167 nsec. In addition to the main memory available in 8K or 16K increments from 24K to 96K bytes, the system has a high-speed control memory with a capacity of either 2K or 4K bytes. Read cycle time for the control memory is 167 nsec/16 bits and write cycle time is 225 nsec. Micrologic is executed in main memory, control memory or both, Burroughs said.

In addition to peripherals listed for the B1714, the B1726 can handle disk pack drives, and head/track disk file subsystems, using up to eight buffered I/O controls.

Monthly lease prices of the B1726 range from $3,000 to $10,000. Comparable purchase prices would range from $135,000 to $475,000. Customer deliveries of the B1712 and B1714 systems will begin in the third quarter of 1972. Deliveries of the B1726 will start during the first quarter of 1973.

The B1700 systems all use variable micrologic to implement microprogramming techniques. The variable micrologic allows the system's CPU to adapt itself, dynamically, under program instruction, to a variety of program languages, Burroughs explained.

The use of microinstruction sets enables the systems to process any language, including programs written for other systems, at full efficiency, Burroughs said. The system restructures itself to the operating instruction requirement for a given language, allowing the user to select the language best suited to the problem he is trying to solve, rather than languages suited to the computer, Burroughs explained.

Users of small business systems, such as the IBM System 3, could realize faster execution times using IBM's present programs, Burroughs said.

The operating system on the B1700, the MCP (Master Control Program), is similar to but not compatible with the operating systems used with larger Burroughs machines. The MCP can execute several programs simultaneously. The number of jobs that can be multiprogrammed depends solely on the amount of storage available, Burroughs said.

A series of applications packages based on software originally designed for turnkey applications is available to B1700 users on an unbundled basis. Called Application Program Products, the packages are designed to provide operational control through daily, weekly, monthly and periodic management reports.

Packages are currently available for the following application areas: wholesale management, distributor management, manufacturing management, bank management and hospital management.

A cassette tape reader is used at the systems console for initial loading of system software and for entering diagnostic software for processor maintenance.

Burroughs introduced a new series of MICR read/sorters with the B1700. They provide a choice of eight to 12 distribution pockets and sorting speeds from 600 to 900 document/min. Other reader/sorters with speeds of 1,000 and 1,625 document/min, with four to 16 distribution pockets, are available.

Also new with the B1700 are removable cartridge disk drives with capacities ranging from a minimum of 2.3M bytes to a maximum subsystem of 55.2M bytes. The average access time is 80 msec.

Applications calling for removable storage media with higher speeds and greater on-line capacities can use disk pack drives with an average access time of 42.5 msec and a capacity of 95.5M bytes.

Line printers for B1700 systems offer speeds ranging from 90 to 1,040 line/min.

Magnetic tape units, including a new compact model and tape clusters with 2-, 3-, or 4-tape stations in a single housing, provide data transfer rates ranging from 10,000 to 36,000 byte/sec.

	B1712	B1714	B1726	IBM System 3/10
CPU Cycle Time	500 nsec	250 nsec	167 nsec	1,520 nsec
Memory Cycle Time	666 nsec/3 byte			1,520 nsec/byte
Memory Capacity	16K – 40K	16K – 64K	24K – 96K	8K – 48K
Unit of Storage	Variable			Byte
STORAGE				
Cartridge	Yes			
Head/track	No		Yes	No
Pack	No		Yes	
Mag Tape	Yes			
LANGUAGES				
Fortran	Yes			
Cobol	Yes			
Basic	Yes			No
RPG	Yes			
Assembler	No			Yes

The B1712 is comparable to the IBM System 3 Model 10. The 1714 and the 1726 are larger systems.

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EDITORIAL OFFICES: 797 Washington St., Newton, Mass. 02160 (617-332-5606; TWX 710-335-6635). Europe: Computerworld, c/o IDC Europa Ltd., 59 Grays Inn Rd., London, W.C.1, England (01-242-8908).

Second-class postage paid at Boston, Mass. and additional mailing offices. Published weekly (except: a single combined issue for the last week in December and the first week in January) by Computerworld, Inc., 797 Washington Street, Newton, Mass. 02160.

25 cents a copy; $9 a year in U.S.; $10 a year in Canada; Airmail to Western Europe and Japan, $15 a year. Other foreign rates on request. MARGARET PHELAN, *circulation manager*. Four weeks' notice required for change of address. Address all subscription correspondence to circulation manager, Computerworld, 797 Washington St., Newton, Mass. 02160.

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ACM Trying to Avert Bankruptcy

(Continued from Page 1)

full and associate members, as of July 1. The student rate of $8/yr remains in effect, but regular membership increases from $25 to $35. Other measures will also be taken, Carlson said.

The association had budgetary difficulties in the 1960s, but reduced the deficit to $189,000 at the end of fiscal 1970. The deficit nearly doubled to $336,000 at the end of fiscal 1971, and is estimated at $381,000 for this fiscal year, Carlson said. The fiscal year ends June 30.

For the last three months, Carlson has been reviewing the activities, successes and failures of the ACM presidency and the Council (the governing body), and in the last issue of *Communications*, the official monthly magazine, he predicted the dues increase [CW, May 17].

"Thousands of members and subscribers" have been "adversely affected" by the present levels of service "and have complained," Carlson noted.

The dues increase will reduce the 1973 deficit to an estimated $214,000, Carlson noted, still worse than the 1970 figure.

Other measures taken or planned in order to achieve cost conservation include continued vacancy for the post of education director and a downward modification of chapter rebates.

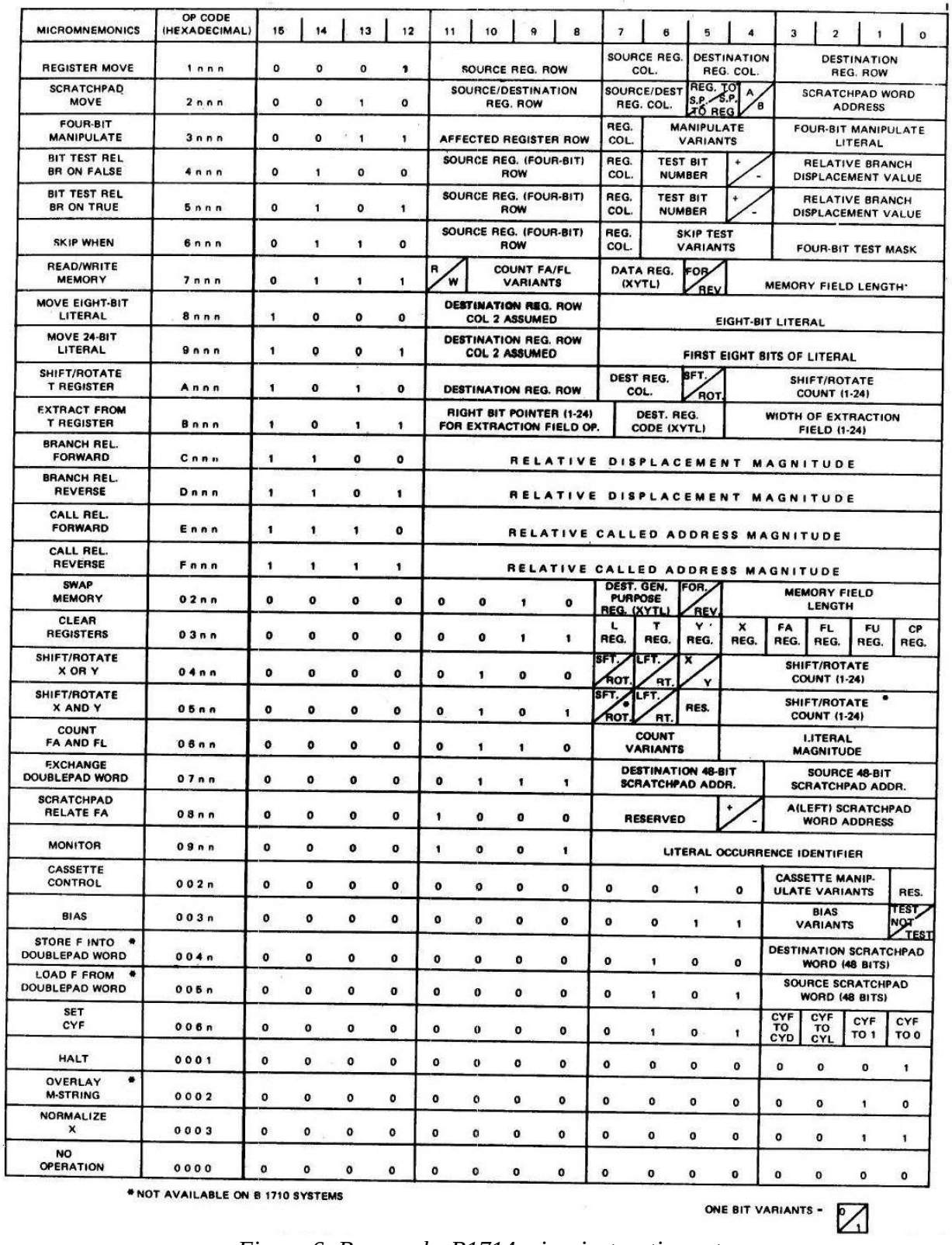
The ACM problem is closely tied to diminishing support from the computer industry, in the form of advertising in *Communications* and corporate memberships, as well as a drastic reduction in financial distribution from profits of the joint computer conferences.

Overall ACM membership increased 38% in the past four years, Carlson noted, but this was "not enough." In the same period, JCC contributions dropped from an average of $7.20/member to 80 cent/member; advertising had dropped from the same $7.20 to $2.10; money from corporate membership diminished from $1.40 to 80 cent/member.

The net result from outside support, then, is a drop from $15.80/member to $3.70/member; Carlson pointed out that the "dues increase of $10 does not even cover the loss of external support of $12.10/member."

The new rates will permit the association to try to restore some services, including adding staff members to handle activities of special-interest groups and committees. However, these "Sigs" will "pay for direct headquarters staff assistance," Carlson warned.

Figure 5: Burroughs B1714 introduction



MICROMNEMONICS	OP CODE (HEXADECIMAL)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REGISTER MOVE	1nnn	0	0	0	1	SOURCE REG. ROW				SOURCE REG. COL.		DESTINATION REG. COL.		DESTINATION REG. ROW			
SCRATCHPAD MOVE	2nnn	0	0	1	0	SOURCE/DESTINATION REG. ROW				SOURCE/DEST REG. COL.		REG. TO S.P. / S.P. TO REG	A / B	SCRATCHPAD WORD ADDRESS			
FOUR-BIT MANIPULATE	3nnn	0	0	1	1	AFFECTED REGISTER ROW				REG. COL.	MANIPULATE VARIANTS			FOUR-BIT MANIPULATE LITERAL			
BIT TEST REL BR ON FALSE	4nnn	0	1	0	0	SOURCE REG. (FOUR-BIT) ROW				REG. COL.	TEST BIT NUMBER		+ / -	RELATIVE BRANCH DISPLACEMENT VALUE			
BIT TEST REL BR ON TRUE	5nnn	0	1	0	1	SOURCE REG. (FOUR-BIT) ROW				REG. COL.	TEST BIT NUMBER		+ / -	RELATIVE BRANCH DISPLACEMENT VALUE			
SKIP WHEN	6nnn	0	1	1	0	SOURCE REG. (FOUR-BIT) ROW				REG. COL.	SKIP TEST VARIANTS			FOUR-BIT TEST MASK			
READ/WRITE MEMORY	7nnn	0	1	1	1	R / W	COUNT FA/FL VARIANTS			DATA REG. (XYTL)		FOR / REV	MEMORY FIELD LENGTH*				
MOVE EIGHT-BIT LITERAL	8nnn	1	0	0	0	DESTINATION REG. ROW COL 2 ASSUMED				EIGHT-BIT LITERAL							
MOVE 24-BIT LITERAL	9nnn	1	0	0	1	DESTINATION REG. ROW COL 2 ASSUMED				FIRST EIGHT BITS OF LITERAL							
SHIFT/ROTATE T REGISTER	Annn	1	0	1	0	DESTINATION REG. ROW				DEST REG. COL.		SFT. / ROT.	SHIFT/ROTATE COUNT (1-24)				
EXTRACT FROM T REGISTER	Bnnn	1	0	1	1	RIGHT BIT POINTER (1-24) FOR EXTRACTION FIELD OP.				DEST. REG. CODE (XYTL)			WIDTH OF EXTRACTION FIELD (1-24)				
BRANCH REL. FORWARD	Cnnn	1	1	0	0	RELATIVE DISPLACEMENT MAGNITUDE											
BRANCH REL. REVERSE	Dnnn	1	1	0	1	RELATIVE DISPLACEMENT MAGNITUDE											
CALL REL. FORWARD	Ennn	1	1	1	0	RELATIVE CALLED ADDRESS MAGNITUDE											
CALL REL. REVERSE	Fnnn	1	1	1	1	RELATIVE CALLED ADDRESS MAGNITUDE											
SWAP MEMORY	02nn	0	0	0	0	0	0	1	0	DEST. GEN. PURPOSE REG. (XYTL)		FOR. / REV.	MEMORY FIELD LENGTH				
CLEAR REGISTERS	03nn	0	0	0	0	0	0	1	1	L REG.	T REG.	Y REG.	X REG.	FA REG.	FL REG.	FU REG.	CP REG.
SHIFT/ROTATE X OR Y	04nn	0	0	0	0	0	1	0	0	SFT. / ROT.	LFT. / RT.	X / Y	SHIFT/ROTATE COUNT (1-24)				
SHIFT/ROTATE X AND Y	05nn	0	0	0	0	0	1	0	1	SFT. / ROT.*	LFT. / RT.	RES.	SHIFT/ROTATE COUNT (1-24)*				
COUNT FA AND FL	06nn	0	0	0	0	0	1	1	0	COUNT VARIANTS			LITERAL MAGNITUDE				
EXCHANGE DOUBLEPAD WORD	07nn	0	0	0	0	0	1	1	1	DESTINATION 48-BIT SCRATCHPAD ADDR.				SOURCE 48-BIT SCRATCHPAD ADDR.			
SCRATCHPAD RELATE FA	08nn	0	0	0	0	1	0	0	0	RESERVED			+ / -	A(LEFT) SCRATCHPAD WORD ADDRESS			
MONITOR	09nn	0	0	0	0	1	0	0	1	LITERAL OCCURRENCE IDENTIFIER							
CASSETTE CONTROL	002n	0	0	0	0	0	0	0	0	0	0	1	0	CASSETTE MANIPULATE VARIANTS			RES.
BIAS	003n	0	0	0	0	0	0	0	0	0	0	1	1	BIAS VARIANTS			TEST / NOT TEST
STORE F INTO DOUBLEPAD WORD *	004n	0	0	0	0	0	0	0	0	0	1	0	0	DESTINATION SCRATCHPAD WORD (48 BITS)			
LOAD F FROM DOUBLEPAD WORD *	005n	0	0	0	0	0	0	0	0	0	1	0	1	SOURCE SCRATCHPAD WORD (48 BITS)			
SET CYF	006n	0	0	0	0	0	0	0	0	0	1	0	1	CYF TO CYD	CYF TO CYL	CYF TO 1	CYF TO 0
HALT	0001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
OVERLAY M-STRING *	0002	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
NORMALIZE X	0003	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
NO OPERATION	0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

* NOT AVAILABLE ON B 1710 SYSTEMS

ONE BIT VARIANTS - 0 / 1

Figure 6: Burroughs B1714 microinstruction set

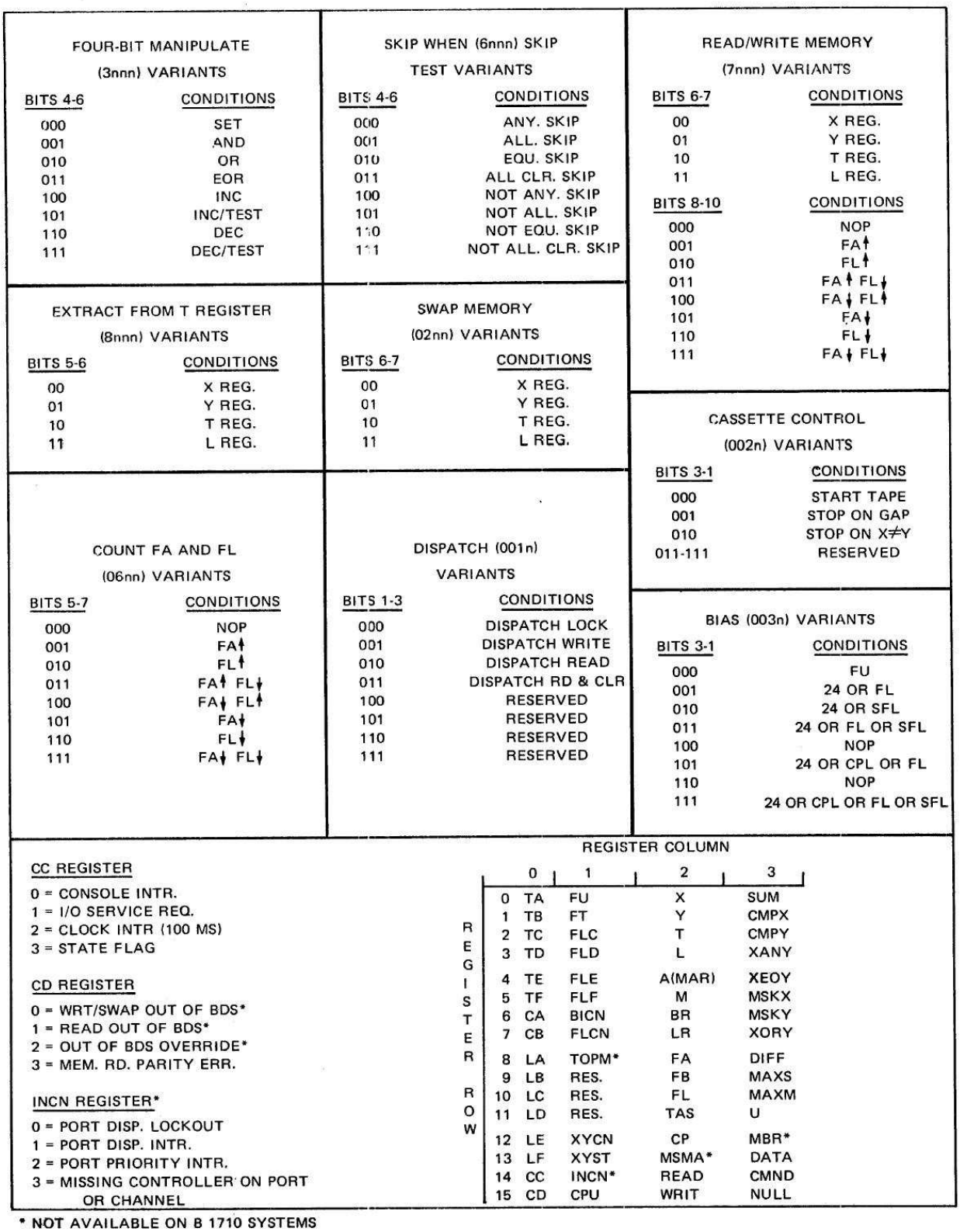


Figure 7: Burroughs B1714 microinstruction fields

RD BITS / UNIT	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	CONTROLLER * ID. (17-23)
CARD READER	VALIDITY CHECK	MEMORY ACCESS ERROR		READ CHECK												CTL. 1 0101010 CTL. 2 0010100
CARD PUNCH	PUNCH CHECK	MEMORY ACCESS ERROR	MEMORY PARITY ERROR													CTL. 0000100
PAPER TAPE READER	TAPE PARITY ERROR	MEMORY ACCESS ERROR		END OF TAPE	BEGINNING OF TAPE		SHORT REC. RD.	UNIT REWINDING								CTL. 10001110 CTL. 20001100
LINE PRINTER	PRINT CHECK		MEMORY PARITY ERROR	END OF PAGE	7-9 = CHAR. SET* 000 = 64 001 = 48 010 = 16		011 = 96 100 = 192	10-11 PRT. SPD.* 00 = 400/860 01 = 300 10 = 600	11 = 1100	PAPER * IN MOTION	MOTOR * ON TEST	NO. PRT. POS. 00 = 132 01 = 120 11 = 80				CTL. 0010110
CONSOLE PRINTER	KEYBOARD E. CANCEL		ATTP. TO EXECUTE END ADDR.		INPUT REQUEST											CTL. 0010110
READER SORTER	UNENCODED DOCUMENT	MEMORY ACCESS ERROR	CANNOT READ	AMOUNT FIELD ERROR	ON-US FIELD ERROR	TRANSIT FIELD ERROR	DOUBLE DOCUMENTS	TOO LATE TO READ	JAM	MISSORT	BATCH TICKET	FLOW STOPPED	EMPTY HOPPER, FULL STACKER			CTL. 0010100
MAGNETIC TAPE	TAPE PARITY ERROR. BUSY	MEMORY ACCESS ERROR	MEMORY PARITY ERROR	END OF TAPE	BEGINNING OF TAPE	WRITE LOCKOUT	END OF FILE	UNIT REWINDING	TIME-OUT (3 FT. BLANK TAPE)	CRC ERROR TRACK IN ERROR TRACK/DENSITY * 000 = 7T. 200 001 = 7T. 556 011 = 7T. 800 101 = 9T. 800 111 = 9T. 1600			000-111 (0-7)	LONG REC.	SHORT REC.	MTC1–0110010 MTC2–0110000 MTC3–0110100 MTC4–0110110 MTC5–0111000
MFCU	INV. CH. COL. 1	MEMORY ACCESS ERROR	MEMORY PARITY ERROR	READ CHECK	PUNCH CHECK	PRI. HOP. EMPTY	SEC. HOP. EMPTY									CTL. 0001000
DISK CARTRIDGE	READ PARITY ERROR	MEMORY ACCESS ERROR	MEMORY PARITY ERROR	WRITE LOCKOUT	TRACK 100 = 203T/2200	OVERRUN	DENSITY 110 = 406/2200		SEEK	SEEK * STATUS		SEEKING				CTL. 0011100
SINGLE LINE	PARITY ERROR	MEMORY ACCESS ERROR	MEMORY PARITY ERROR	TIME-OUT	BREAK DET.	END. CTL. CODE NOT RECEIVED	CHAINING TERM	LOSS OF CLR. TO SD.	CARRIER LOSS		OFF HOOK	RINGING OR ENQ.				SEE BELOW
DISK PACK	READ PARITY ERROR	MEMORY ACCESS ERROR	MEMORY PARITY ERROR	WRITE LOCKOUT	TRANS. P.E. 001 = 20SUR/203T	OVERRUN 010 = 20SUR/406T	TRK/DENS.*	ADDRESS PARITY ERROR	SEEK T.O.	SEEK * STATUS	CTL. NO. 0/1	SEEKING				CTL. 0011110

* TEST DESCRIPTOR ONLY

COMMON RESULT DESCRIPTOR BITS:
0 = I/O COMPLETE
1 = EXCEPTION CONDITION
2 = NOT READY

DATA COMMUNICATIONS CTL. ID. BITS 17-23
1000000 = ADAPTER NOT PRESENT
10nnnnn = LEASED OR DIRECT CONNECT
11nnnnn = SWITCHED LINE
nnnnn = 00010 – STANDARD LINE ADAPTER
01000 – TELETYPE ADAPTER
00100 – A.C.U. ADAPTER

Figure 8: Burroughs B1714 input/output conditions

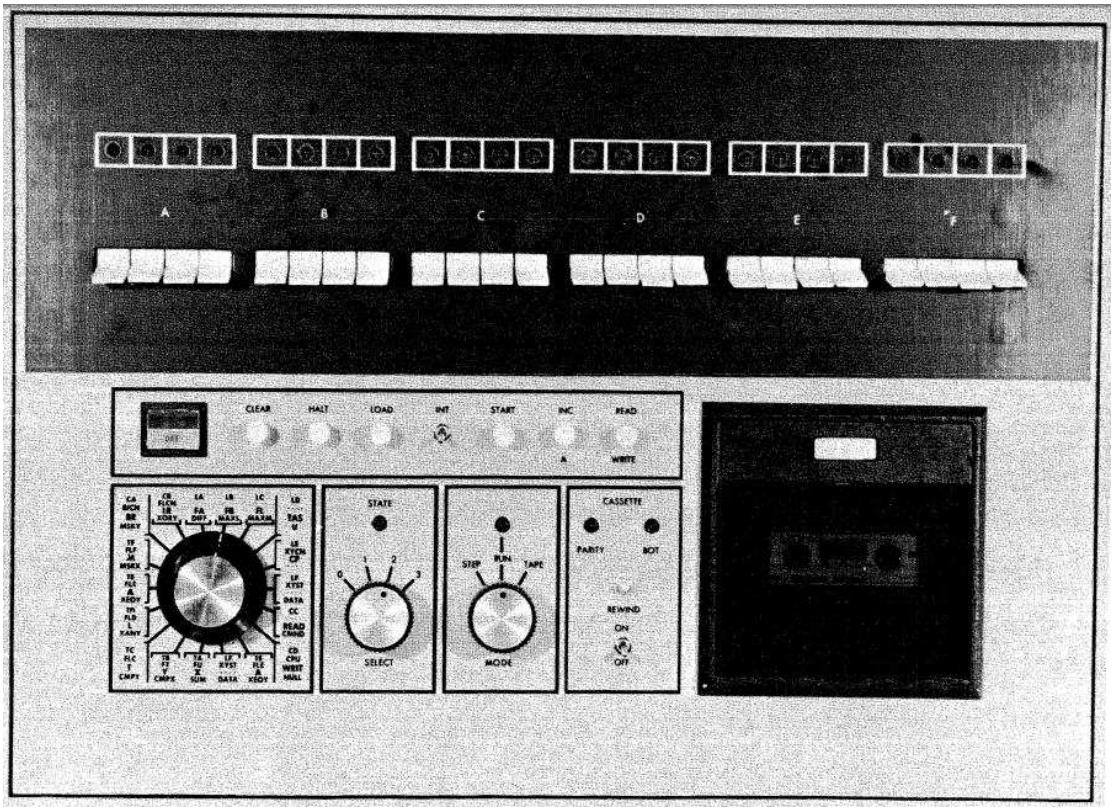


Figure 9: Burroughs B1714 control panel

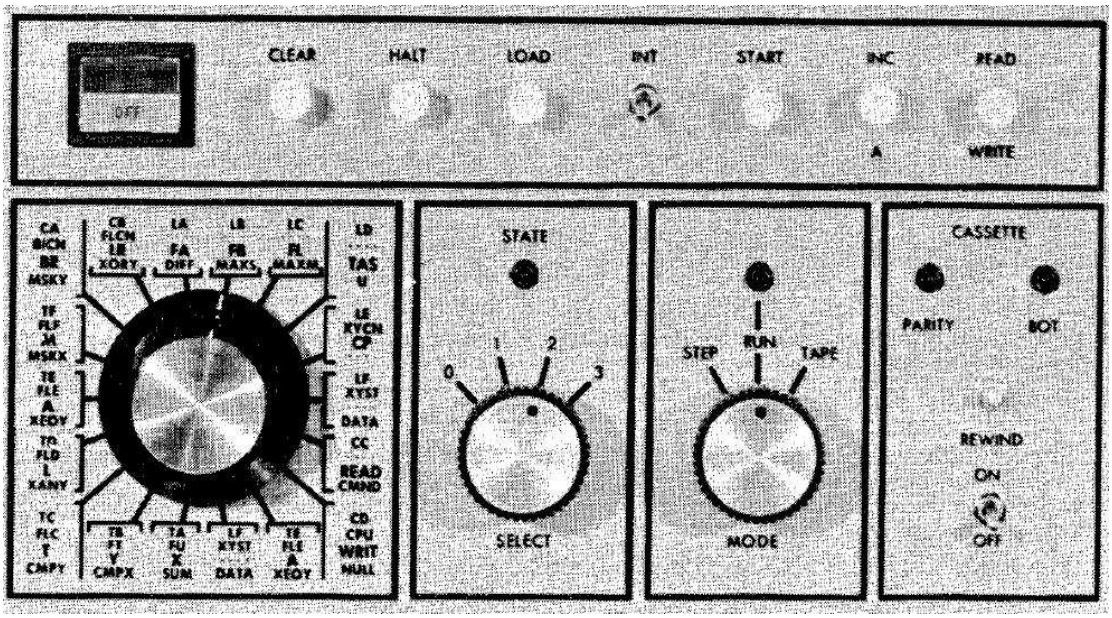


Figure 10: Burroughs B1714 controls closeup

Figure 11: TCD's Burroughs B1714 in action, view of front panel

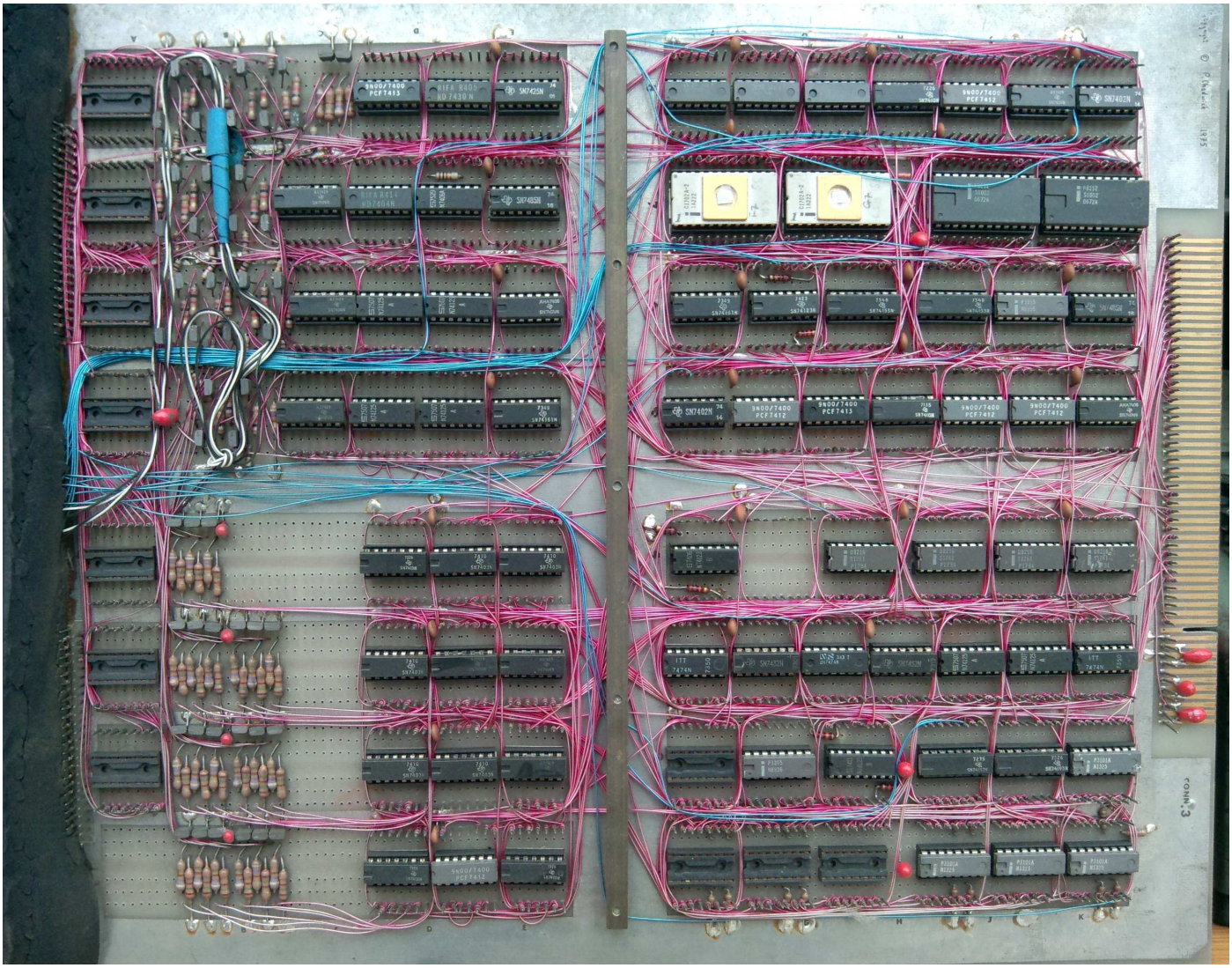


Figure 12: Burroughs B1714 prototyping board 1

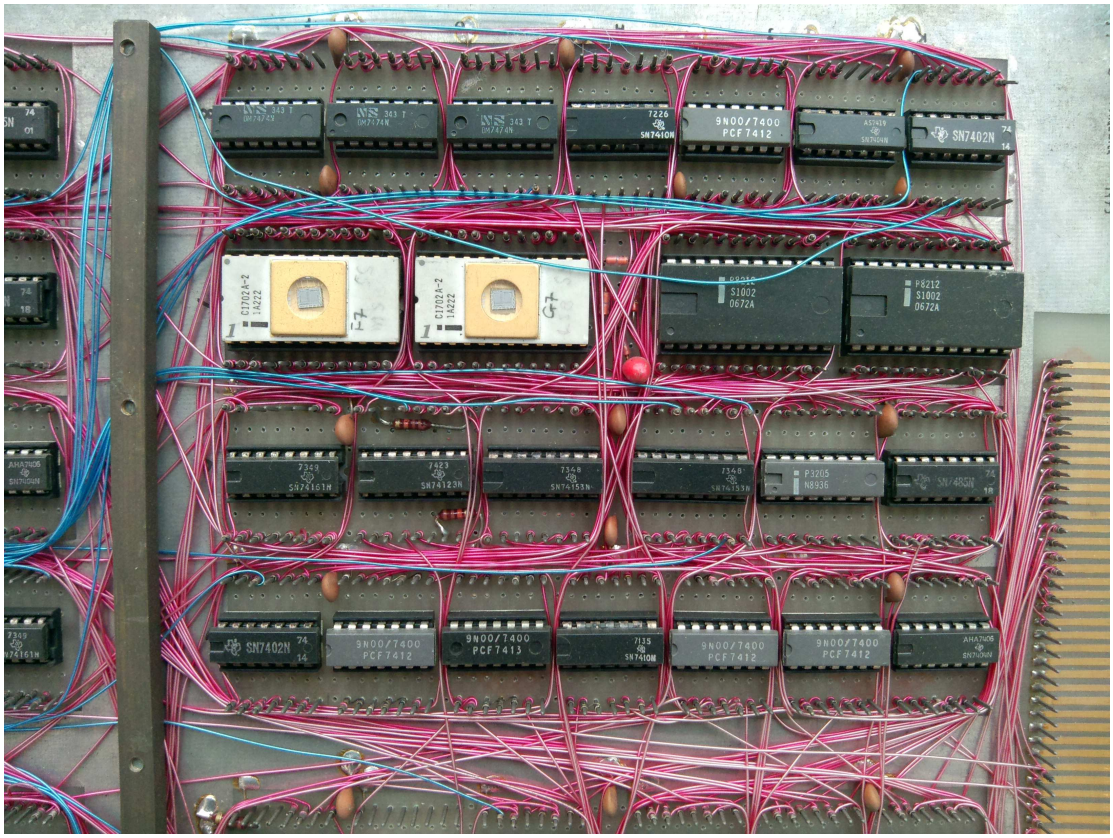


Figure 13: Burroughs B1714 prototyping board 1 closeup

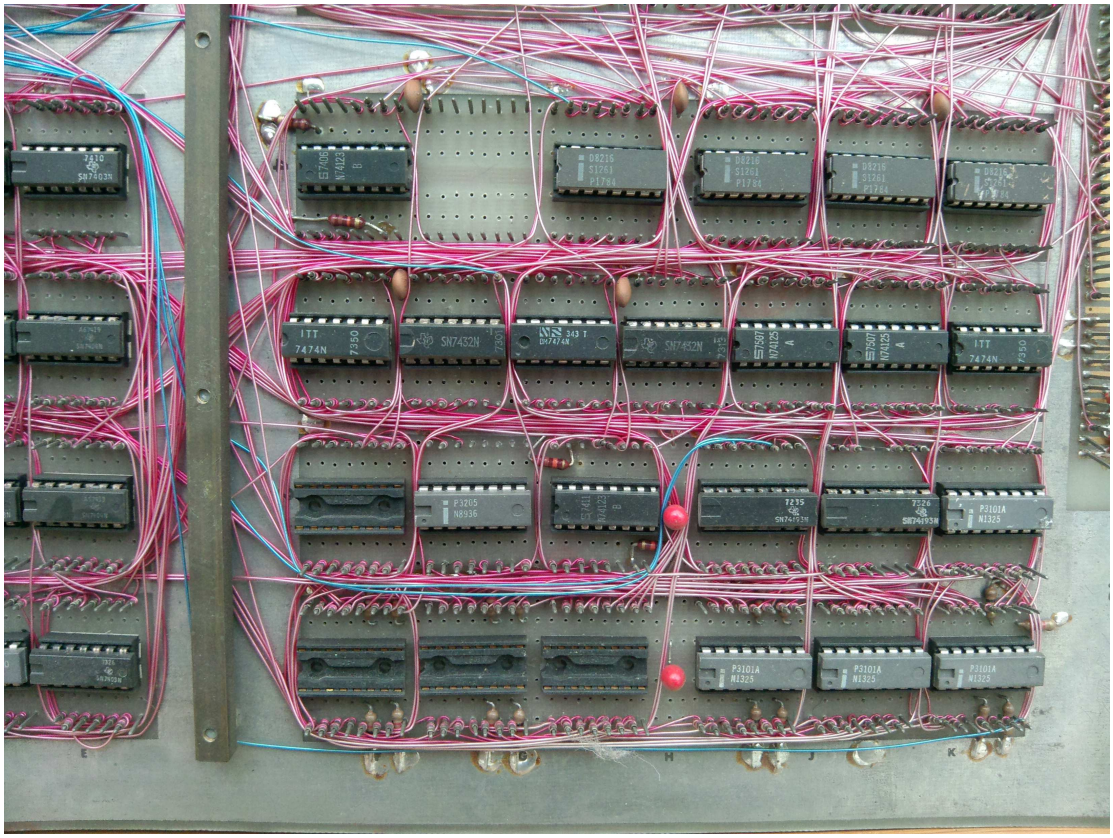


Figure 14: Burroughs B1714 prototyping board 1 closeup

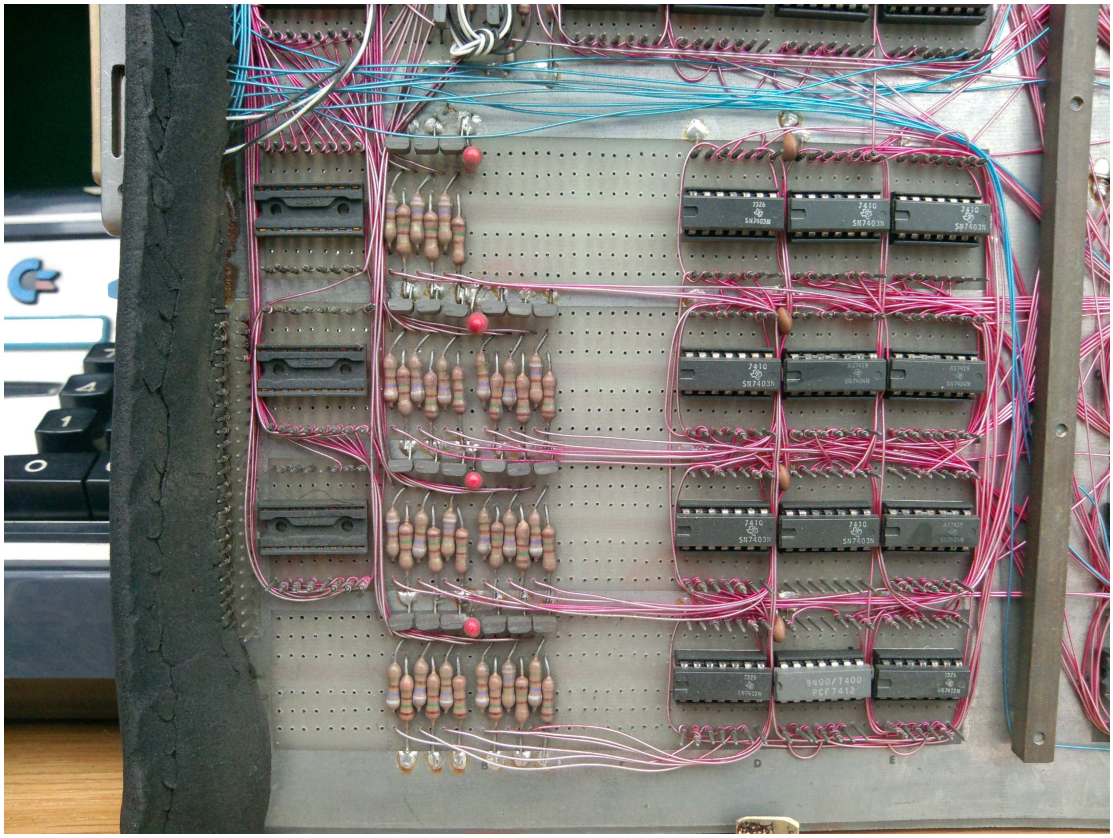


Figure 15: Burroughs B1714 prototyping board 1 closeup

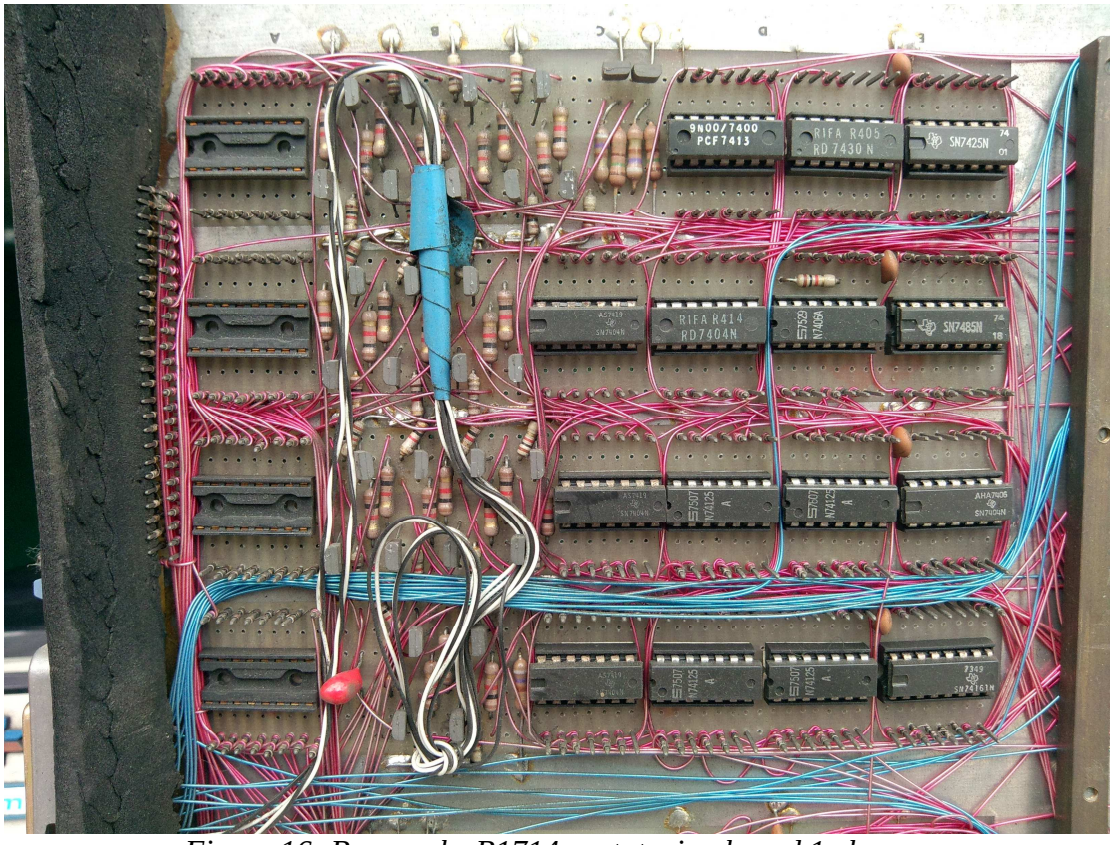


Figure 16: Burroughs B1714 prototyping board 1 closeup

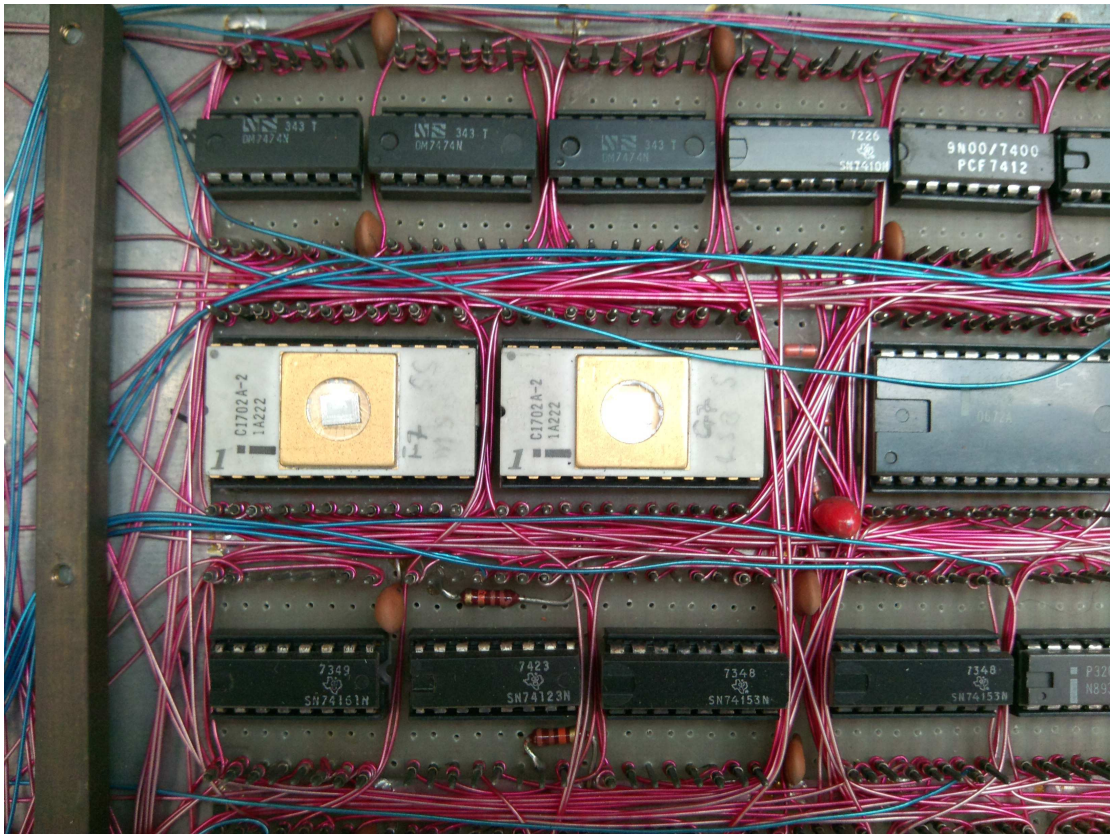


Figure 17: Burroughs B1714 prototyping board 1 EPROM closeup

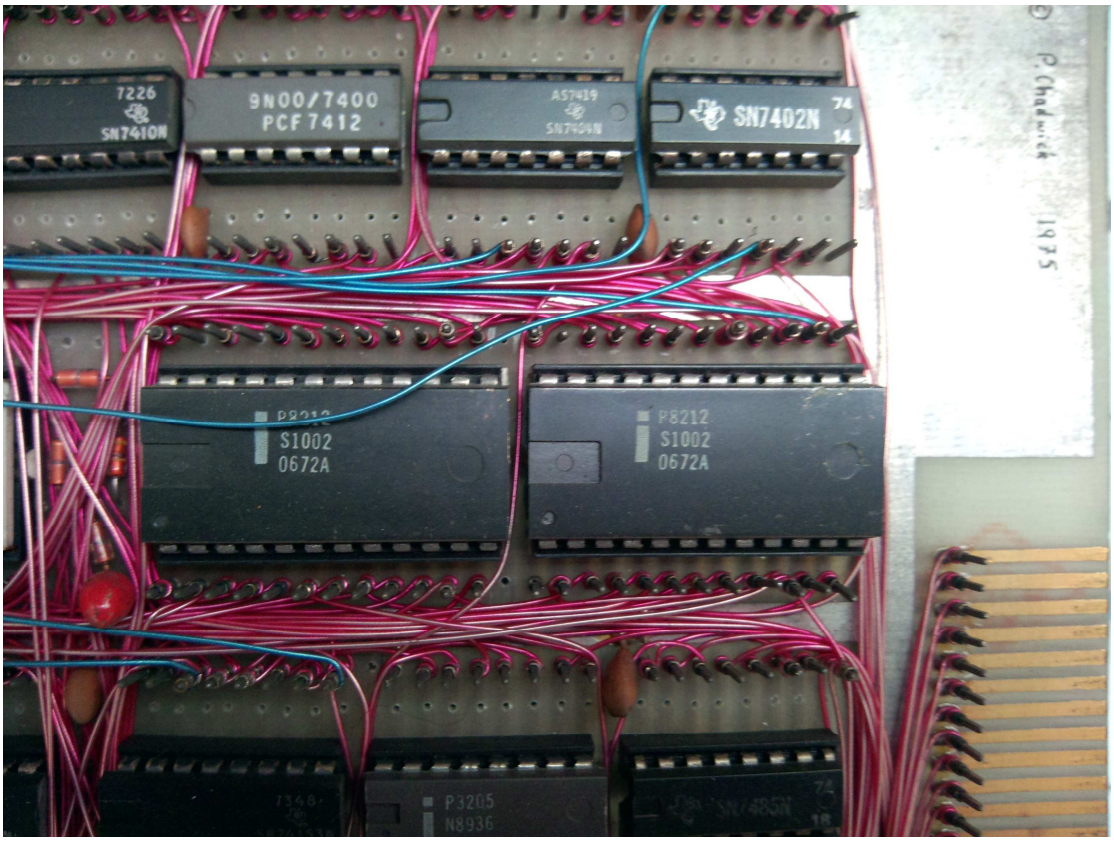


Figure 18: Burroughs B1714 prototyping board 1 Intel P8212 closeup
Note legend: "Copyright P.Chadwick 1975

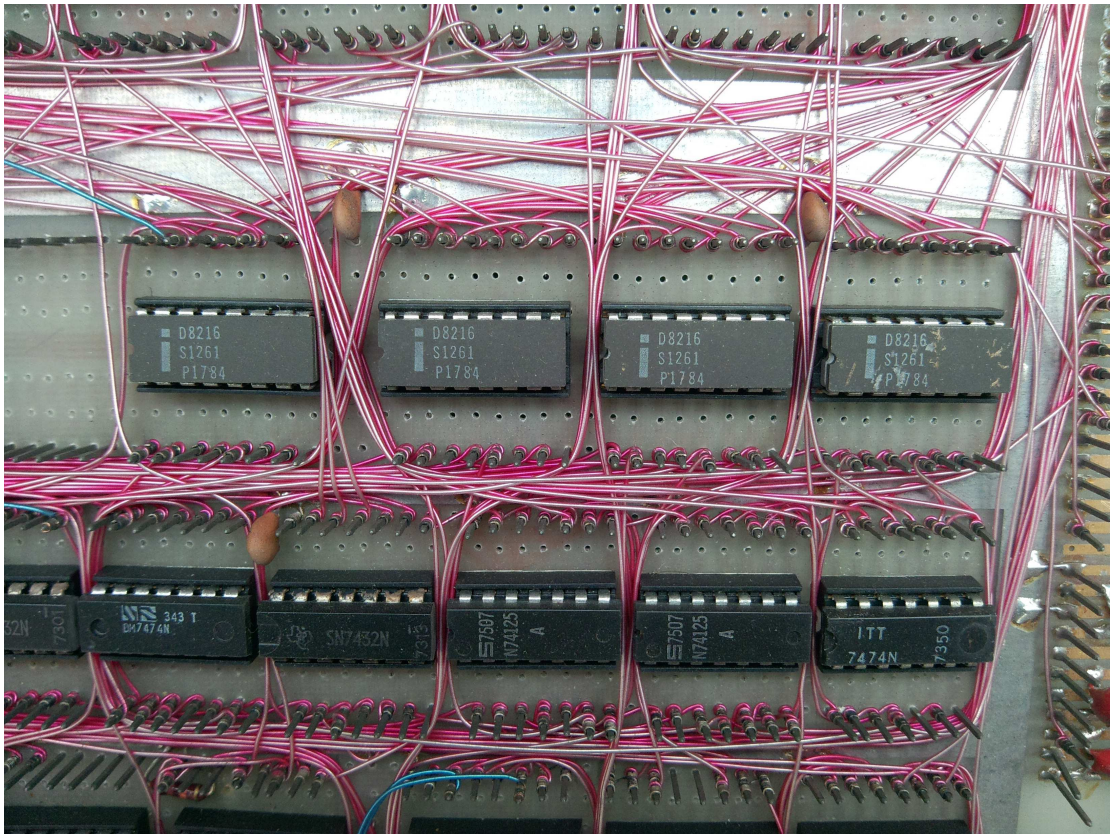


Figure 19: Burroughs B1714 prototyping board 1 closeup

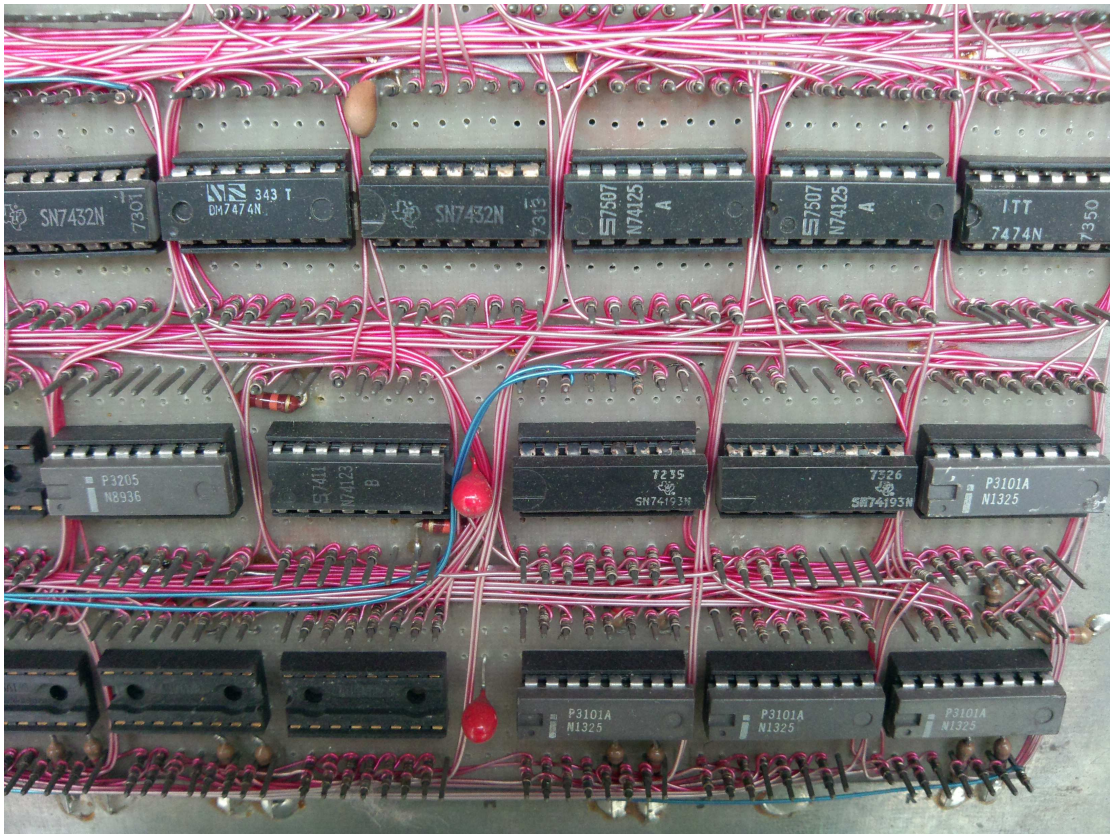


Figure 20: Burroughs B1714 prototyping board 1 closeup

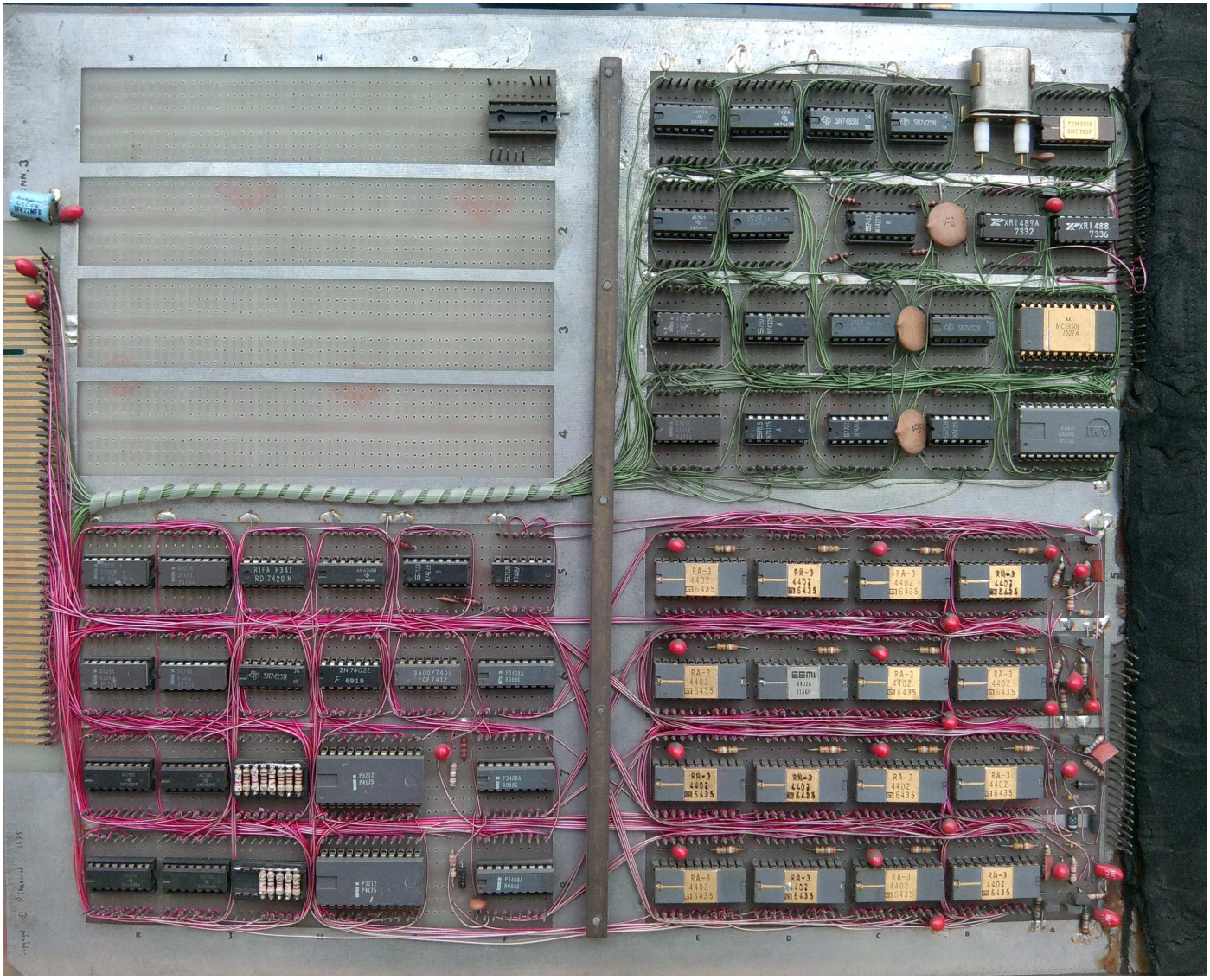


Figure 21: Burroughs B1714 prototyping board 2 closeup

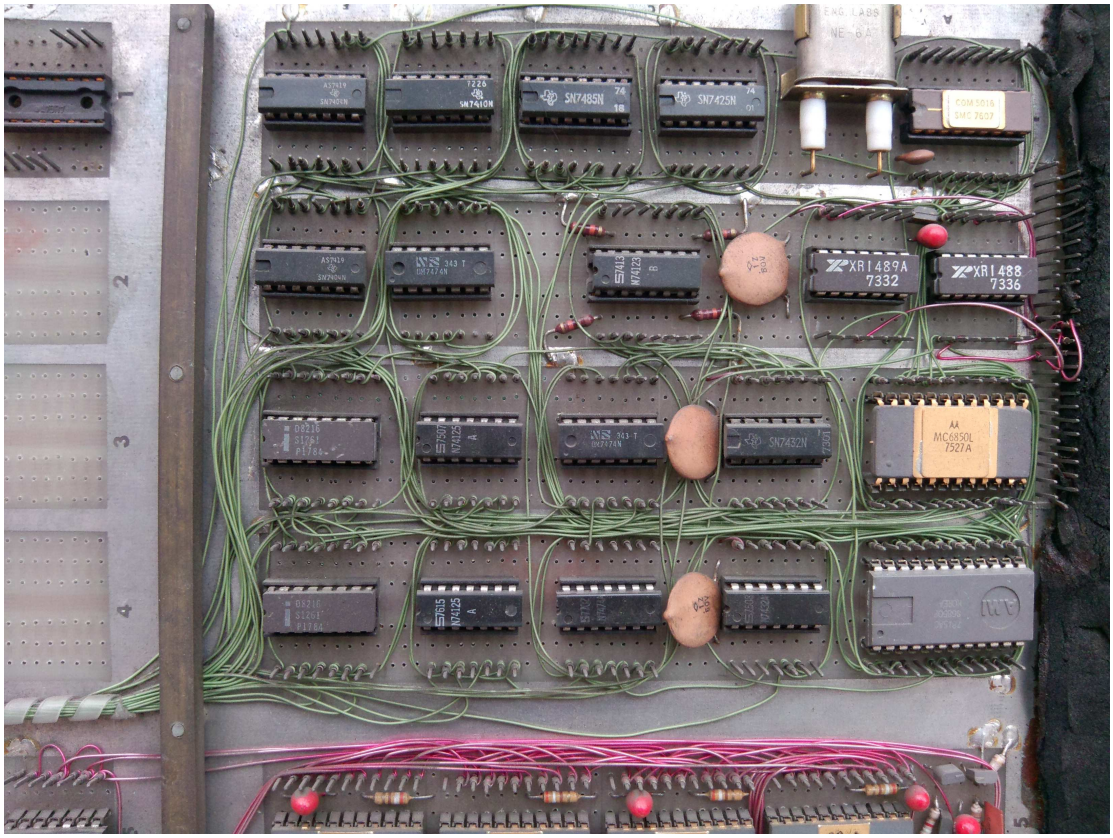


Figure 22: Burroughs B1714 prototyping board 2 closeup

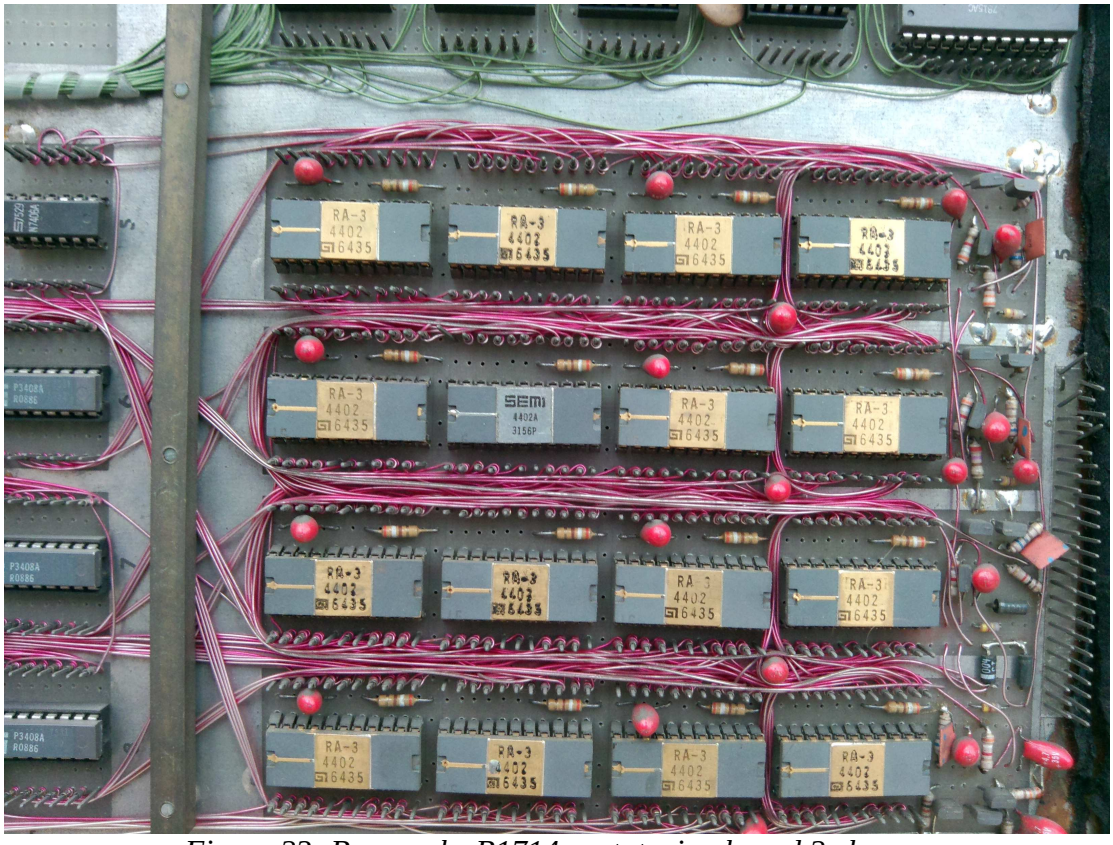


Figure 23: Burroughs B1714 prototyping board 2 closeup

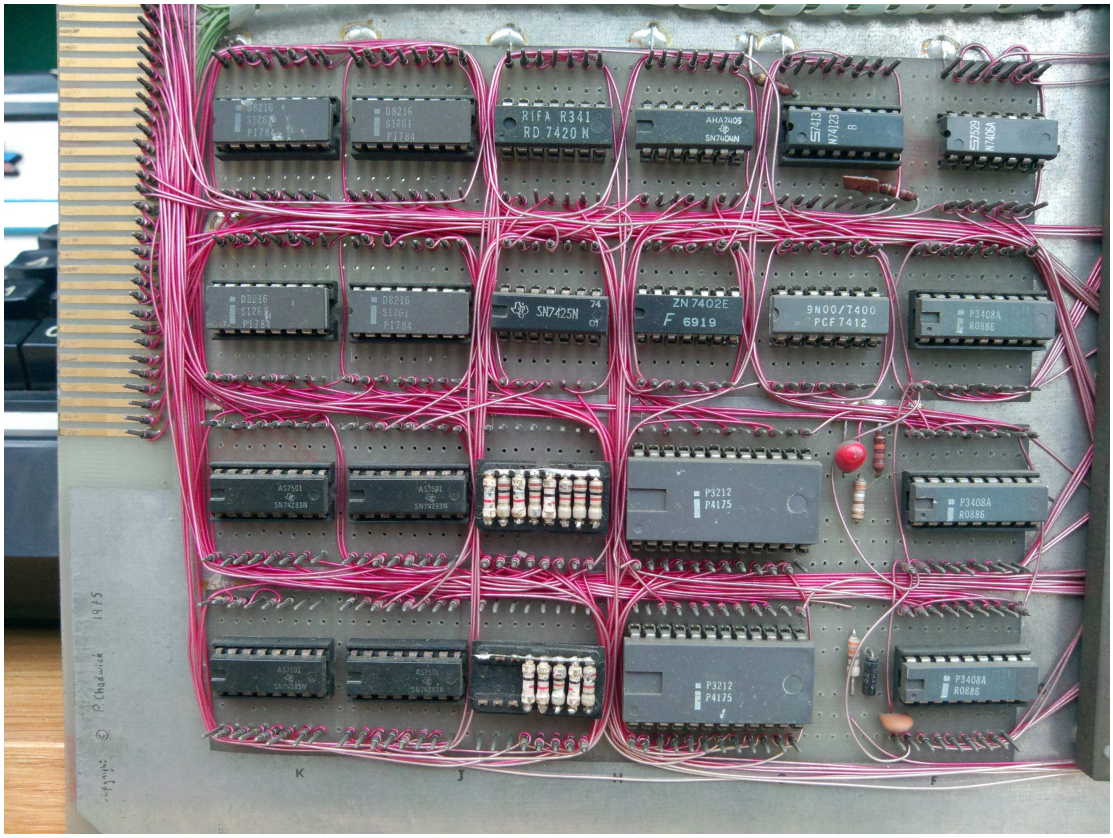


Figure 24: Burroughs B1714 prototyping board 2 closeup

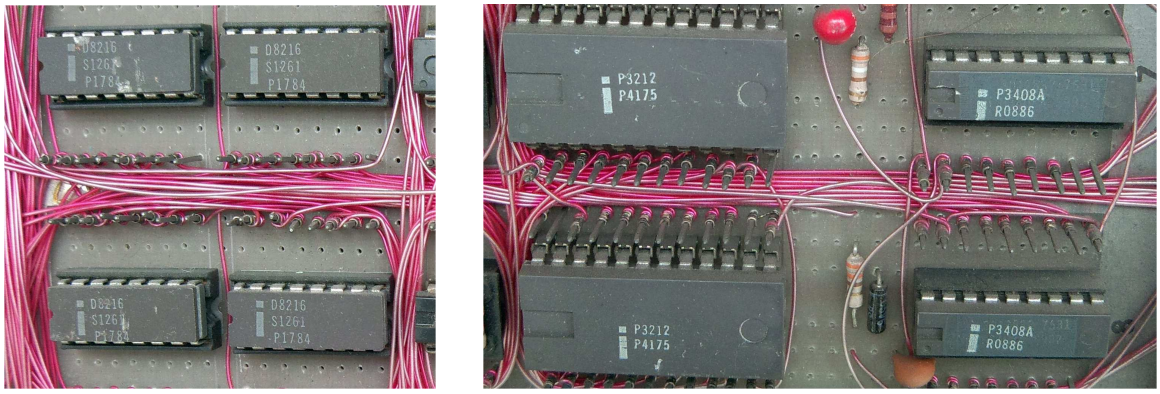


Figure 25: Burroughs B1714 prototyping board 2 closeups

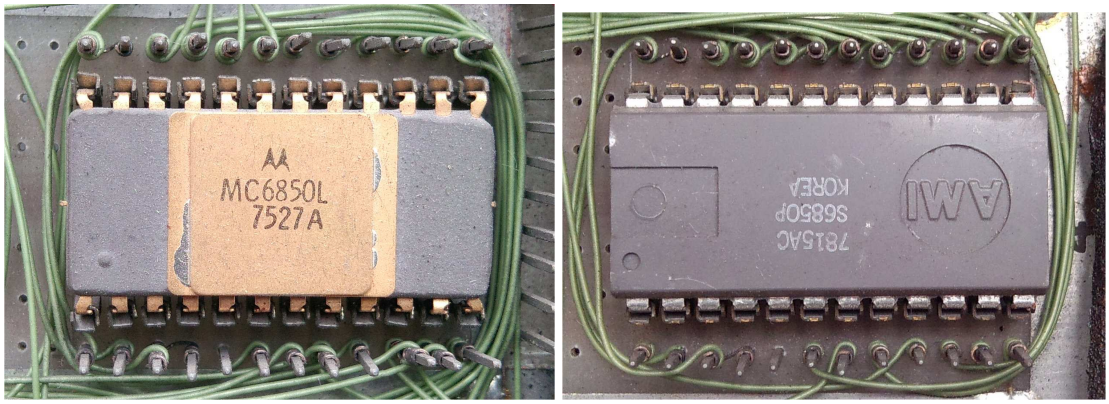


Figure 26: Burroughs B1714 prototyping board 2 ACIA closeups
(a) Motorola MC6850 ACIA, (b) AMI S6850 ACIA

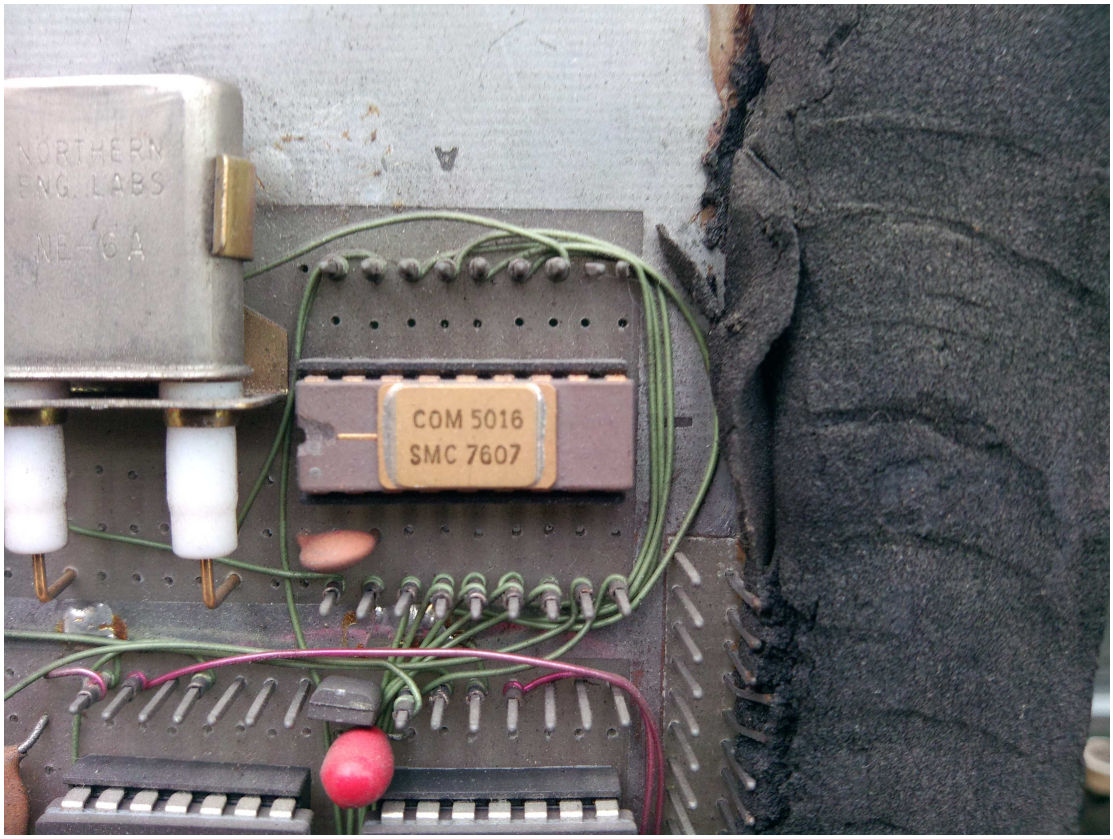


Figure 27: Burroughs B1714 prototyping board 2 closeup

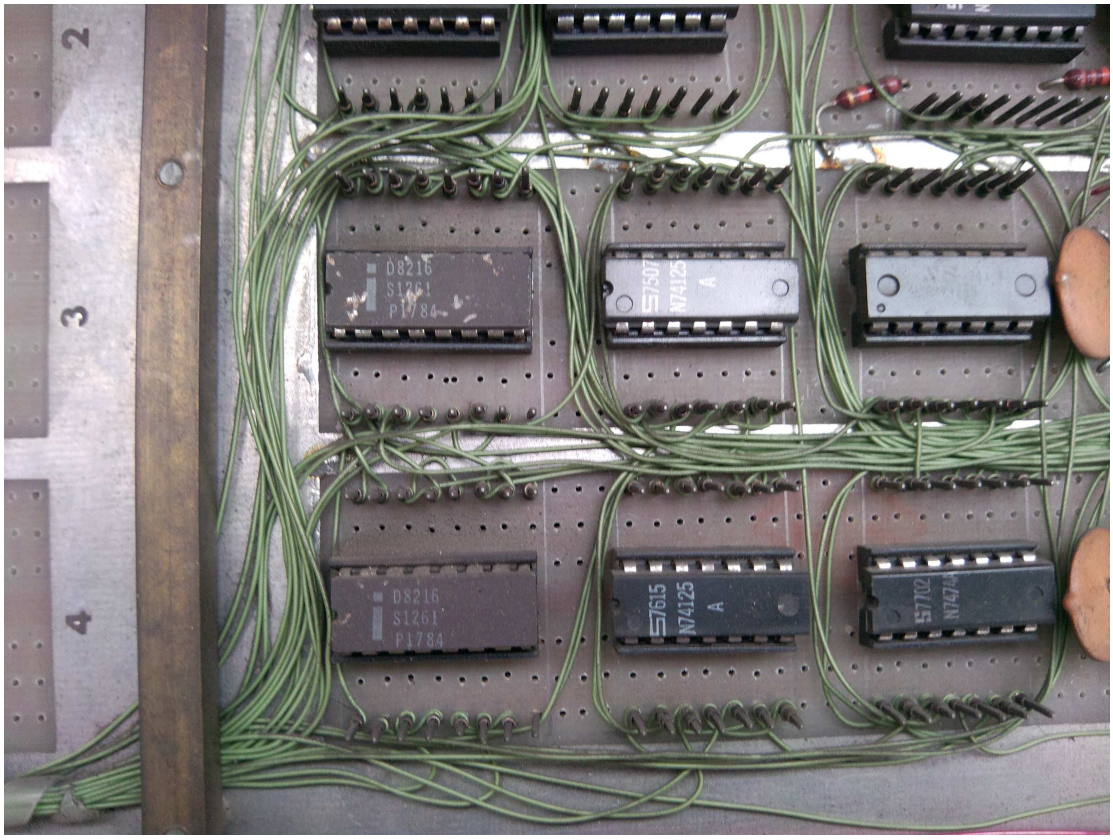


Figure 28: Burroughs B1714 prototyping board 2 closeup